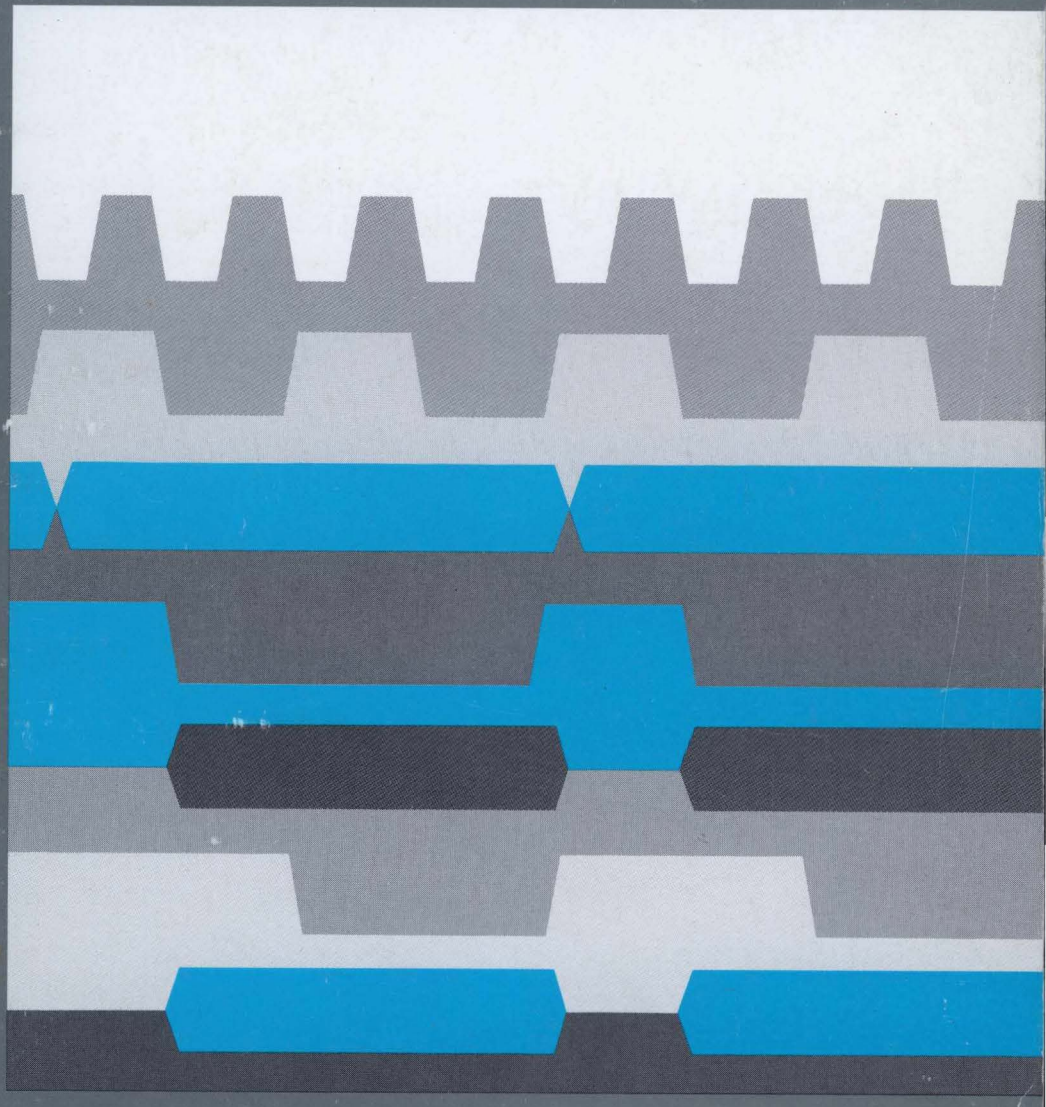
HITACHI®

GRAPHIC MEMORY DATA BOOK



Graphic Memory Data Book

May 17, 1994

HITACHI®

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Contents

Section 1

Synchronous DRAM

HM5241605 Series

Preliminary

131,072-word x 16-bit x 2-bank Synchronous Dynamic RAM

HITACHI

Rev. 0.3
Apr. 13, 1994

All inputs and outputs are referred to the rising edge of the clock input. The HM5241605 is offered in 2 banks for improved performance.

Features

- 3.3V Power supply
- Clock frequency
  66 MHz/57 MHz/50 MHz
- LVTTL interface
- Single pulsed $\overline{RAS}$
- 2 Banks can operates simultaneously and independently
- Burst read/write operation and burst read/single write operation capability
- Programmable burst length
  1/2/4/8/full page
- Programmable burst sequence
  Sequential/interleave
- Full page burst length capability
  Sequential burst
  burst stop capability
- Programmable $\overline{CAS}$ latency
  1/2/3
- Byte control by DQMU and DQML
- 1024 refresh cycles: 16 ms
- 2 variations of refresh
  — Auto refresh
  — Self refresh

Ordering Information

Type No.	Frequency	Package
HM5241605TT-20	50 MHz	400-mil 50-pin
HM5241605TT-17	57 MHz	plasticTSOP II
HM5241605TT-15	66 MHz	(TTP-50D)

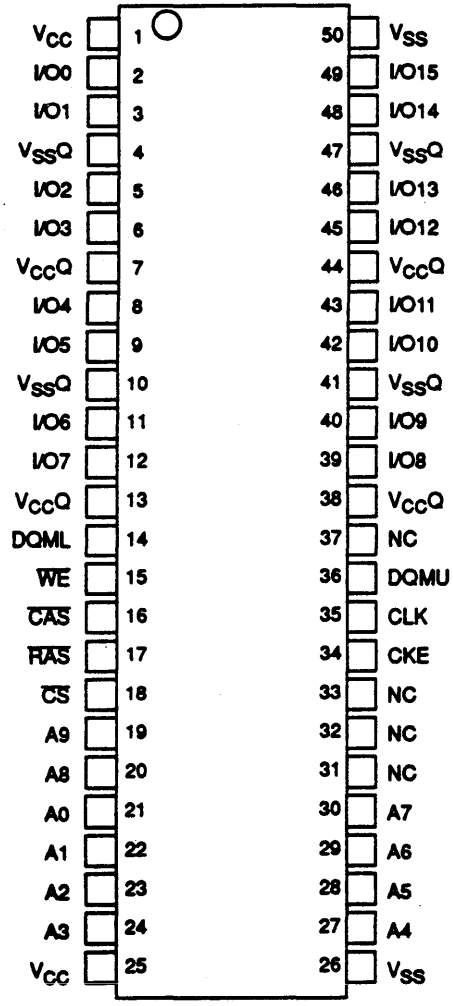
Preliminary: This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

Hitachi semiconductor

ADE-203-186(C)(Z)

Pin Arrangement

HM5241605TT Series

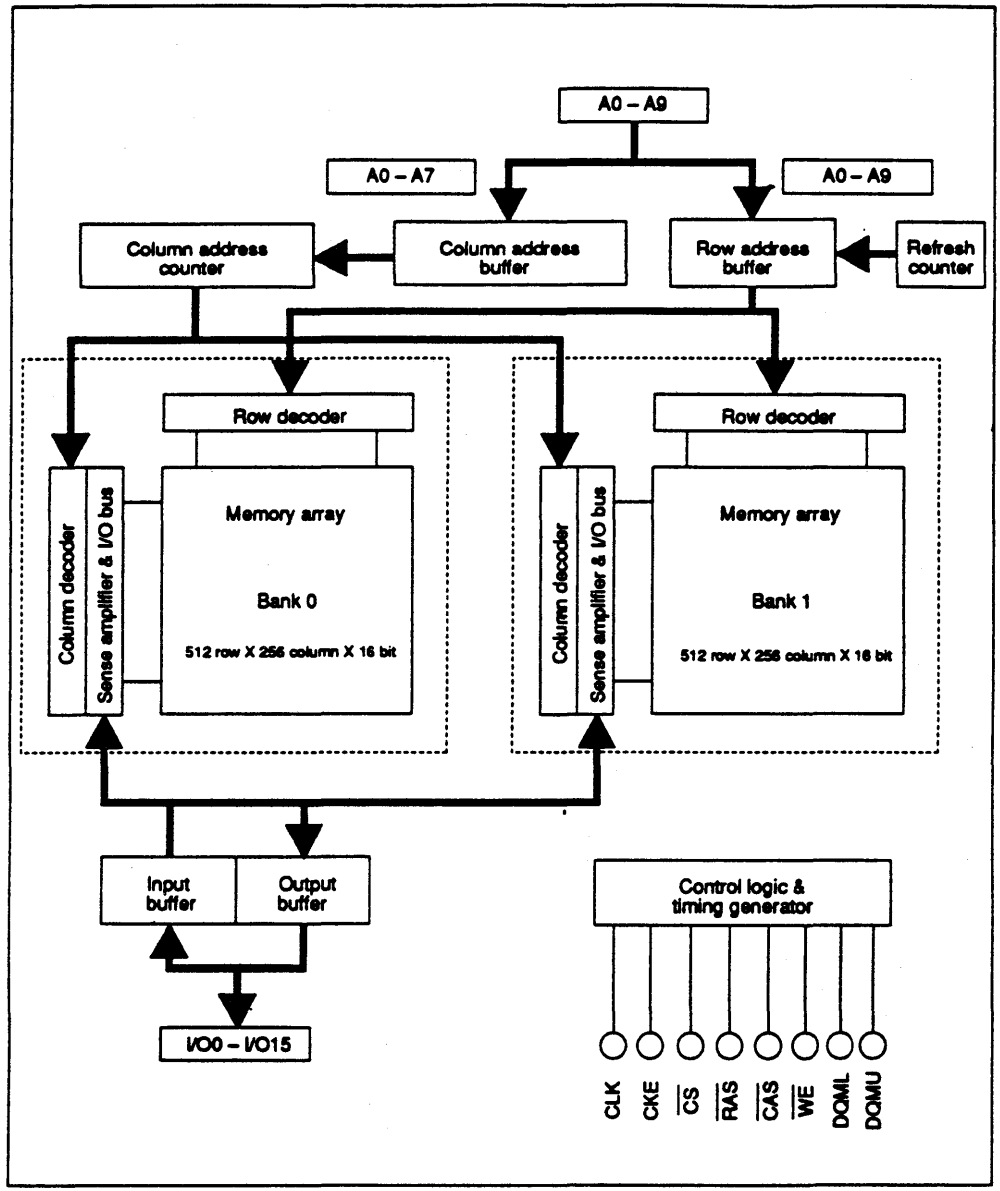


(Top View)

Pin Description

Pin name	Function
A0 – A9	Address input – Row address A0 – A8 – Column address A0 – A7 – Bank select address A9
I/O0 – I/O15	Data-input/output
$\overline{CS}$	Chip select
$\overline{RAS}$	Row address strobe command
$\overline{CAS}$	Column address strobe command
$\overline{WE}$	Write enable command
DQMU DQML	Upper byte input/output mask Lower byte input/output mask
CLK	Clock input
CKE	Clock enable
V_{CC}	Power for internal circuit (3.3 V)
V_{SS}	Ground for internal circuit
$V_{CC}Q$	Power for I/O pin (3.3 V)
$V_{SS}Q$	Ground for I/O pin
NC	No connection

Block Diagram



Pin Functions

CLK (input pin): CLK is the master clock input to this pin. The other input signals are referred at CLK rising edge.

$\overline{CS}$ (input pin): When $\overline{CS}$ is Low, the command input cycle becomes valid. When $\overline{CS}$ is High, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.

$\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ (input pins): Although these pin names are the same as those of conventional DRAMs, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.

A0 to A8 (input pins): Row address (AX0 to AX8) is determined by A0 to A8 level at the bank active command cycle CLK rising edge. Column address (A0 to A7) is determined by A0 to A7 level at the read or write command cycle CLK rising edge. And this column address becomes burst access start address. A8 defines the precharge mode. When A8 = High at the precharge command cycle, both banks are precharged. But when A8 = Low at the precharge command cycle, only the bank that is selected by A9(BS) is precharged.

A9 (input pin): A9 is a bank select signal (BS). The memory array of the HM5241605 is divided into bank 0 and bank 1, both which contain 512 row x 256 column x 16 bits. If A9 is Low, bank 0 is selected, and if A9 is High, bank 1 is selected.

CKE (input pin): This pin determines whether or not the next CLK is valid. If CKE is High, the next CLK rising edge is valid. If CKE is Low, the next CLK rising edge is invalid. This pin is used for power-down and clock suspend modes.

DQMU/DQML (input pins): DQMU controls upper byte and DQML controls lower byte input/output buffers.
Read operation: If DQMU/DQML is High, the output buffer becomes High-Z. If the DQMU/DQML is Low, the output buffer becomes Low-Z.
Write operation: If DQMU/DQML is High, the previous data is held (the new data is not written). If DQMU/DQML is Low, the data is written.

I/O0 to I/O15 (I/O pins): Data is input to and output from these pins. These pins are the same as those of a conventional DRAM.

V_{CC} and $V_{CC}Q$ (power supply pins): 3.3 V is applied. (V_{CC} is for the internal circuit and $V_{CC}Q$ is for the output buffer.)

V_{SS} and $V_{SS}Q$ (power supply pins): Ground is connected. (V_{SS} is for the internal circuit and $V_{SS}Q$ is for the output buffer.)

Command Operation

Command Truth Table

The synchronous DRAM recognizes the following commands specified by the $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and address pins.

Function	Symbol	CKE n-1	n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	A9	A8	A7 - 0
Ignore command	DESL	H	X	H	X	X	X	X	X	X
No operation	NOP	H	X	L	H	H	H	X	X	X
Burst stop in full page	BST	H	X	L	H	H	L	X	X	X
Column address and read command	READ	H	X	L	H	L	H	V	L	V
Read with auto-precharge	READ A	H	X	L	H	L	H	V	H	V
Column address and write command	WRIT	H	X	L	H	L	L	V	L	V
Write with auto-precharge	WRIT A	H	X	L	H	L	L	V	H	V
Row address strobe and bank act.	ACTV	H	X	L	L	H	H	V	V	V
Precharge select bank	PRE	H	X	L	L	H	L	V	L	X
Precharge all bank	PALL	H	X	L	L	H	L	X	H	X
Refresh	REF/SELF	H	V	L	L	L	H	X	X	X
Mode register set	MRS	H	X	L	L	L	L	L	L	V

Note: H: V_{IH}. L: V_{IL}. X: V_{IH} or V_{IL}. V: Valid address input

•**Ignore command [DESL]:** When this command is set ($\overline{CS}$ is High), the synchronous DRAM ignore command input at the clock. However, the internal status is held.

•**No operation [NOP]:** This command is not an execution command. However, the internal operations continue.

•**Burst stop in full-page [BST]:** This command stops a full-page burst operation (burst length = full-page(256)), and is illegal otherwise. Full page burst continues until this command is input. When data input/output is completed for a full-page of data (256), it automatically returns to the start address, and input/output is performed repeatedly.

•**Column address strobe and read command [READ]:** This command starts a read operation. In addition, the start address of burst read is determined by the column address (AY0-AY7) and the bank select address (BS). After the read operation, the output buffer becomes High-Z.

•**Read with auto-precharge [READ A]:** This command automatically performs a precharge operation after a burst read with a burst length of 1, 2, 4, or 8. When the burst length is full-page(256), this command is illegal.

•**Column address strobe and write command [WRIT]:** This command starts a write operation. When the burst write mode is selected, the column address (AY0 to AY7) and the bank select address (A9) become the burst write start address. When the single write mode is selected, data is only written to the location specified by the column address (AY0 to AY7) and the bank select address (A9).

•**Write with auto-precharge [WRIT A]:** This command automatically performs a precharge operation after a burst write with a length of 1, 2, 4, or 8, or after a single write operation. When the burst length is full-page(256), this command is illegal.

•**Row address strobe and bank activate [ACTV]:** This command activates the bank that is selected by A9(BS) and determines the row address (AX0-AX8). When A9 is Low, bank 0 is activated. When A9 is High, bank 1 is activated.

•**Precharge selected bank [PRE]:** This command starts precharge operation for the bank selected by A9. If A9 is Low, bank 0 is selected. If A9 is High, bank 1 is selected.

•**Precharge all banks [PALL]:** This command starts a precharge operation for all banks.

•**Refresh [REF/SELF]:** This command starts the refresh operation. There are two types of refresh operation, the one is auto-refresh, and the other is self-refresh. For details, refer to the CKE truth table section.

•**Mode register set [MRS]:** Synchronous DRAM has a mode register that defines how it operates. The mode register is specified by the address pins (A0-A9) at the mode register set cycle. For details, refer to the mode register configuration. After power on, the contents of the mode register are undefined, execute the mode register set command to set up the mode register.

DQM Truth Table

Function	Symbol	CKE n - 1	CKE n	DQM U	DQM L
Upper byte write enable/output enable	ENBU	H	X	L	X
Lower byte write enable/output enable	ENBL	H	X	X	L
Upper byte write inhibit/output disable	MASKU	H	X	H	X
Lower byte write inhibit/output disable	MASKL	H	X	X	H

Note: H: V_{IH}. L: V_{IL}. X: V_{IH} or V_{IL}.

The HM5241605 series can mask input/output data by means of DQMU and DQML. DQMU masks the upper byte and DQML masks the lower byte. During reading, the output buffer is set to Low-Z by setting DQMU/DQML to Low, enabling data output. On the other hand, when DQMU/DQML is set to High, the output buffer becomes High-Z, disabling data output.

During writing, data is written by setting DQMU/DQML to Low. When DQMU/DQML is set to High, the previous data is held (the new data is not written). Desired data can be masked during burst read or burst write by setting DQMU/DQML. For details, refer to the DQM control section of the HM5241605 operating instructions.

CKE Truth Table

Current state	Function		CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address
Active	Clock suspend mode entry		H	L	X	X	X	X	X
Any	Clock suspend		L	L	X	X	X	X	X
Clock suspend	Clock suspend mode exit		L	H	X	X	X	X	X
Idle	Auto-refresh command	REF	H	H	L	L	L	H	X
Idle	Self-refresh entry	SELF	H	L	L	L	L	H	X
Idle	Power down entry		H	L	L	H	H	H	X
			H	L	H	X	X	X	X
Self refresh	Self refresh exit		L	H	L	H	H	H	X
			L	H	H	X	X	X	X
Power down	Power down exit		L	H	L	H	H	H	X
			L	H	H	X	X	X	X

Note: H: V_{IH}. L: V_{IL}. X: V_{IH} or V_{IL}.

•**Clock suspend mode entry:** The synchronous DRAM enters clock suspend mode from active mode by setting CKE to Low. The clock suspend mode changes depending on the current status (1 clock before) as shown below.

•**ACTIVE clock suspend:** This suspend mode ignores inputs after the next clock by internally maintaining the bank active status.

•**READ suspend and READ A suspend:** The data being output is held (and continues to be output).

•**WRITE suspend and WRIT A suspend:** In this mode, external signals are not accepted. However, the internal state is held.

•**Clock suspend:** During clock suspend mode, keep the CKL to Low.

•**Clock suspend mode exit:** The synchronous DRAM exits from clock suspend mode by setting CKE to High during the clock suspend state.

•**IDLE:** In this state, all banks are not selected, and completed precharge operation.

•**Auto-refresh command [REF]:** When this command is input from the IDLE state, the synchronous DRAM starts auto-refresh operation. (The auto-refresh is the same as the CBR refresh of conventional DRAMs.) During the auto-refresh operation, refresh address and bank select address are generated inside the synchronous DRAM. For every auto-refresh cycle, the internal address counter is updated. Accordingly, 1,024 times are required to refresh the entire memory. Before executing the auto-refresh command, all the banks must be in the IDLE state. In addition, since the precharge for all banks is automatically performed after auto-refresh, no precharge command is required after auto-refresh.

•**Self-refresh entry [SELF]:** When this command is input during the IDLE state, the synchronous DRAM starts self-refresh operation. After the execution of this command, self-refresh continues while CKE is Low. Since self-refresh is performed internally and automatically, external refresh operations are unnecessary.

•**Power down mode entry:** When this command is executed during the IDLE state, the synchronous DRAM enters power down mode. In power down mode, power consumption is suppressed by cutting off the initial input circuit.

•**Self-refresh exit:** When this command is executed during self-refresh mode, the synchronous DRAM can exit from self-refresh mode. After exiting from self-refresh mode, the synchronous DRAM enters the IDLE state.

•**Power down exit:** When this command is executed at the power down mode, the synchronous DRAM can exit from power down mode. After exiting from power down mode, the synchronous DRAM enters the IDLE state.

Function Truth Table

The following table shows the operations that are performed when each command is issued in each mode of the synchronous DRAM.

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Precharge	H	X	X	X	X	DESL	Enter IDLE after t_{RP}
	L	H	H	H	X	NOP	Enter IDLE after t_{RP}
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, A8	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A8	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	ILLEGAL
	L	L	H	L	BA, A8	PRE, PALL	ILLEGAL
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Idle	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	BST	NOP
	L	H	L	H	BA, CA, A8	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A8	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	Bank and row active
	L	L	H	L	BA, A8	PRE, PALL	NOP
	L	L	L	H	X	REF, SELF	Refresh
	L	L	L	L	MODE	MRS	Mode register set

Function Truth Table (cont.)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Row active	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	BST	NOP
	L	H	L	H	BA, CA, A8	READ/READ A	Begin read
	L	H	L	L	BA, CA, A8	WRIT/WRIT A	Begin write
	L	L	H	H	BA, RA	ACTV	Other bank active*3 ILLEGAL on same bank
	L	L	H	L	BA, A8	PRE, PALL	Precharge
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Read	H	X	X	X	X	DESL	Continue burst to end
	L	H	H	H	X	NOP	Continue burst to end
	L	H	H	L	X	BST	Burst stop to full page
	L	H	L	H	BA, CA, A8	READ/READ A	Continue burst read to $\overline{CAS}$ latency and New read
	L	H	L	L	BA, CA, A8	WRIT/WRIT A	Term burst read/start write
	L	L	H	H	BA, RA	ACTV	Other bank active*3 ILLEGAL on same bank
	L	L	H	L	BA, A8	PRE, PALL	Term burst read and Precharge
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

Function Truth Table (cont.)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Read with auto-precharge	H	X	X	X	X	DESL	Continue burst to end and precharge
	L	H	H	H	X	NOP	Continue burst to end and precharge
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, A8	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A8	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	Other bank active*3 ILLEGAL on same bank
	L	L	H	L	BA, A8	PRE, PALL	ILLEGAL
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Write	H	X	X	X	X	DESL	Continue burst to end
	L	H	H	H	X	NOP	Continue burst to end
	L	H	H	L	X	BST	Burst stop on full page
	L	H	L	H	BA, CA, A8	READ/READ A	Term burst and New read
	L	H	L	L	BA, CA, A8	WRIT/WRIT A	Term burst and New write
	L	L	H	H	BA, RA	ACTV	Other bank active*3 ILLEGAL on same bank
	L	L	H	L	BA, A8	PRE, PALL	Term burst write and Precharge*2
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

Function Truth Table (cont.)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Write with auto-precharge	H	X	X	X	X	DESL	Continue burst to end and precharge
	L	H	H	H	X	NOP	Continue burst to end and precharge
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, A8	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A8	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	Other bank active*3 ILLEGAL on same bank
	L	L	H	L	BA, A8	PRE, PALL	ILLEGAL
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Refresh (auto-refresh)	H	X	X	X	X	DESL	Enter IDLE after t_{RC}
	L	H	H	H	X	NOP	Enter IDLE after t_{RC}
	L	H	H	L	X	BST	Enter IDLE after t_{RC}
	L	H	L	H	BA, CA, A8	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A8	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	ILLEGAL
	L	L	H	L	BA, A8	PRE, PALL	ILLEGAL
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

Note 1. H: V_{IH}. L: V_{IL}. X: V_{IH} or V_{IL}.
The other combinations are inhibit.
2. An interval of t_{RWL} is required between the final valid data input and the precharge command.
3. If t_{RRD} is not satisfied, this operation is illegal.

From [PRECHARGE]

To [DESL], [NOP] or [BST]: When these commands are executed, the synchronous DRAM enters the IDLE state after t_{RP} has elapsed from the completion of precharge.

From [IDLE]

To [DESL], [NOP], [BST], [PRE] or [PALL]: These commands result in no operation.

To [ACTV]: The bank specified by the address pins and the ROW address is activated.

To [REF], [SELF]: The synchronous DRAM enters refresh mode (auto-refresh or self-refresh).

To [MRS]: The synchronous DRAM enters the mode register set cycle.

From [ROW ACTIVE]

To [DESL], [NOP] or [BST]: These commands result in no operation.

To [READ], [READ A]: A read operation starts. (However, an interval of t_{RCD} is required.)

To [WRIT], [WRIT A]: A write operation starts. (However, an interval of t_{RCD} is required.)

To [ACTV]: This command makes the other bank active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

To [PRE], [PALL]: These commands set the synchronous DRAM to precharge mode. (However, an interval of t_{RAS} is required.)

From [READ]

To [DESL], [NOP]: These commands continue read operations until the burst operation is completed.

To [BST]: This command stops a full-page burst.

To [READ], [READ A]: Data output by the previous read command continues to be output. After $\overline{CAS}$ latency, the data output resulting from the next command will start.

To [WRIT], [WRIT A]: These commands stop a burst read, and start a write cycle.

To [ACTV]: This command makes other banks bank active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

To [PRE], [PALL]: These commands stop a burst read, and the synchronous DRAM enters precharge mode.

From [READ with AUTO-PRECHARGE]

To [DESL], [NOP]: These commands continue read operations until the burst operation is completed, and the synchronous DRAM then enters precharge mode.

To [ACTV]: This command makes other banks bank active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

From [WRITE]

To [DESL], [NOP]: These commands continue write operations until the burst operation is completed.

To [BST]: This command stops a full-page burst.

To [READ], [READ A]: These commands stop a burst and start a read cycle.

To [WRIT], [WRIT A]: These commands stop a burst and start the next write cycle.

To [ACTV]: This command makes the other bank active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

To [PRE], [PALL]: These commands stop burst write and the synchronous DRAM then enters precharge mode.

From [WRITE with AUTO-PRECHARGE]

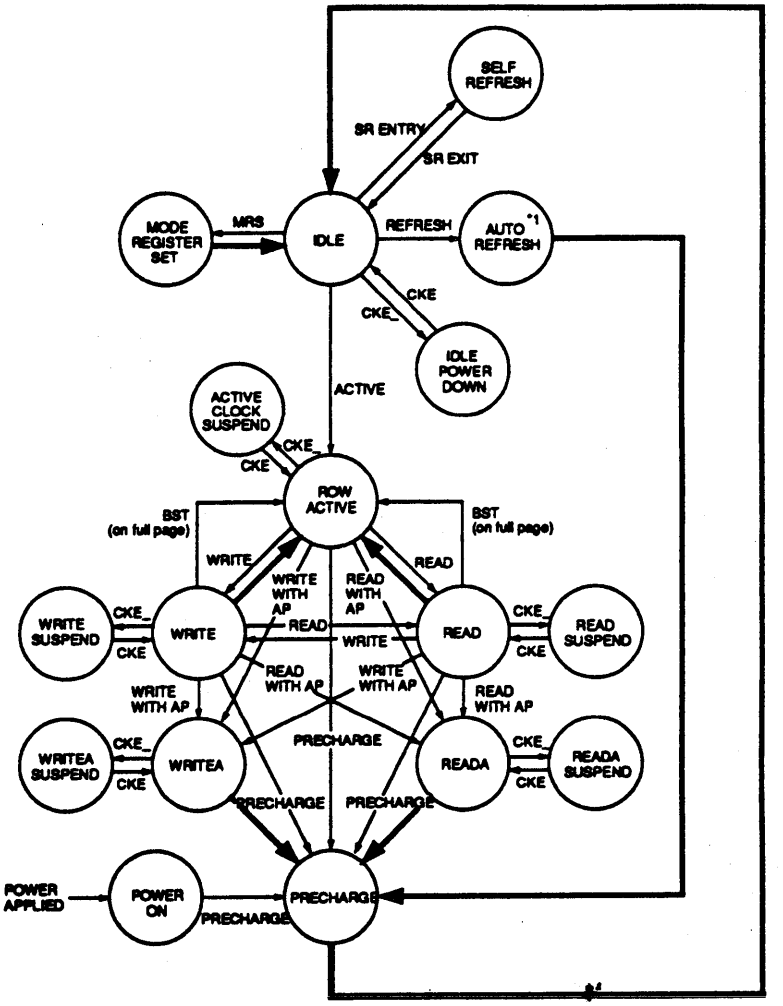
To [DESL], [NOP]: These commands continue write operations until the burst is completed, and the synchronous DRAM enters precharge mode.

To [ACTV]: This command makes the other bank activ. (However, an interval of t_{RC} is required.) Attempting to make the currently active bank active results in an illegal command.

From [REFRESH]

To [DESL], [NOP], [BST]: After an auto-refresh cycle (after t_{RC}), the synchronous DRAM automatically enters the IDLE state.

Simplified State Diagram



Automatic transition after completion of command.
Transition resulting from command input.

Note: 1. After the auto-refresh operation, precharge operation is performed automatically and enter the IDLE state.

Mode Register Configuration

The mode register is set by the input to the address pins (A0 to A9) during mode register set cycles. The mode register consists of five sections, each of which is assigned to address pins.

•A9 and A8: (OPCODE)
The synchronous DRAM has two types of write modes. One is the burst write mode, and the other is the single write mode. These bits specify write mode.

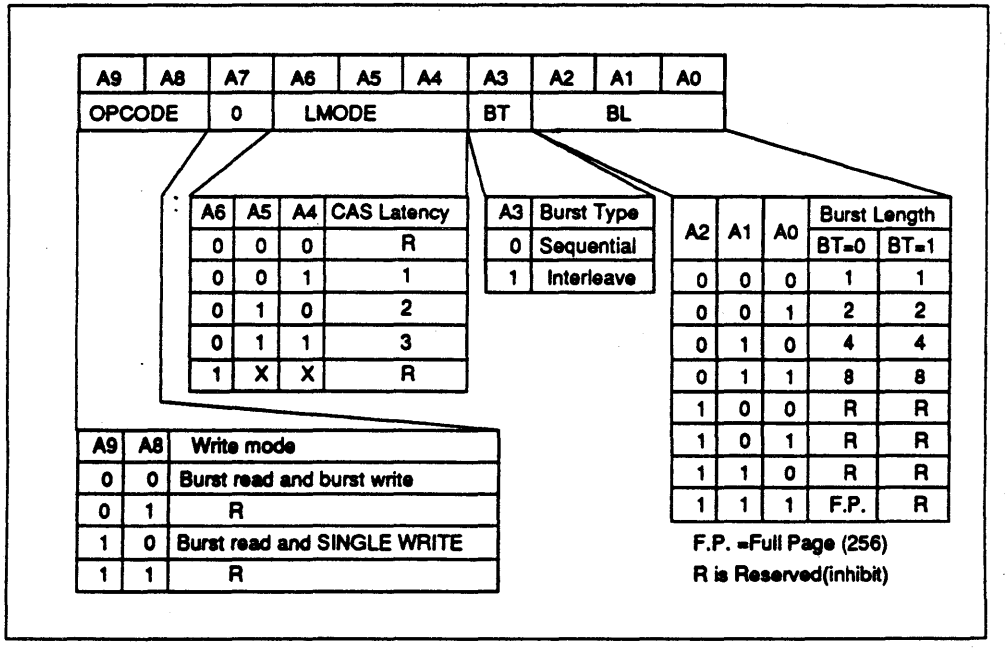
•Burst read and BURST WRITE
Burst write is performed for the specified burst length starting from the column address specified in the write cycle.
•Burst read and SINGLE WRITE
Data is only written to the column address specified during the write cycle, regardless of the burst length.

•A7
Keep this bit Low at the mode register set cycle.

•A6, A5, A4: (LMODE)
These pins specify the $\overline{CAS}$ latency.

•A3: (BT)
A burst type is specified. When full-page burst is performed, only "sequential" can be selected.

•A2, A1, A0: (BL)
These pins specify the burst length.



Burst Sequence

Burst length = 2

Stating Ad.	Addressing(decimal)	
A0	Sequence	Interleave
0	0, 1,	0, 1,
1	1, 0,	1, 0,

Burst length = 4

Stating Ad.		Addressing(decimal)	
A1	A0	Sequence	Interleave
0	0	0, 1, 2, 3,	0, 1, 2, 3,
0	1	1, 2, 3, 0,	1, 0, 3, 2,
1	0	2, 3, 0, 1,	2, 3, 0, 1,
1	1	3, 0, 1, 2,	3, 2, 1, 0,

Burst length = 8

Stating Ad.			Addressing(decimal)	
A2	A1	A0	Sequence	Interleave
0	0	0	0, 1, 2, 3, 4, 5, 6, 7,	0, 1, 2, 3, 4, 5, 6, 7,
0	0	1	1, 2, 3, 4, 5, 6, 7, 0,	1, 0, 3, 2, 5, 4, 7, 6,
0	1	0	2, 3, 4, 5, 6, 7, 0, 1,	2, 3, 0, 1, 6, 7, 4, 5,
0	1	1	3, 4, 5, 6, 7, 0, 1, 2,	3, 2, 1, 0, 7, 6, 5, 4,
1	0	0	4, 5, 6, 7, 0, 1, 2, 3,	4, 5, 6, 7, 0, 1, 2, 3,
1	0	1	5, 6, 7, 0, 1, 2, 3, 4,	5, 4, 7, 6, 1, 0, 3, 2,
1	1	0	6, 7, 0, 1, 2, 3, 4, 5,	6, 7, 4, 5, 2, 3, 0, 1,
1	1	1	7, 0, 1, 2, 3, 4, 5, 6,	7, 6, 5, 4, 3, 2, 1, 0,

Operation of HM5241605 Series

Read/Write Operations

•Bank active

Before executing a read or write operation, the corresponding bank and the row address must be activated by the bank active (ACTV) command. Either bank 0 or bank 1 is activated according to the status of the A9 pin, and the row address (AX0 to AX8) is activated by the A0 to A8 pins at the bank active command cycle. An interval of t_{RCD} is required between the bank active command input and the following read/write command input.

•Read operation

A read operation starts when a read command is input. Output buffer becomes Low-Z in the ($\overline{CAS}$ Latency - 1) cycle after read command set. HM5241605 series can perform a burst read operation.

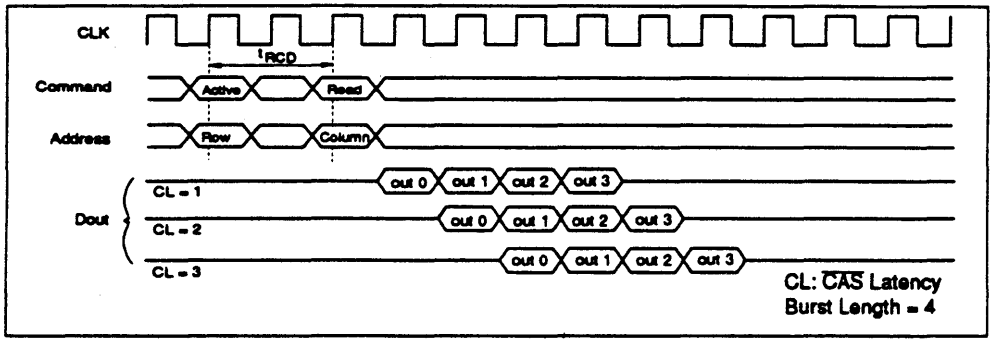
The burst length can be set to 1,2,4,8 or full-page(256). The start address for a burst read is specified by the column address (AY0 to AY7) and the bank select address (A9) at the read command set cycle. In a read operation, data output starts after the number of cycles specified by the $\overline{CAS}$ Latency. The $\overline{CAS}$ Latency can be set to 1,2,3.

When the burst length is 1, 2, 4, or 8, the Dout buffer automatically becomes High-Z at the next cycle after the successive burst-length data has been output.

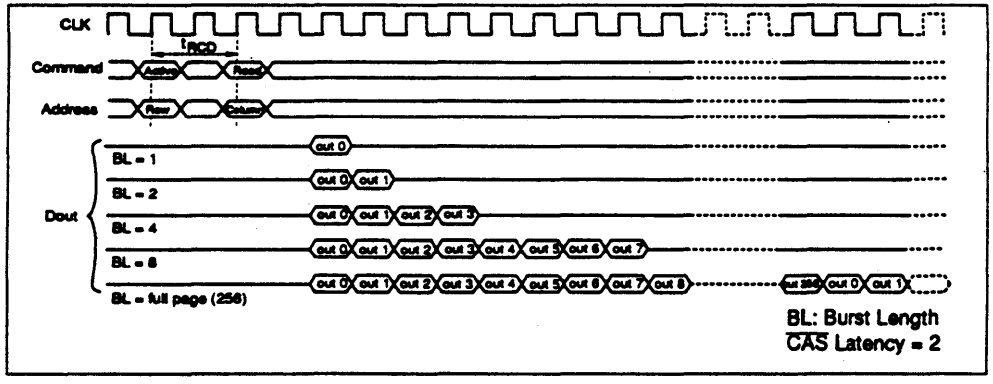
When the burst length is full-page(256), data is repeatedly output until the burst stop command is input.

The $\overline{CAS}$ latency and burst length must be specified at the mode register.

$\overline{CAS}$ Latency



Burst Length



Read/Write Operations (cont.)

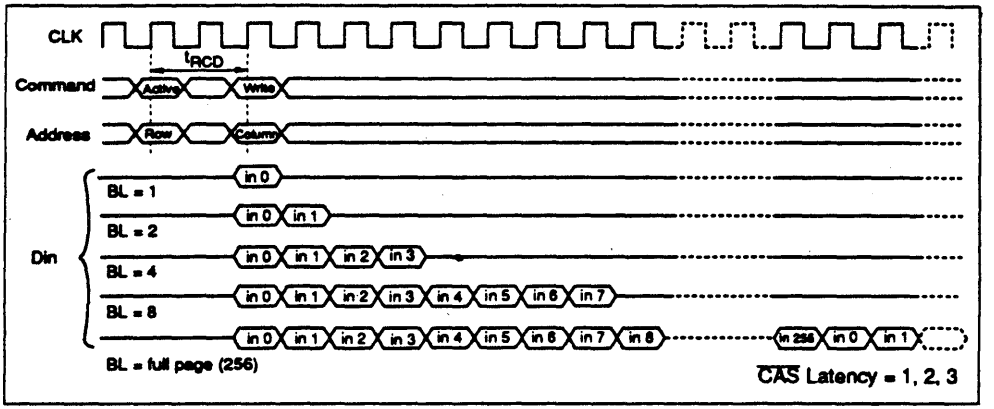
•Write operation

Burst write or single write mode is selected by the OPCODE (A9, A8) of the mode register.

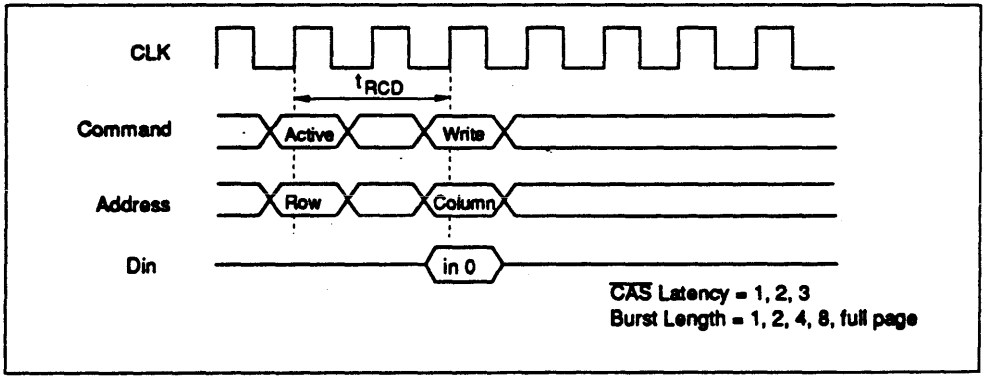
(1) Burst write: A burst write operation is enabled by setting OPCODE(A9, A8) to (0, 0). A burst write starts in the same cycle as a write command set. (The latency of data input is 0.) The burst length can be set to 1, 2, 4, 8, and full-page, like burst read operations. The write start address is specified by the column address (AY0 to AY7) and the bank select address (A9) at the write command set cycle.

(2) Single write: A single write operation is enabled by setting OPCODE(A9, A8) to (1, 0). In a single write operation, data is only written to the column address (AY0 to AY7) and the bank select address (A9) specified by the write command set cycle without regard to the burst length setting. (The latency of data input is 0).

Burst Write



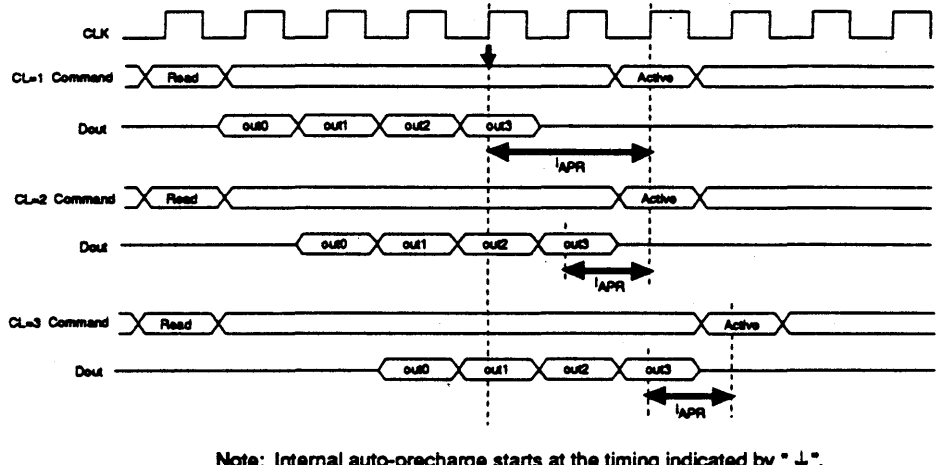
Single Write



Read/Write Operations (cont.)

•**Read with auto-precharge**: In this operation, since precharge is automatically performed after completing a read operation, a precharge command need not be executed after each read operation. The command executed for the same bank after the execution of this command must be the bank active (ACTV) command. In addition, an interval defined by t_{APR} is required before execution of the next command.

$\overline{CAS}$ latency	Precharge start cycle
3	2 cycle before the final data is output
2	1 cycle before the final data is output
1	same cycle as the final data is output



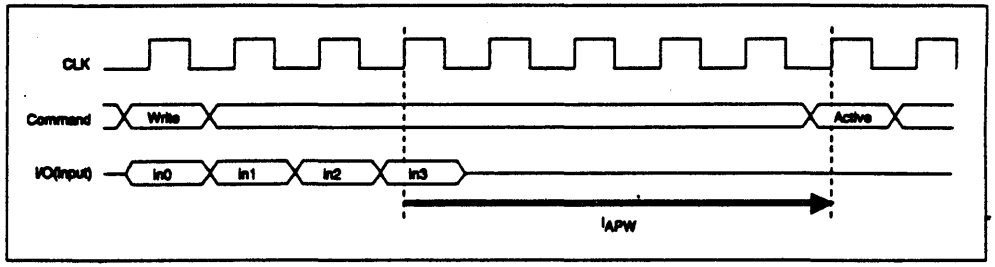
Note: Internal auto-precharge starts at the timing indicated by "↓".
At CLK = 33 MHz (t_{APR} changes depending on the operating frequency.

Read/Write Operations (cont.)

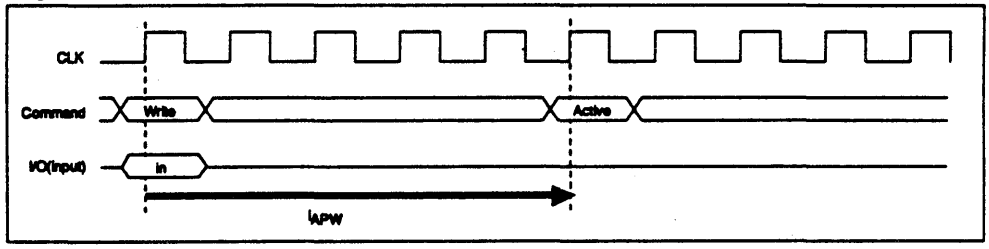
•**Write with auto-precharge:** In this operation, since precharge is automatically performed after completing a burst write or single write operation, a precharge command need not be executed after each write operation.

The command executed for the same bank after the execution of this command must be the bank active (ACTV) command. In addition, an interval of t_{APW} is required between the final valid data input and input of the next command.

Burst Write (Burst Length = 4)



Single Write



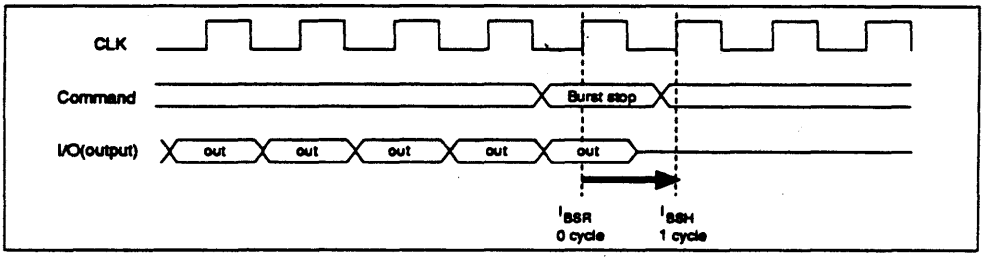
Full-page Burst Stop

•**Burst stop command during burst read:** The burst stop (BST) command is used to stop data output during a full-page burst. The BST command sets the output buffer to High-Z and stops the full-page burst read.

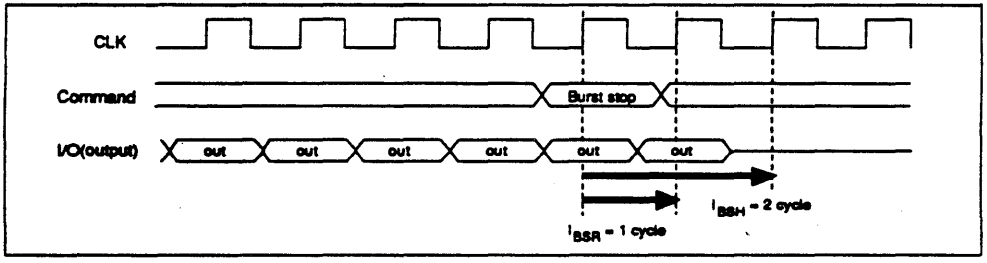
The timing from command input to the last data changes depending on the $\overline{CAS}$ latency setting. When the $\overline{CAS}$ latency is 3, the data becomes invalid two cycles after the BST command. In addition, the BST command is valid only during full-page burst mode, and is invalid with burst lengths of 1, 2, 4, and 8.

$\overline{CAS}$ latency	BST to valid data	BST to high impedance
1	0	1
2	1	2
3	1	3

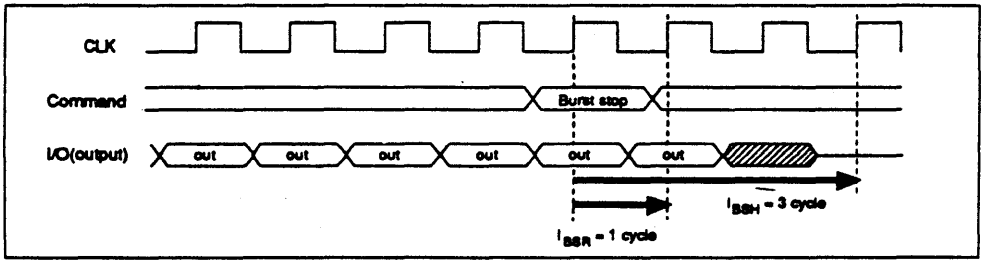
$\overline{CAS}$ Latency = 1, Burst Length = full page



$\overline{CAS}$ Latency = 2, Burst Length = full page



$\overline{CAS}$ Latency = 3, Burst Length = full page

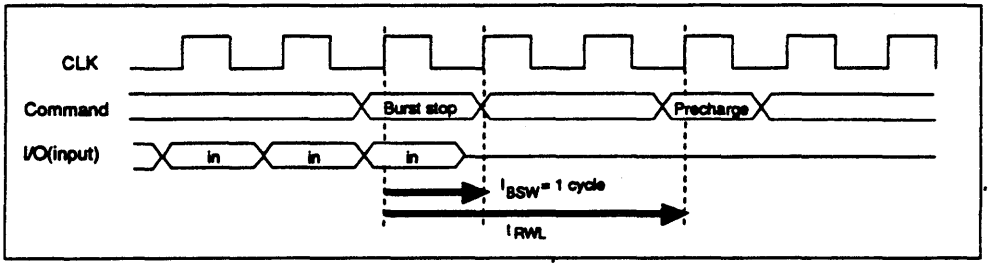


Full-page Burst Stop (cont.)

•**Burst stop command at burst write:** The burst stop command (BST command) is used to stop data input during a full-page burst write. Data is still written in the same cycle as the BST command, but no data is written in subsequent cycles.

In addition, the BST command is only valid during full-page burst mode, and is invalid with burst lengths of 1, 2, 4, and 8. And an interval of t_{RWL} is required between the BST command and the next precharge command.

Burst Length = full page

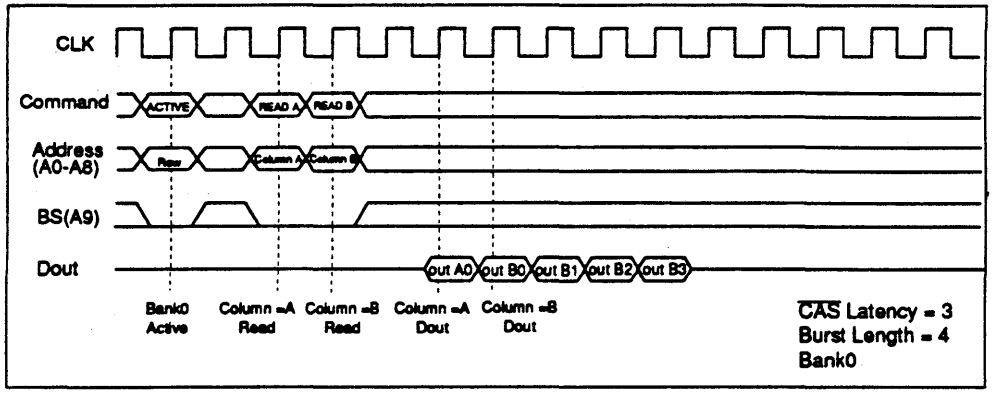


Command Intervals

•Read command to Read command interval

(1) Same bank, same ROW address: When another read command is executed at the same ROW address of the same bank as the preceding read command execution, the second read can be performed after an interval of no less than 1 cycle. Even when the first command is a burst read that is not yet finished, the data read by the second command will be valid.

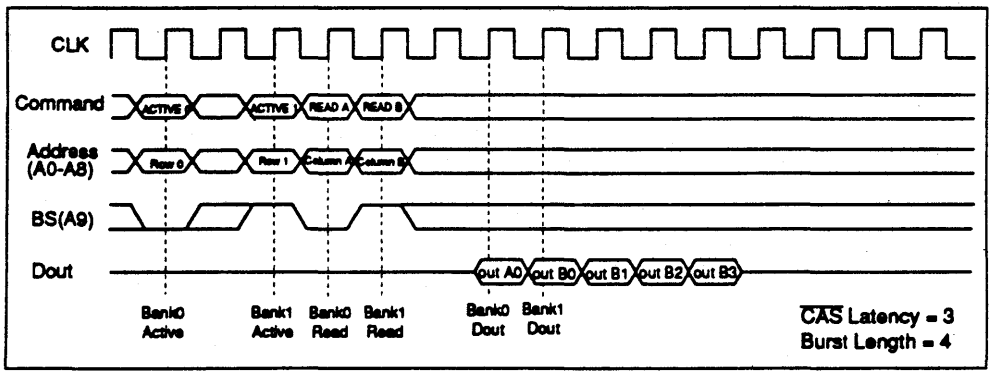
READ to READ Command Interval (same ROW address in same bank)



(2) Same bank, different ROW address: When the ROW address changes on same bank, consecutive read commands cannot be executed; it is necessary to separate the two read commands with a precharge command and a bank-active command.

(3) Different bank: When the bank changes, the second read can be performed after an interval of no less than 1 cycle, provided that the other bank is in the bank-active state. Even when the first command is a burst read that is not yet finished, the data read by the second command will be valid.

READ to READ Command Interval (different bank)

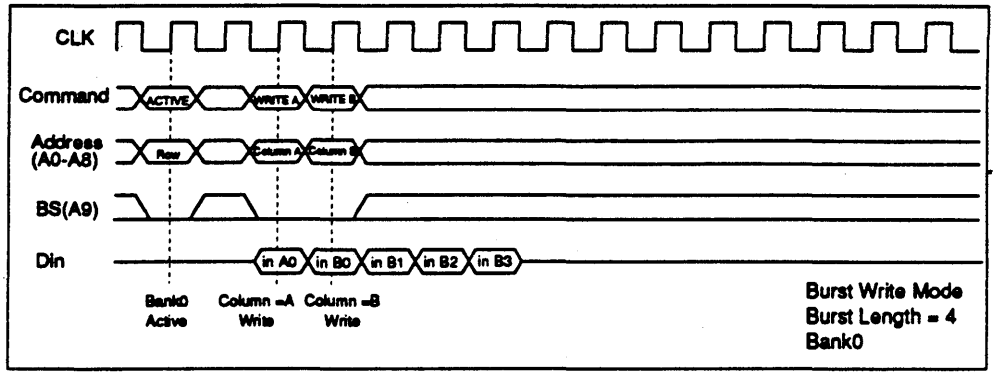


Command Intervals (cont.)

•Write command to Write command interval

(1) Same bank, same ROW address: When another write command is executed at the same ROW address of the same bank as the preceding write command, the second write can be performed after an interval of no less than 1 cycle. In the case of burst writes, the second write command has priority.

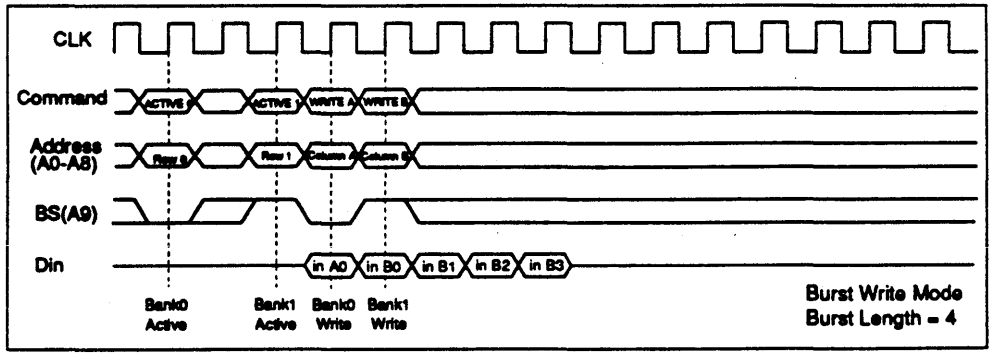
WRITE to WRITE Command Interval (same ROW address in same bank)



(2) Same bank, different ROW address: When the ROW address changes, consecutive write commands cannot be executed; it is necessary to separate the two write commands with a precharge command and a bank-active command.

(3) Different bank: When the bank changes, the second write can be performed after an interval of no less than 1 cycle, provided that the other bank is in the bank-active state. In the case of burst write, the second write command has priority.

WRITE to WRITE Command Interval (different bank)

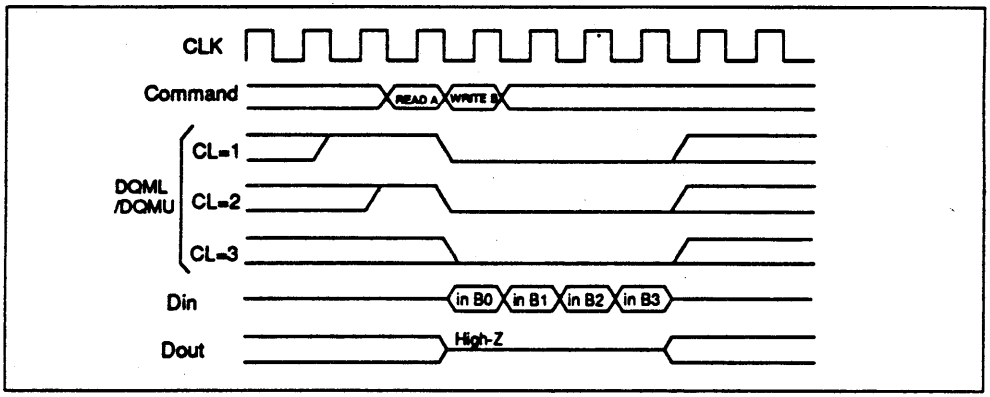


Command Intervals (cont.)

•Read command to Write command interval

(1) Same bank, same ROW address: When the write command is executed at the same ROW address of the same bank as the preceding read command, the write command can be performed after an interval of no less than 1 cycle. However, DQML/DQMU must be set High so that the output buffer becomes High-Z before data input.

READ to WRITE Command Interval



(2) Same bank, different ROW address: When the ROW address changes, consecutive write commands cannot be executed; it is necessary to separate the two write commands with a precharge command or a bank-active command.

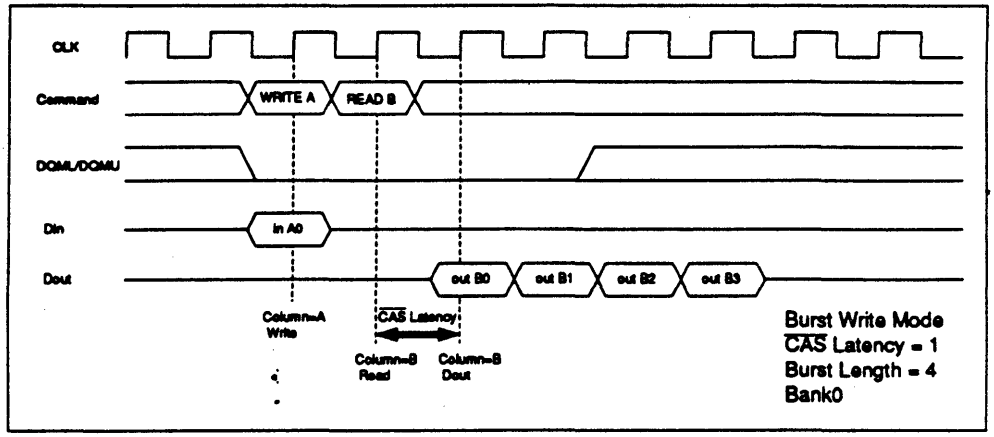
(3) Different bank: When the bank changes, the write command can be performed after an interval of no less than 1 cycle, provided that the other bank is in the bank-active state. However, DQML/DQMU must be set High so that the output buffer becomes High-Z before data input.

Command Intervals (cont.)

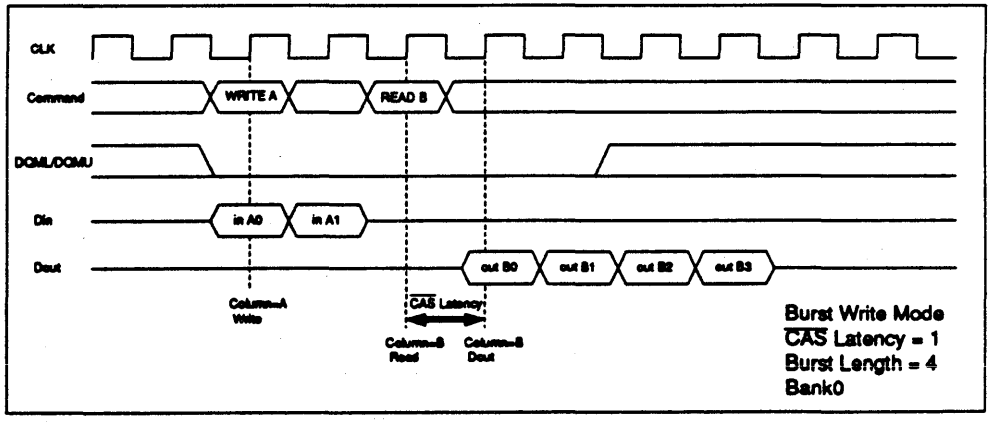
•Write command to Read command interval

(1) Same bank, same ROW address: When the read command is executed at the same ROW address of the same bank as the preceding write command, the write command can be performed after an interval of no less than 1 cycle. However, in the case of a burst write, data will continue to be written until one cycle before the read command is executed.

WRITE to READ Command Interval (1)



WRITE to READ Command Interval (2)



(2) Same bank, different ROW address: When the ROW address changes, consecutive write commands cannot be executed; it is necessary to separate the two write commands with a precharge command and a bank-active command.

(3) Different bank: When the bank changes, the write command can be performed after an interval of no less than 1 cycle, provided that the other bank is in the bank-active state. However, in the case of a burst write, data will continue to be written until one cycle before the read command is executed (as in the case of the same bank and the same address).

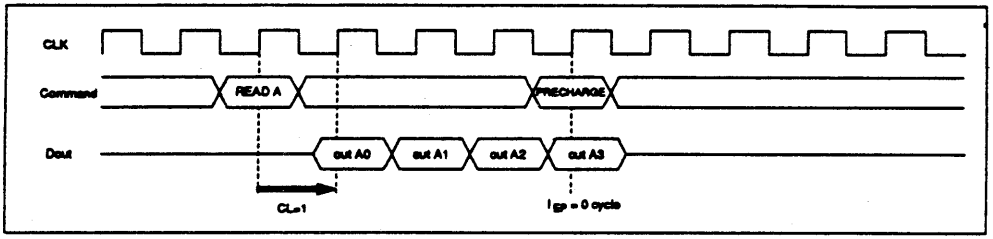
Command Intervals (cont.)

•Read command to Precharge command interval (same bank): When the precharge command is executed for the same bank as the read command that preceded it, the minimum interval between the two commands is one cycle. However, since the output buffer then becomes High-Z after the cycles defined by l_{HZP}, there is a possibility that burst read data output will be interrupted, if the precharge command is input during burst read.

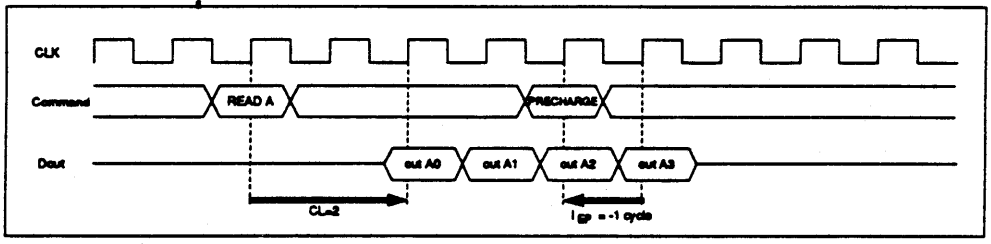
To read all data by burst read, the cycles defined by l_{EP} must be assured as an interval from the final data output to precharge command execution.

READ to PRECHARGE Command Interval (same bank): To output all data

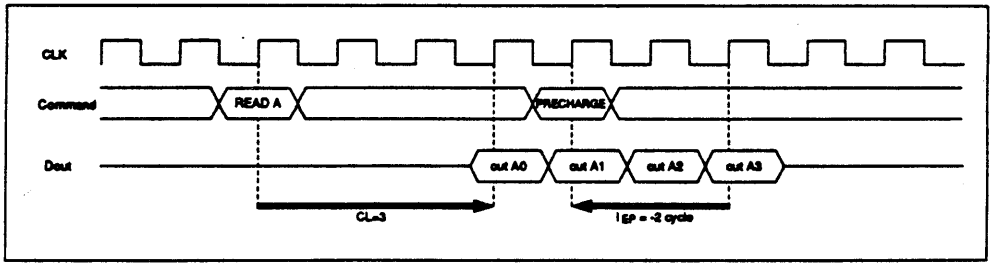
$\overline{CAS}$ Latency = 1, Burst Length = 4



$\overline{CAS}$ Latency = 2, Burst Length = 4



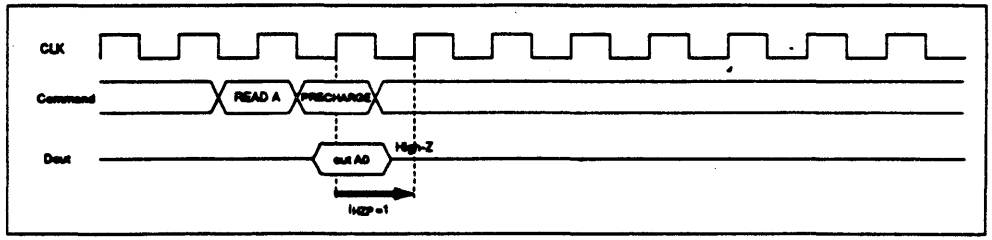
$\overline{CAS}$ Latency = 3, Burst Length = 4



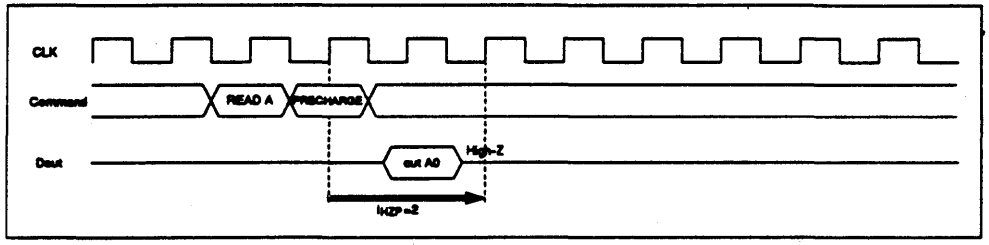
Command Intervals (cont.)

READ to PRECHARGE Command Interval (same bank): To stop output data

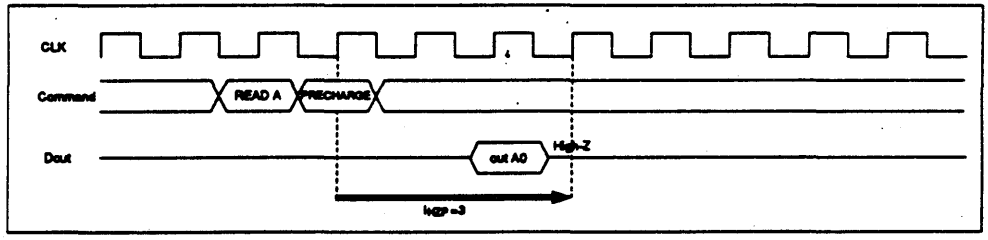
$\overline{CAS}$ Latency = 1, Burst Length = 1, 2, 4, 8



$\overline{CAS}$ Latency = 2, Burst Length = 1, 2, 4, 8



$\overline{CAS}$ Latency = 3, Burst Length = 1, 2, 4, 8

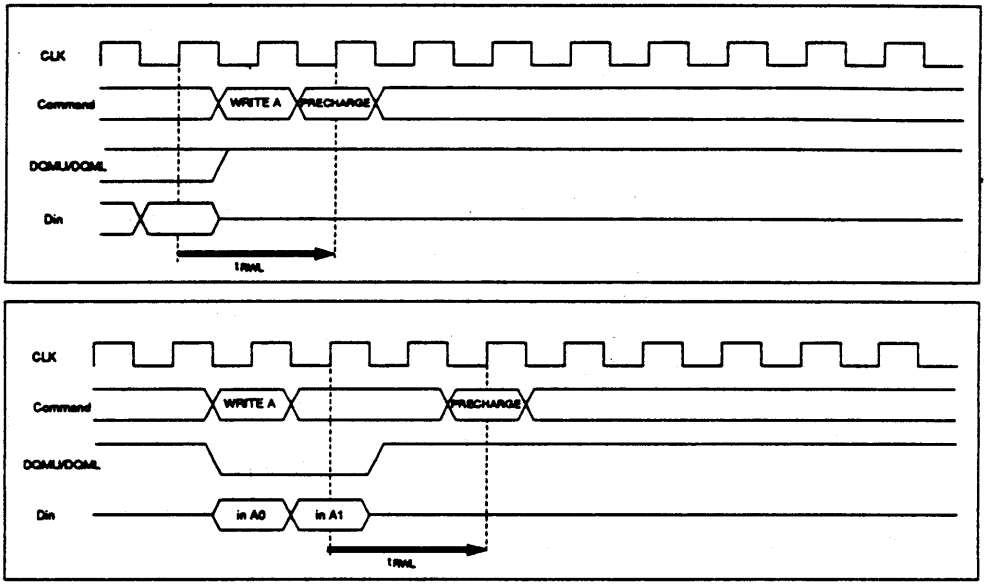


Command Intervals (cont.)

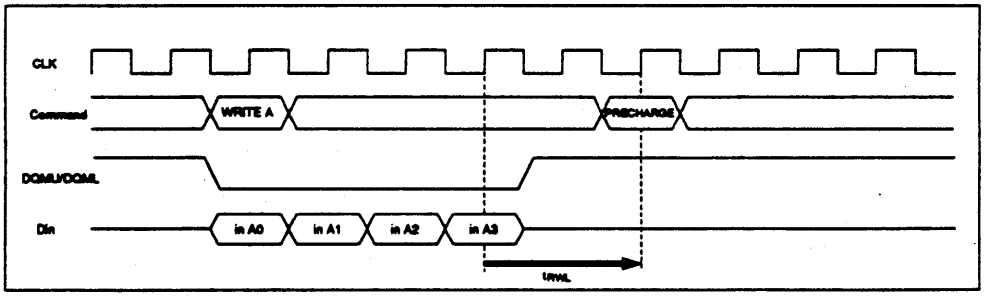
•Write command to Precharge command interval (same bank): When the precharge command is executed for the same bank as the write command that preceded it, the minimum interval between the two commands is 1 cycle. However, if the burst write operation is unfinished, the input data must be masked by means of DQMU and DQML for assurance of the cycle defined by t_{RWL}.

WRITE to PRECHARGE Command Interval (same bank)

Burst Length = 4 (To stop write operation)



Burst Length = 4 (To write all data)



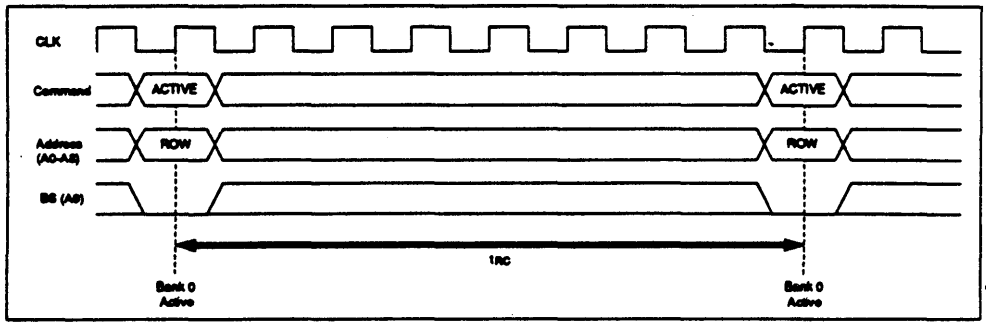
Command Intervals (cont.)

•Bank active command interval

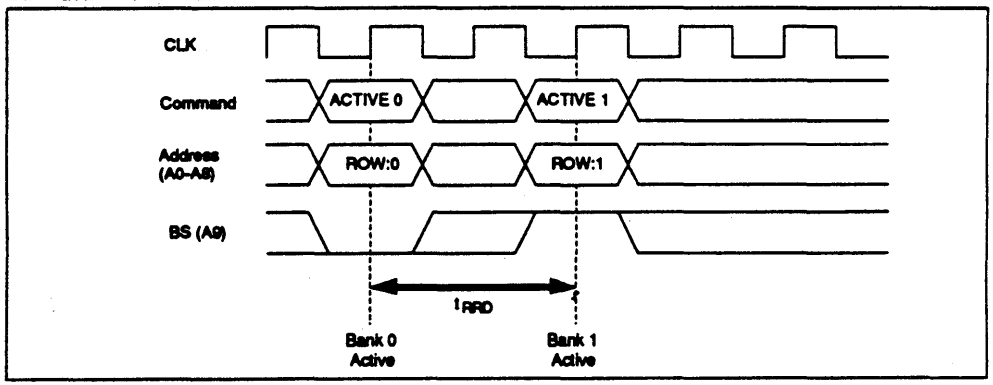
(1) Same bank: The interval between the two bank-active commands must be no less than t_{RC}.

(2) In the case of different bank-active commands: The interval between the two bank-active commands must be no less than t_{RRD}.

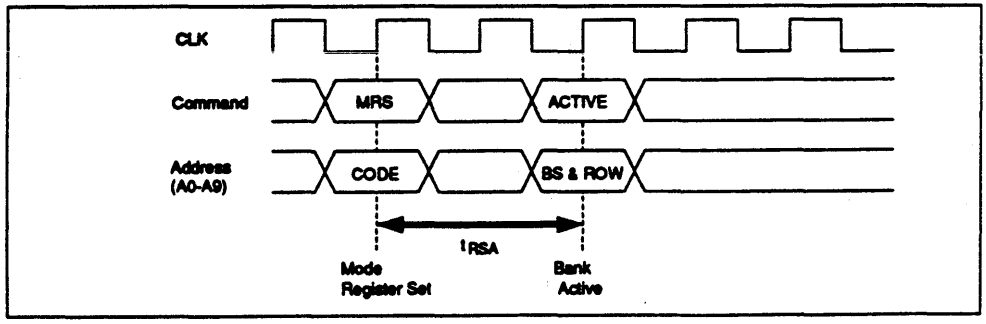
Bank active to bank active for same bank



Bank active to bank active for different bank



•Mode register set to Bank-active command interval: The interval between setting the mode register and executing a bank-active command must be no less than t_{RSA}.



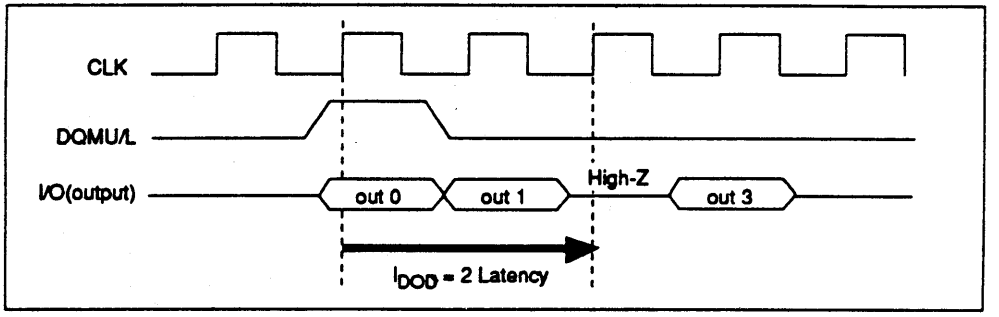
DQM Control

The DQML and DQMU mask the lower and upper bytes of the I/O data, respectively. The timing of DQML/DQMU is different during reading and writing.

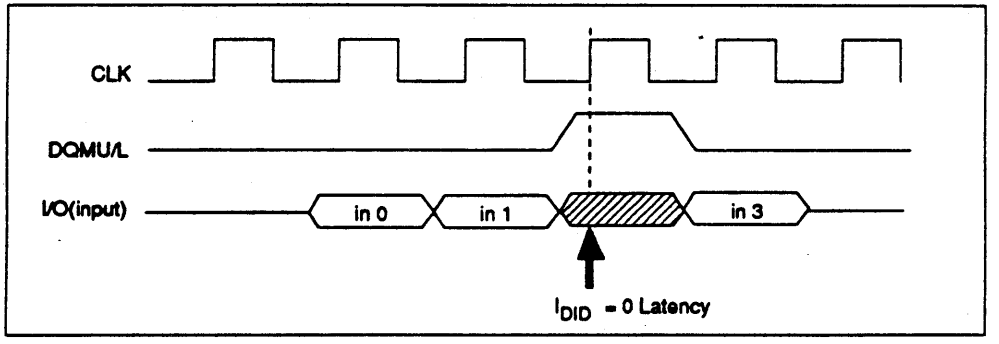
•**Reading:** When data is read, the output buffer can be controlled by DQML/DQMU.
By setting DQML/DQMU to Low, the output buffer becomes Low-Z, enabling data output. By setting DQML/DQMU to High, the output buffer becomes High-Z, and the corresponding data is not output. However, internal reading operations continue. The latency of DQML/DQMU during reading is 2.

•**Writing:** Input data can be masked by DQML/DQMU. By setting DQML/DQMU to Low, data can be written. In addition, when DQML/DQMU is set to High, the corresponding data is not written, and the previous data is held. The latency of DQML/DQMU during writing is 0.

Reading



Writing



Refresh

•Auto-refresh

All the banks must be precharged before executing an auto-refresh command. Since the auto-refresh command updates the interval counter every time it is executed and determines the banks and the ROW addresses to be refreshed, external address specification is not required. The refresh cycle is 1,024 cycles/16 ms. (1,024 cycles are required to refresh all the ROW addresses.) The output buffer becomes High-Z after auto-refresh start. In addition, since a precharge has been completed by an internal operation after the auto-refresh, an additional precharge operation by the precharge command is not required.

•Self-refresh

After executing a self-refresh command, the self-refresh operation continues while CKE is held Low. During self-refresh operation, all ROW addresses are refreshed by the internal refresh timer. A self-refresh is terminated by a self-refresh exit command. After the self-refresh, since it is impossible to determine the address of the last ROW to be refreshed, an auto-refresh should immediately be performed for all addresses (1,024 cycles).

Others

•Power-down mode

The synchronous DRAM enters power-down mode when CKE goes Low in the IDLE state. In power down mode, power consumption is suppressed by deactivating the input initial circuit. Power down mode continues while CKE is held Low. In addition, by setting CKE to High, the synchronous DRAM exits from the power down mode, and command input is enabled from the next cycle. In this mode, internal refresh is not performed.

•Clock suspend mode

By driving CKE to Low during a bank-active or read/write operation, the synchronous DRAM enters clock suspend mode. During clock suspend mode, external input signals are ignored and the internal state is maintained. When CKE is driven High, the synchronous DRAM terminates clock suspend mode, and command input is enabled from the next cycle. For details, refer to the "CKE Truth Table".

•Power-up sequence

During power-up sequence, the DQML/DQMU and the CKE must be set to High. When 100 µs has past after power on, all banks must be precharged using the precharge command. After t_{RP} delay, set the mode register. And after t_{RSA} delay, execute two cycles of auto-refresh operation as dummy, an interval of t_{RC} is required between two auto-refresh commands.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−1.0 to +4.6	V
Supply voltage relative to V_{SS}	V_{CC}	−1.0 to +4.6	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage	V_{CC}, $V_{CC}Q$	3.0	3.6	V	1
	V_{SS}, $V_{SS}Q$	0	0	V	
Input high voltage	V_{IH}	2.0	4.6	V	1, 2
Input low voltage	V_{IL}	−0.3	0.8	V	1, 3

Notes: 1. All voltage referred to V_{SS}
2. V_{IH} (max) = 5.5 V for pulse width ≤ 5 ns
3. V_{IL} (min) = −1.0 V for pulse width ≤ 5 ns

DC Characteristics (Ta = 0 to 70°C, V_{CC}, $V_{CC}Q$ = 3.3 V ± 0.3 V, V_{SS}, $V_{SS}Q$ = 0 V)

		HM5241605								
		-15		-17		-20				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test conditions	Notes
Operating current	I_{CC1}	—	80	—	70	—	65	mA	Burst length=1 t_{RC} = min	1, 2
Standby current (Bank Disable)	I_{CC2}	—	3	—	3	—	3	mA	CKE=V_{IL}, t_{CK} = min	
		—	2	—	2	—	2	mA	CKE=V_{IL} CLK=V_{IL} or V_{IH} Fixed	
		—	25	—	22	—	20	mA	CKE=V_{IH}, NOP command t_{CK} = min	3
Active standby current (Bank active)	I_{CC3}	—	7	—	7	—	7	mA	CKE=V_{IL}, t_{CK} = min, I/O=High-Z	1, 2
		—	30	—	26	—	23	mA	CKE=V_{IH}, NOP command t_{CK} = min, I/O = High-Z	1, 2, 3
Burst operating current (CL=1)	I_{CC4}	—	55	—	50	—	45	mA	t_{CK} = min	1, 2
(CL=2)		—	100	—	90	—	80	mA		
(CL=3)		—	105	—	95	—	85	mA		
Refresh current	I_{CC5}	—	70	—	65	—	60	mA	t_{RC} = min	
Self refresh current	I_{CC6}	—	2	—	2	—	2	mA	$V_{IH} \geq V_{CC} - 0.2$ $V_{IL} \leq 0.2$ V	
Input leakage current	I_{LI}	−10	10	−10	10	−10	10	µA	$0 \leq V_{in} \leq V_{CC}$	
Output leakage current	I_{LO}	−10	10	−10	10	−10	10	µA	$0 \leq V_{out} \leq V_{CC}$ I/O = disable	
Output high voltage	V_{OH}	2.4	—	2.4	—	2.4	—	V	I_{OH} = −2 mA	
Output low voltage	V_{OL}	—	0.4	—	0.4	—	0.4	V	I_{OL} = 2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} (max) is specified at the output open condition.
2. One bank operation.
3. Input signal transition is once per two CLK cycles.

Capacitance (Ta = 25°C, V_{CC}, $V_{CC}Q$ = 3.3 V ± 0.3 V)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	5	pF	1, 3
Input capacitance (Signals)	C_{I2}	—	5	pF	1, 3
Output capacitance (I/O)	C_O	—	7	pF	1, 2, 3

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. DQMU/L = V_{IH} to disable Dout.
3. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to 70°C, V_{CC}, $V_{CC}Q$ = 3.3 V ± 0.3 V, V_{SS}, $V_{SS}Q$ = 0 V)

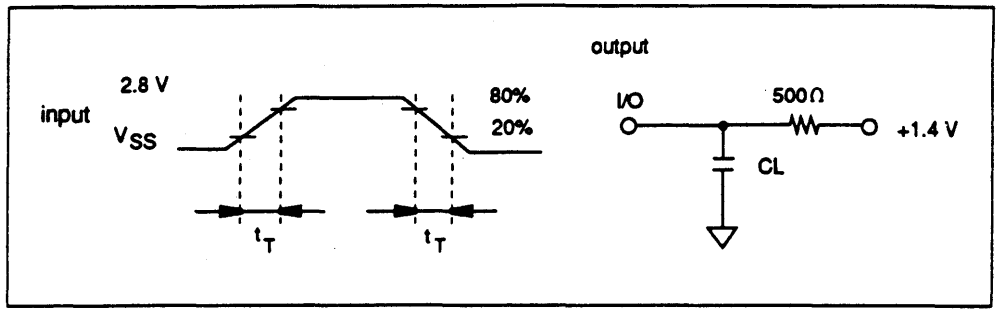
		HM5241605							
		-15		-17		-20			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
System clock (CL=1)	t_{CK}	30	—	35	—	40	—	ns	
cycle time (CL=2, 3)		15	—	17.5	—	20	—	ns	1
CLK high pulse width	t_{CKH}	6	—	7	—	8	—	ns	1
CLK low pulse width	t_{CKL}	6	—	7	—	8	—	ns	1
Access time (CL=1)	t_{AC}	—	30	—	34	—	38	ns	1, 2
from CLK (CL=2)		—	15	—	16.5	—	18	ns	1, 2
(CL=3)		—	13	—	15.5	—	18	ns	1, 2
Read command (CL=1, 2)	t_{ACK}	—	30	—	34	—	38	ns	1
to data valid time (CL=3)		—	43	—	50.5	—	58	ns	1
Data-out hold time (CL=1)	t_{OH}	4	—	4	—	4	—	ns	1, 2
(CL=2, 3)		2	—	2	—	2	—	ns	
CLK to Data-out low impedance	t_{LZ}	0	—	0	—	0	—	ns	1,2
CLK to Data-out (CL=1)	t_{HZ}	4	15	4	17	4	19	ns	
high impedance (CL=2, 3)		2	10	2	12	2	14	ns	1, 3
Data-in setup time	t_{DS}	4	—	4	—	4	—	ns	1
Data in hold time	t_{DH}	2	—	2	—	2	—	ns	1
Address setup time	t_{AS}	4	—	4	—	4	—	ns	1
Address hold time	t_{AH}	2	—	2	—	2	—	ns	1
CKE setup time	t_{CES}	4	—	4	—	4	—	ns	1

AC Characteristics (Ta = 0 to 70 °C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V)(cont.)

		HM5241605							
		-15		-17		-20			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
CKE setup time for power down exit	t_{CESP}	13	—	15	—	17	—	ns	1
CKE hold time	t_{CEH}	2	—	2	—	2	—	ns	1
Command($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{DQM}$) setup time	t_{CS}	4	—	4	—	4	—	ns	1
Command($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$,$\overline{DQM}$) hold time	t_{CH}	2	—	2	—	2	—	ns	1
Ref/Active to Ref/Active command period	t_{RC}	110	—	120	—	130	—	ns	1
Active to Precharge command period	t_{RAS}	70	10000	75	10000	80	10000	ns	1
Active to precharge on full page mode	t_{RASC}	—	80000	—	80000	—	80000	ns	1
Active command to column command (same bank)	t_{RCD}	30	—	35	—	40	—	ns	1
Precharge to active command period	t_{RP}	34	—	34	—	40	—	ns	1
The last data-in to Precharge lead time	t_{RWL}	30	—	35	—	40	—	ns	1
Active (a) to Active (b) command period	t_{RRD}	30	—	35	—	40	—	ns	1
Register set to active command	t_{RSA}	30	—	35	—	40	—	ns	1
Transition time (rise to fall)	t_T	1	5	1	5	1	5	ns	
Refresh period	t_{REF}	—	16	—	16	—	16	ms	

Notes: 1. AC measurement assumes t_T = 1 ns. Reference level for timing of input signals is 1.40 V.
2. Access time is measured at 1.40 V. Load condition is CL = 50 pF with current source.
3. t_{HZ} (max) defines the time at which the outputs achieves ± 200 mV.
Load condition is CL = 5 pF with current source.
4. t_{CES} define CKE setup time to CKE rising edge except power down exit command.

HM5241605 (LVTTL)



Relationship Between Frequency and Minimum Latency

Parameter	Symbol	HM5241605 -15		-17		-20		Notes
Frequency (MHz)		66	33	57	28.5	50	25	
t_{CK} (ns)		15	30	17.5	35	20	40	
Active command to column command (same bank)	t_{RCD}	2	1	2	1	2	1	
Active command to active command (same bank)	t_{RC}	8	5	7	4	7	4	= [t_{RAS} + t_{RP}]
Active command to precharge command (same bank)	t_{RAS}	5	3	5	3	4	2	
Precharge command to active command (same bank)	t_{RP}	3	2	2	1	2	1	
Last data input to precharge command (same bank)	t_{RWL}	2	1	2	1	2	1	
Active command to active command (different bank)	t_{RRD}	2	1	2	1	2	1	
Last data in to active command (Auto precharge, same bank)	l_{APW}	5	3	4	2	4	2	= [t_{RWL} + t_{RP}]
Self refresh exit to command input	l_{SEC}	8	4	7	4	7	4	= [t_{RC}]
Precharge command to high impedance	l_{HZP}							
($\overline{CAS}$ latency = 3)		3	3	3	3	3	3	
($\overline{CAS}$ latency = 2)		2	2	2	2	2	2	
($\overline{CAS}$ latency = 1)		—	1	—	1	—	1	
Last data out to active command	l_{APR}							
(auto precharge) ($\overline{CAS}$ latency = 2, 3)		2	1	1	0	1	0	= [t_{RP}] − 1
(same bank) ($\overline{CAS}$ latency = 1)		—	2	—	1	—	1	= [t_{RP}]
Last data out to precharge	l_{EP}							
(early precharge) ($\overline{CAS}$ latency = 3)		−2	−2	−2	−2	−2	−2	
($\overline{CAS}$ latency = 2)		−1	−1	−1	−1	−1	−1	
($\overline{CAS}$ latency = 1)		—	0	—	0	—	0	
Column command to column command	l_{CCD}	1	1	1	1	1	1	
Write command to data in latency	l_{WCD}	0	0	0	0	0	0	
DQM to data in	l_{DID}	0	0	0	0	0	0	
DQM to data out	l_{DOD}	2	2	2	2	2	2	
CKE to CLK disable	l_{CLE}	1	1	1	1	1	1	

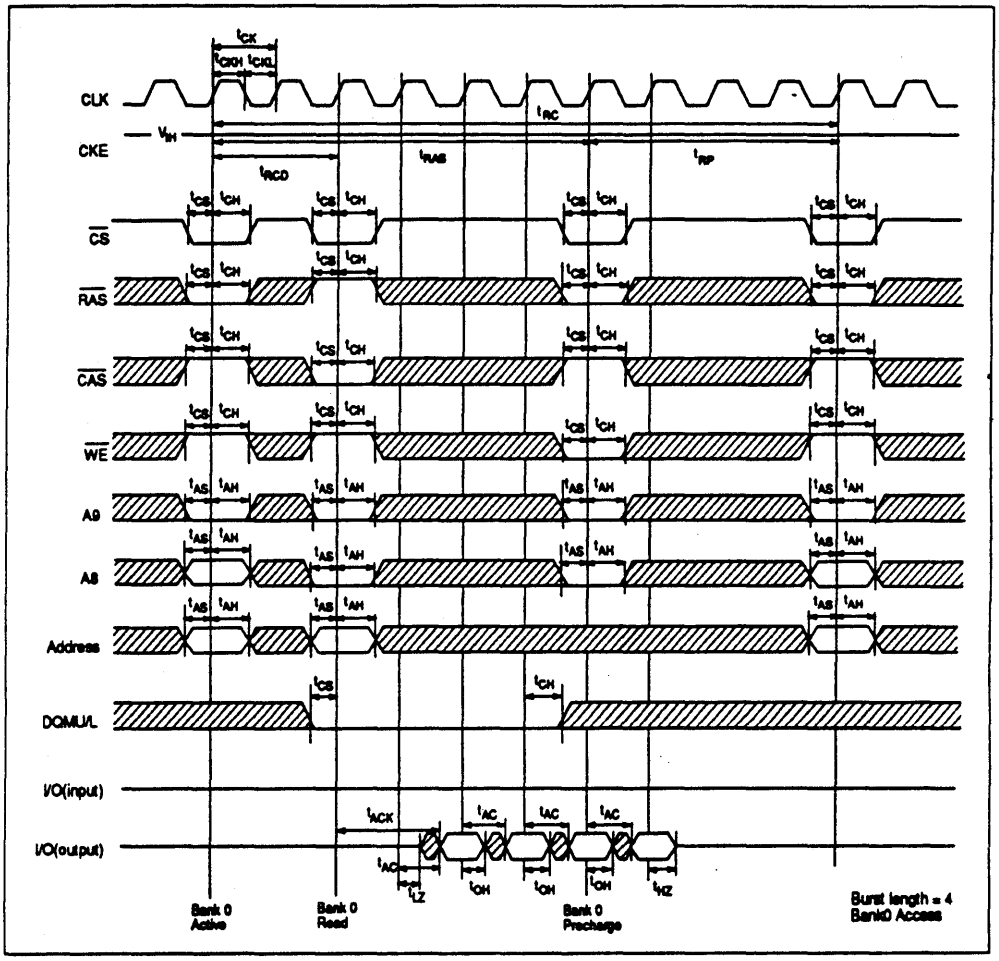
Relationship Between Frequency and Minimum Latency (cont.)

Parameter		HM5241605						
		-15		-17		-20		
Frequency (MHz)		66	33	57	28.5	50	25	
t_{CK} (ns)	Symbol	15	30	17.5	35	20	40	Notes
Register set to active command	t_{RSA}	2	1	2	1	2	1	
CS to command disable	l_{CDD}	0	0	0	0	0	0	
Power down exit to command input	l_{PEC}	1	1	1	1	1	1	
Burst stop to output valid data hold	l_{BSR}							
(CAS latency =1)		—	0	—	0	—	0	
(CAS latency =2, 3)		1	1	1	1	1	1	
Burst stop to output high impedance	l_{BSH}							
(CAS latency = 1)		—	1	—	1	—	1	
(CAS latency = 2)		2	2	2	2	2	2	
(CAS latency = 3)		3	3	3	3	3	3	
Burst stop to write data ignore	l_{BSW}	1	1	1	1	1	1	

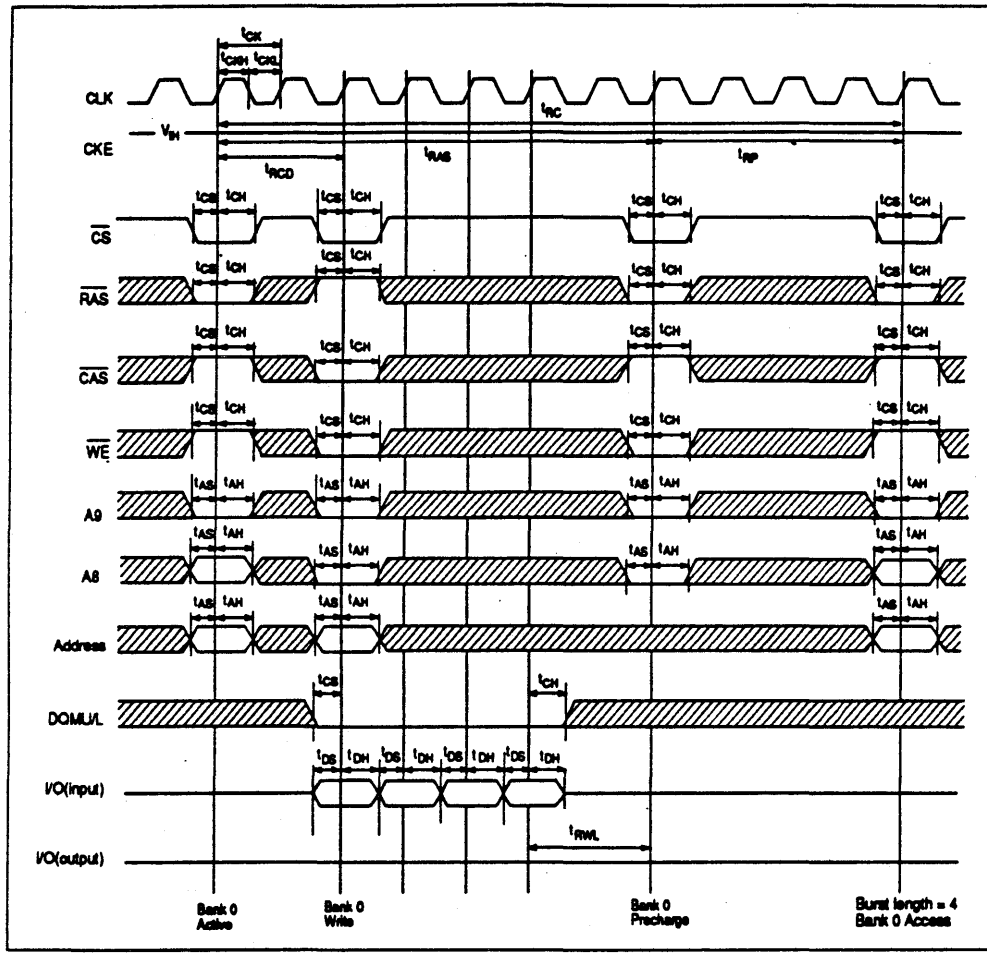
Note: 1. t_{RCD} to t_{RRD} are recommended value.
2. CL = $\overline{CAS}$ latency.

Timing Waveforms

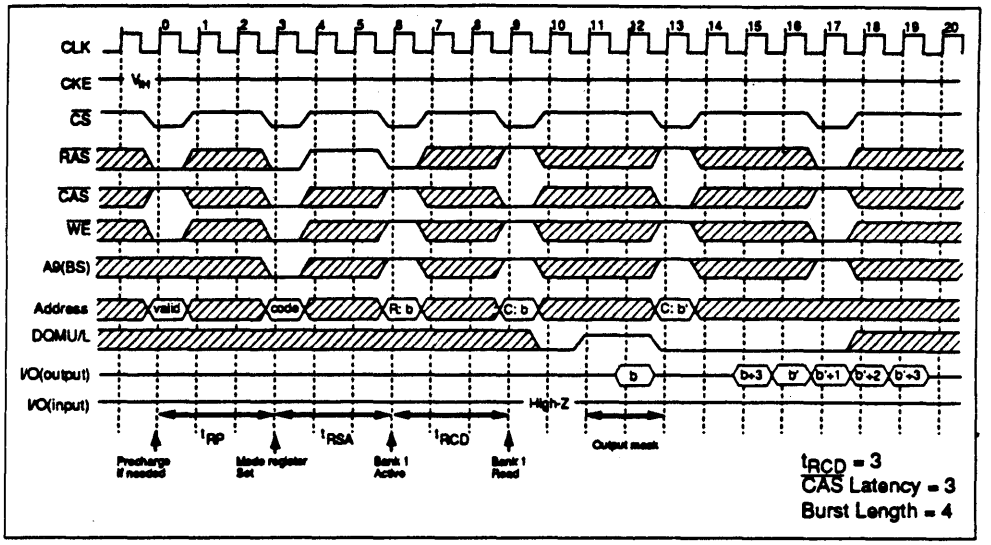
Read Cycle



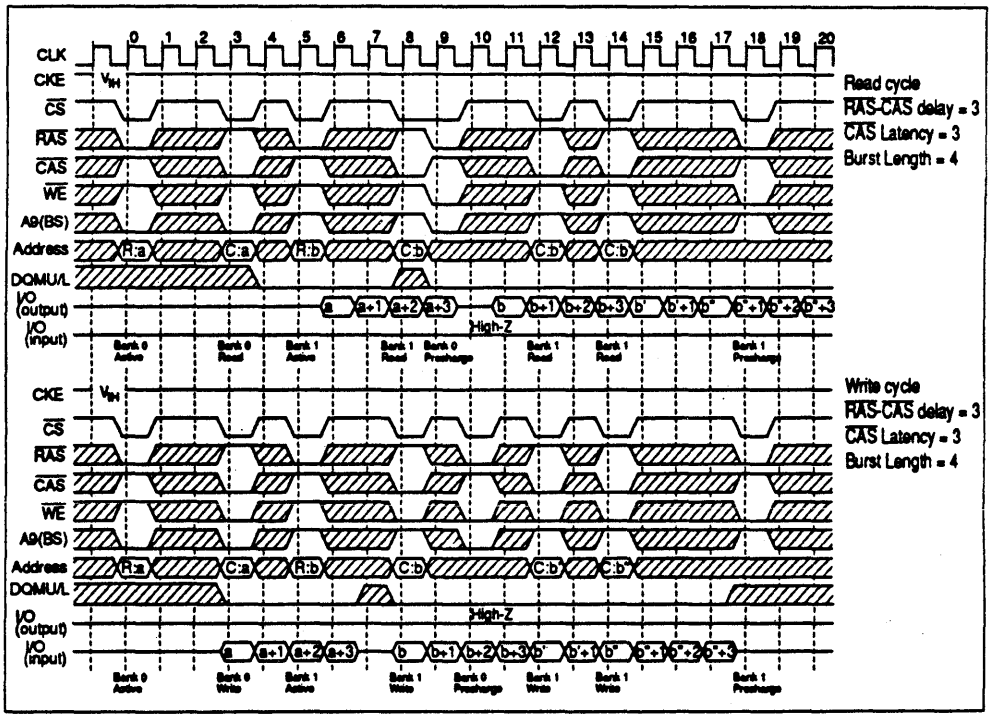
Write Cycle


CLK
CKE
$\overline{CS}$
$\overline{RAS}$
$\overline{CAS}$
$\overline{WE}$
A9
A8
Address
DQM(U/L
I/O(input)
I/O(output)
Bank 0 Active
Bank 0 Write
Bank 0 Precharge
Burst length = 4 Bank 0 Access

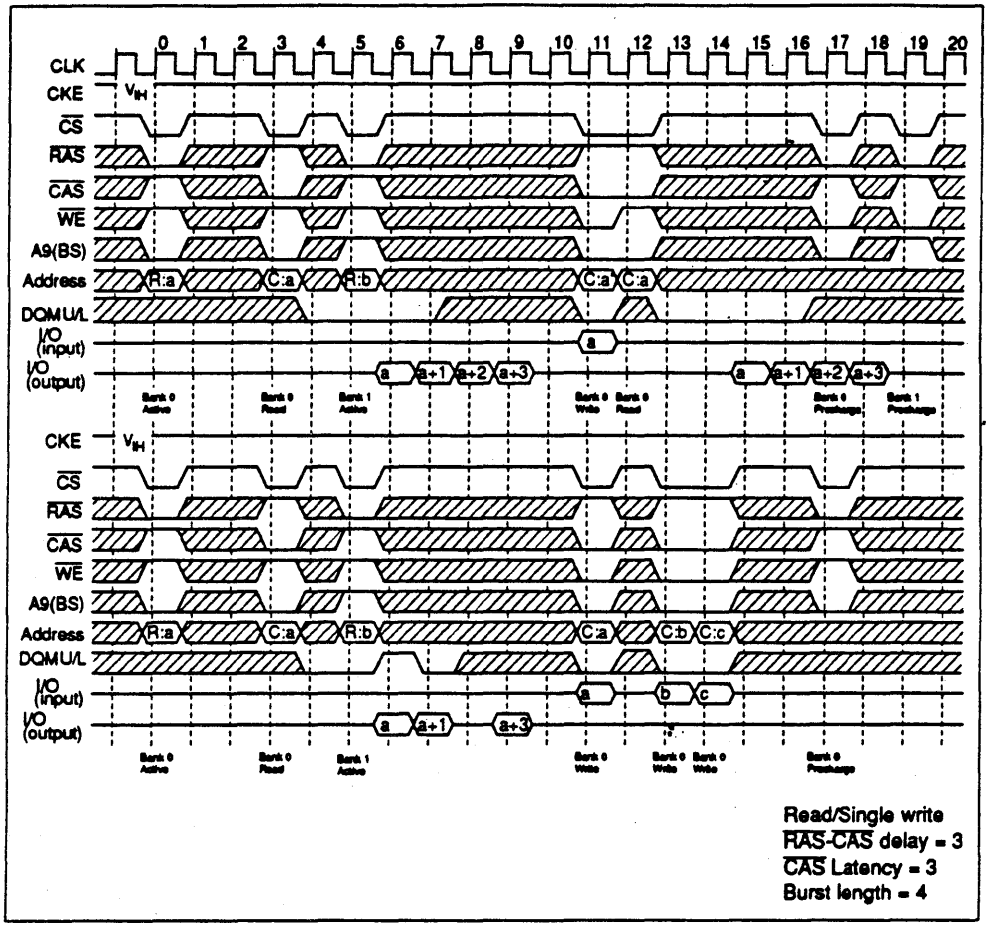
Mode Register Set Cycle



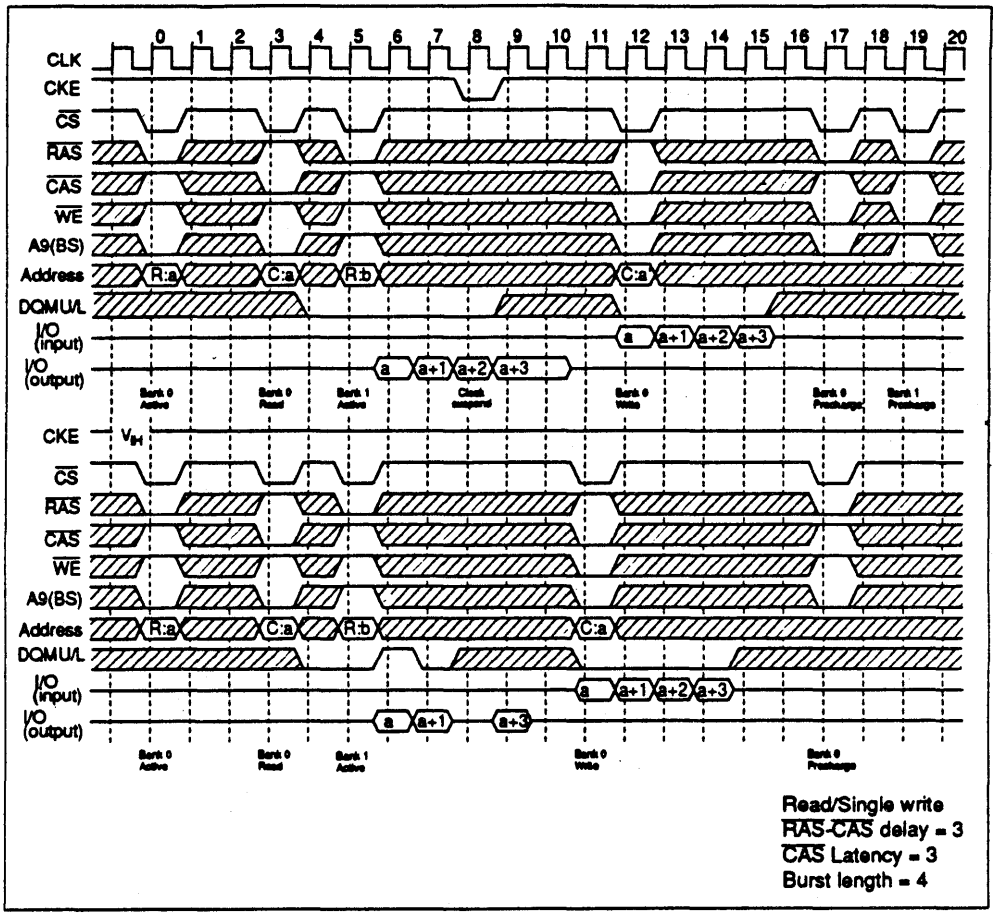
Read Cycle/Write Cycle



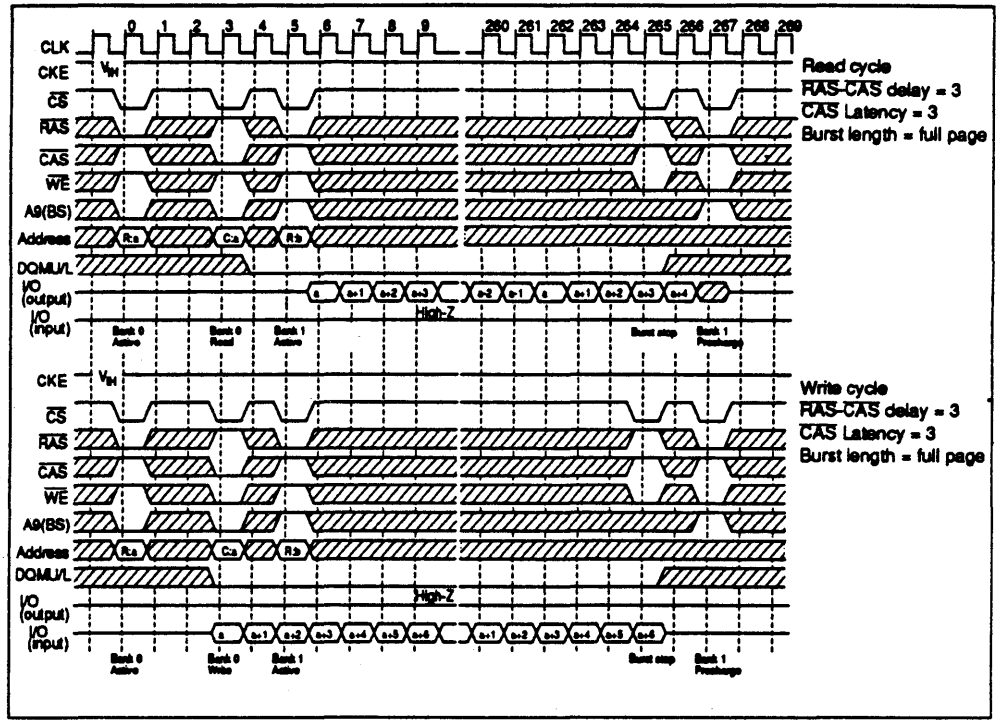
Read/Single Write Cycle



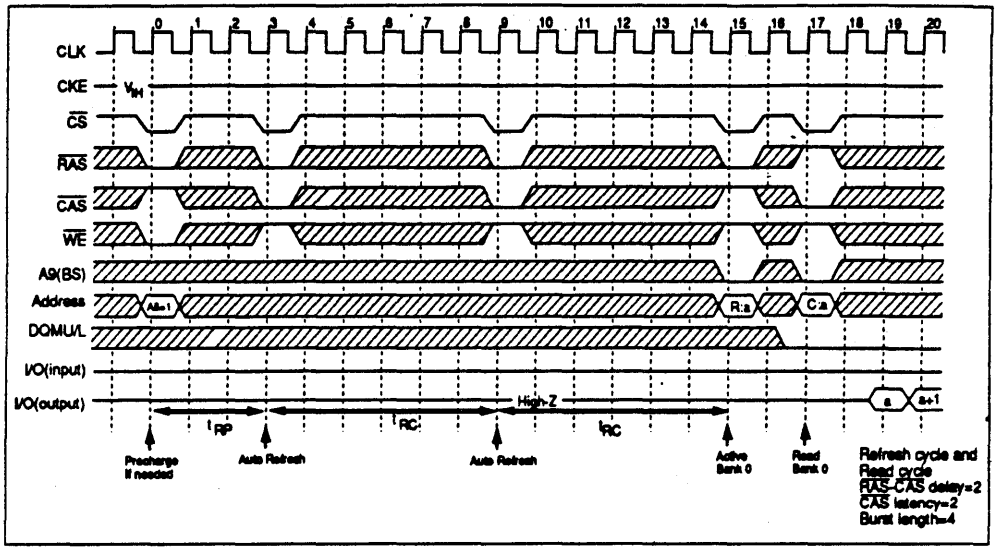
Read/Burst Write Cycle



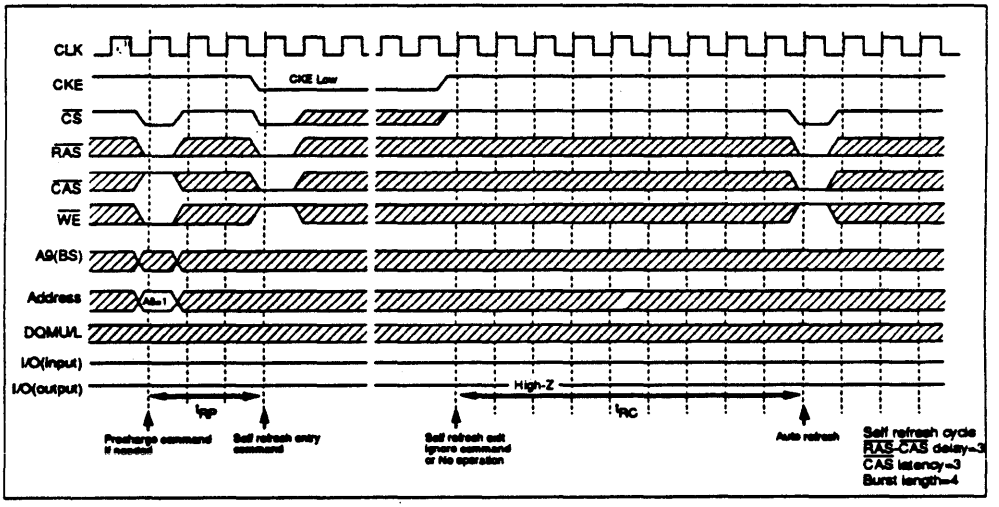
Full Page Read/Write Cycle



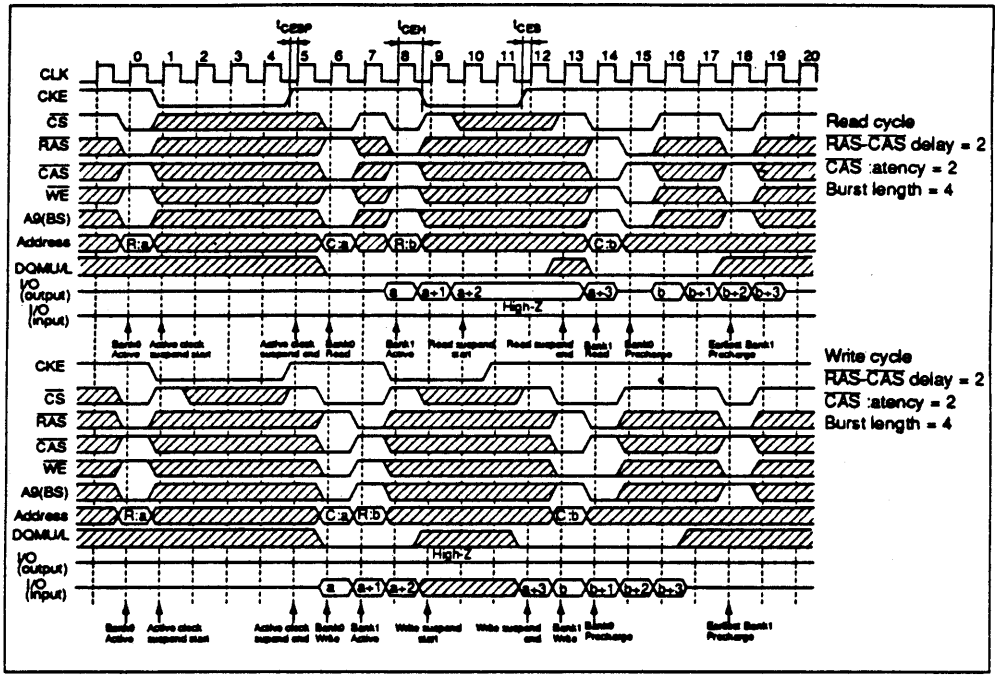
Auto Refresh Cycle



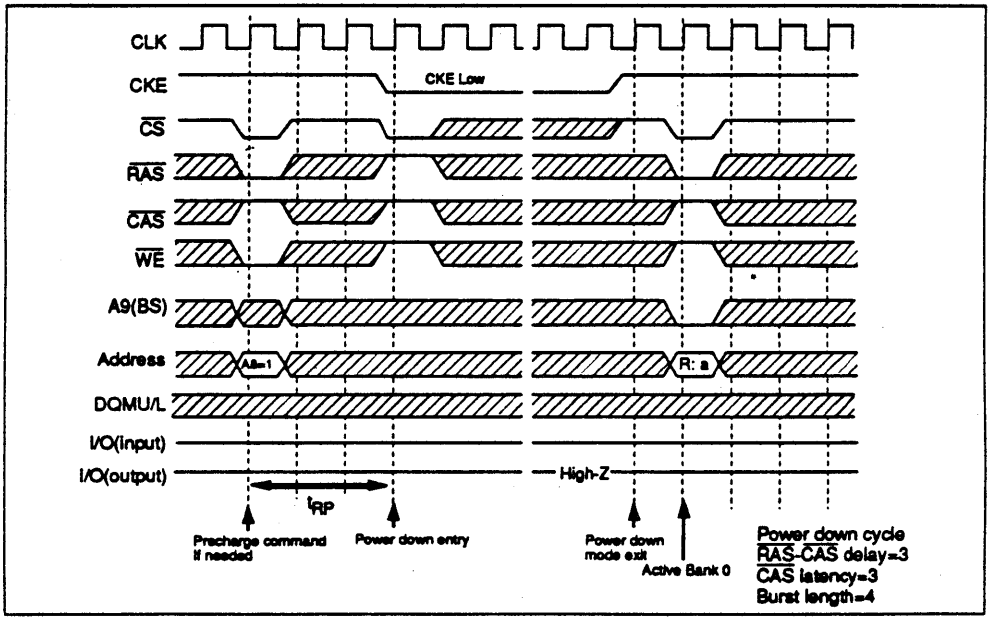
Self Refresh Cycle



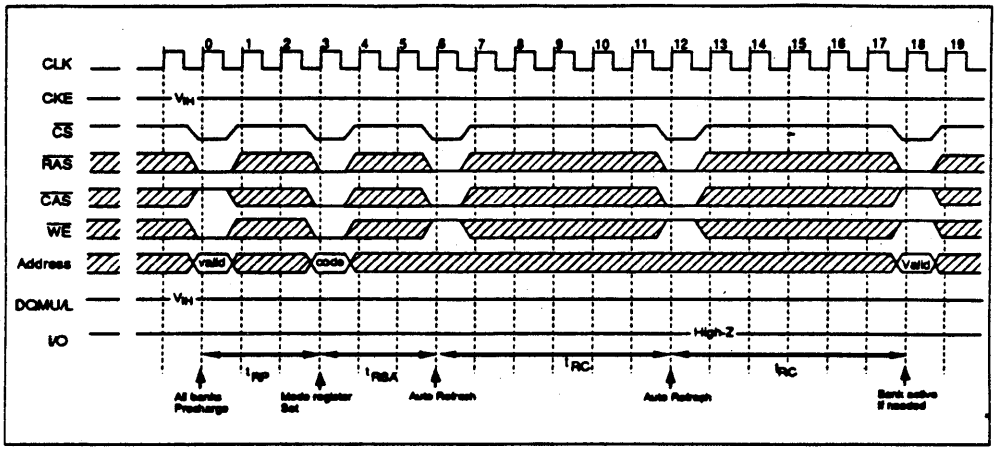
Clock Suspend Mode



Power Down Mode

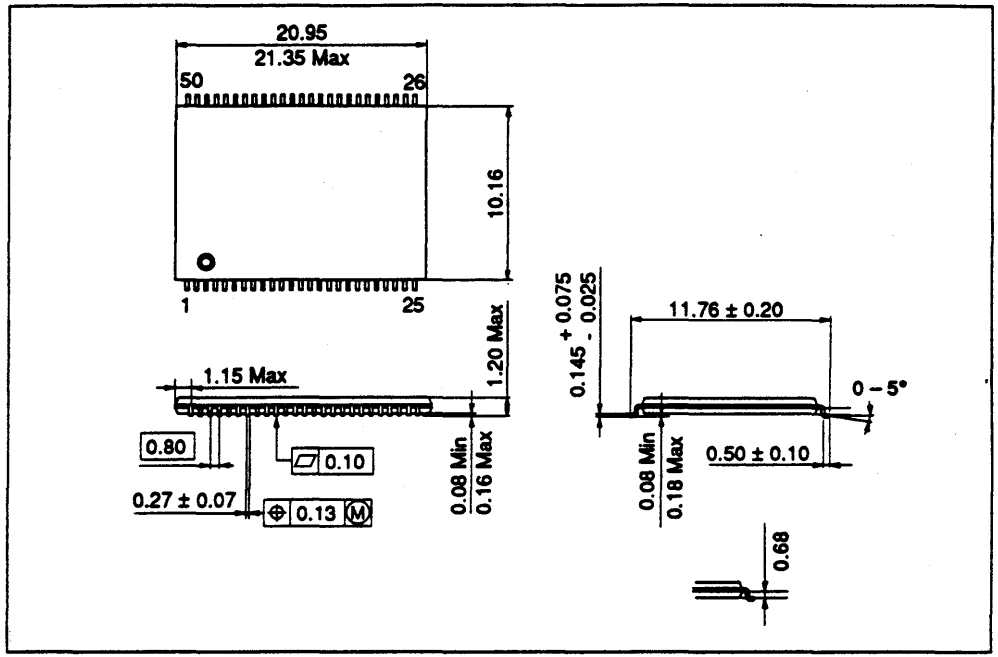


Power Up Sequence



Package Dimensions

HM5241605TT Series (TTP-50D) **Unit: mm**



HM5283206 Series

PRELIMINARY SPEC

131, 072-word x32-bit x2-bank Synchronous Graphic RAM

HITACHI

All inputs and outputs signals refers to rising edge of the clock input. The HM5283206 provides 2 banks to realize better performance. 8 column Block write and write per bit functions are added for graphic applications.

Features

- 3.3V Power supply
- Clock frequency
  80 MHz/66 MHz/57 MHz/50 MHz
- LVTTL interface
- 2 Banks can operates simultaneously and independently
- Burst read / write operation and burst read / single write operation capability
- Programmable burst length
  1/2/4/8 full page
- Programmable burst sequence
  Sequential / interleave
- Full page burst length capability
  Sequential burst
  burst stop capability
- Programmable CAS latency
  1/2/3
- Byte control by DQM
- 8 column block write function with column address mask
- Write per bit function (old mask)
- 2 variations of refresh
  – Auto refresh
  – Self refresh (1024 refresh cycles : 16ms)

Ordering Information

Type No.		Frequency	Package
HM5283206FP-20		50 MHz	100-pin plastic QFP
	-17	57 MHz	
	-15	66 MHz	
	-12	80 MHz	
HM5283206TT-20		50 MHz	400-mil 80-pin plastic TSOP II
	-17	57 MHz	
	-15	66 MHz	
	-12	80 MHz	

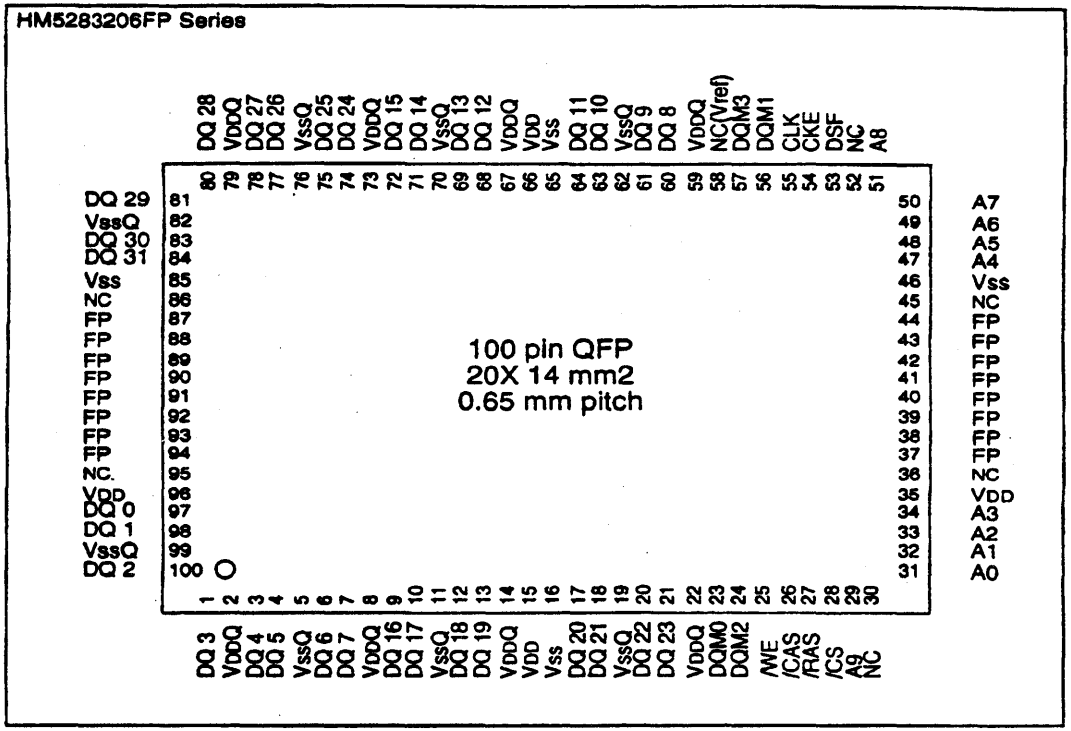
Preliminary : This document contains information on a new product. Specifications and information contained herein are subjected to change without notice.

Hitachi semiconductor

ADE-203-223(Z)

Pin Arrangement

HM5283206FP Series



Pin Description

Pin name	Function		Pin name	Function
A0—A9	Address input		DQM	Byte input/output mask
	— Row address	A0—A8	CLK	Clock input
	— Column addres	A0—A7	CKE	Clock enable
A9	Bank select addres	BS	VDD	Power for internal circuit(3.3V)
DQ0—DQ31	Data-input/out-put		Vss	Ground for internal circuit
/RAS	Row address asserted		VDDQ	Power forDQ pin(3.3V)
	bank enable		VssQ	Gorund for DQ pin
/CS	Chip select		DSF	Special function input flag
/CAS	Column address assreted		NC	No connection
/WE	Write enable		FP	TBD

Pin Functions

CLK(Input pin): Clock provides the fundamental timing signal . The other input signals refer CLK rising edge.

/CS(Input pin): By setting /CS to low level, commands are ready to be accepted.

/RAS, /CAS, /WE, DSF(Input pins): All these pins are used to issue commands.

A0-A8(Input pins): Row address (AX0-AX8) is acquired through A0-A8 pins when bank active commands are executed. Column address (AY0-AY7) is acquired through A0-A7 when read or write commands are executed. A8 determines precharge mode when precharge commands are issued . If A8 is low, select bank goes into precharge process. If A8 is high, all banks are selected for precharge operation.

A9(Input pins): A9 is a bank select signal(BS). In case A9 = '0', bank 0 is selected. In case A9 = '1',bank 1 is selected.

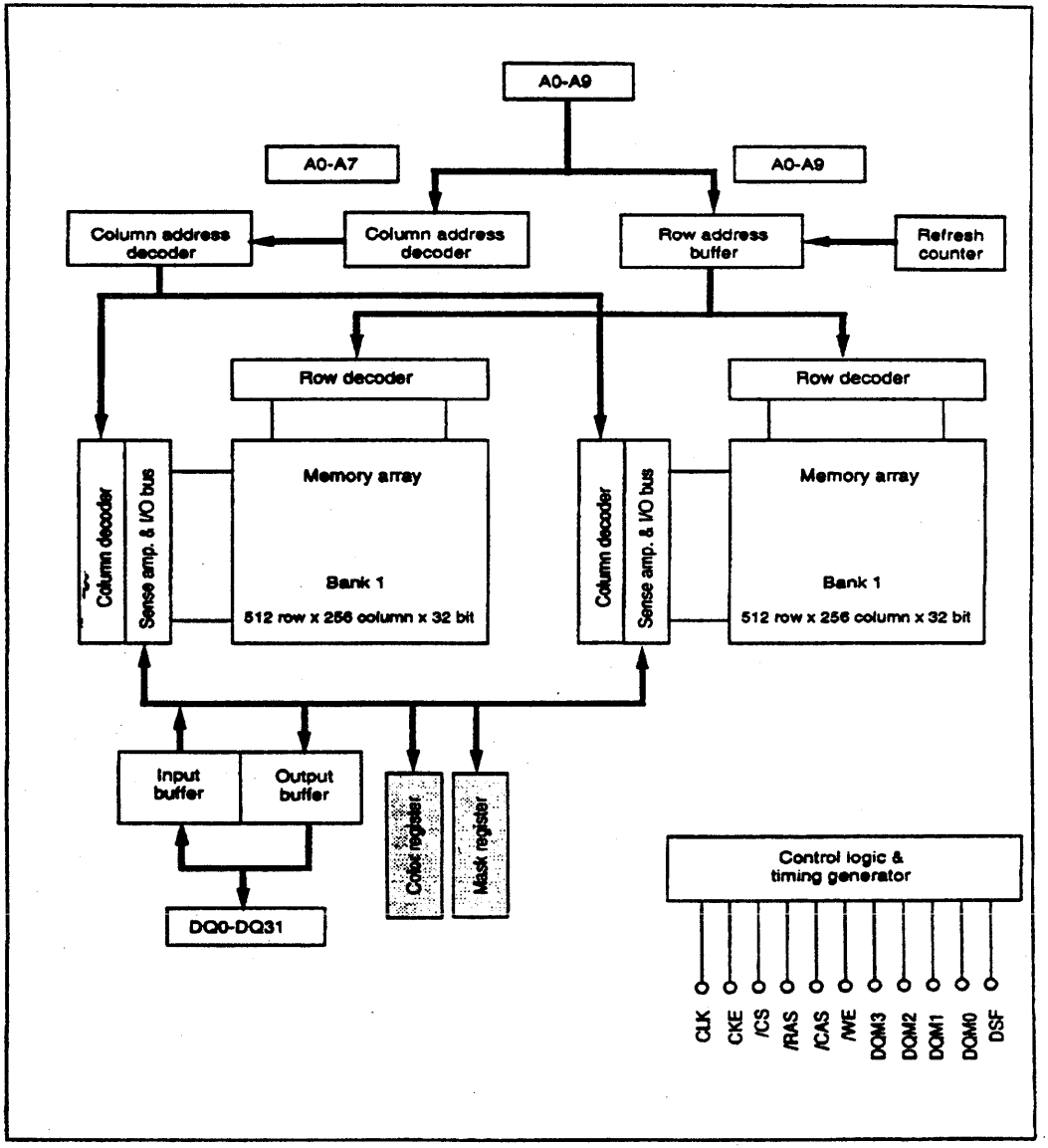
CKE(Input pin): By referring low level on CKE pin, HM5283206 determines to go into clock suspend modes or power down modes. In self refresh mode, low level on this pin is also referred to turn on refresh process.

DQM0, DQM1, DQM2 and DQM3(Input pins): DQM0 controls DQ0-DQ7. DQM1 controls DQ8 -DQ15. DQM2 controls DQ16-DQ23. DQM3 controls DQ24-DQ31. In read mode, referring high level on DQM pins, HM5283206 floats related DQ pins. In write mode, referring high level on DQM pins, HM5283206 ignores input data through related DQ pins.

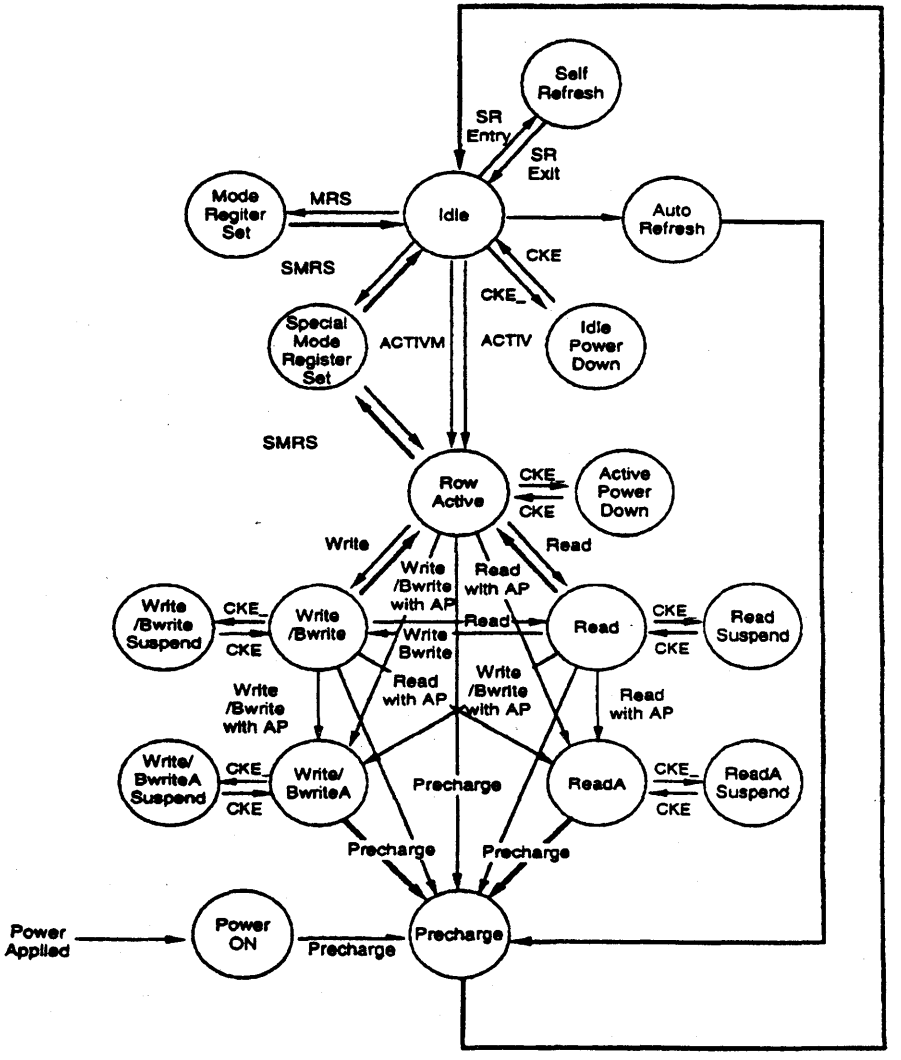
DQ0-DQ31(Input/output): These are the data line for the HM5283206.

VDD, VSS, VDDQ, VSSQ(Power supply): VDD and VSS are power supply pins for internal circuits. VDDQ and VSSQ are power supply pins for DQ buffers.

Block Diagram



Simplified State Diagram



Automatic transition after completion of command

Transition resulting from command input.

Note.1.After the auto-refresh operation, precharge operation is performed automatically and enter the IDLE state.

Command Operation

Command Truth Table

The HM5283206 recognizes the following commands specified by the /CS, /RAS, /CAS, /WE, DSF and address pins.

Function		CKE n-1	CKE n	/CS	/RAS	/CAS	/WE	DSF	A9	A8	A7-0
Ignore Command	DESL	H	X	H	X	X	X	X	X	X	X
No operation	NOP	H	X	L	H	H	H	L	X	X	X
Burst stop in full page	BST	H	X	L	H	H	L	L	X	X	X
Column address & read command	READ	H	X	L	H	L	H	L	V	L	V
Read with auto precharge	READA	H	X	L	H	L	H	L	V	H	V
Column address & write command	WRIT	H	X	L	H	L	L	L	V	L	V
Write with auto precharge	WRITA	H	X	L	H	L	L	L	V	H	V
Row address strobe and bank act.	ACTV	H	X	L	L	H	H	L	V	V	V
Precharge select bank	PRE	H	X	L	L	H	L	L	V	L	X
Precharge all banks	PALL	H	X	L	L	H	L	L	X	H	X
Mode register set	MRS	H	X	L	L	L	L	L	L	L	V
Row address strobe and bank act. and Masked write enable	ACTVM	H	X	L	L	H	H	H	V	V	V
Column address & Block write command	BWRIT	H	X	L	H	L	L	H	V	L	V
Block write with auto precharge	BWRITA	H	X	L	H	L	L	H	V	H	V
Special mode register set	SMRS	H	X	L	L	L	L	H	L	L	V

Note: H:High level. L: Low level: X:H or L(Don't care). V:Valid address input

.Ignore command[DESL]: When this command is set (/CS is high), the HM5283206 ignores command input. Internal operation is held.

.No operation[NOP]: This command is not an execution command and does not affect internal operation.

.Burst stop in full-page[BST]: This command stops the full page burst operation (burst length is 256(full-page)), and is illegal for the burst length 1, 2, 4, 8. Full page burst continues until this command is input.

When full page read/write is completed, it automatically returns to the start address, and read/write is performed repeatedly.

.Column address strobe and read command[READ]: This command starts read operation. The start address of burst read is determined by the column address(AY0-AY7) and the bank select address A9. After the read operation, the HM5283206 floats DQ output buffer.

.Read with auto-precharge[READ A]: This command automatically performs a precharge operation after a burst read with burst length 1, 2, 4 or 8. When the burst length is full-page(256), this command is illegal.

.Column address strobe and write command[WRIT]: This command starts a write operation. When the burst write mode is selected, the column address (AY0-AY7) and the bank select address A9 become the start address of burst write . When the single write mode is selected, data is only written to the location defined by the column address (AY0 to AY7) and the bank select address A9.

.Column address strobe and block write command[BWRIT]: By this command, the HM5283206 executes a block write with the data stored in the color register. The column block address is given through A0-A7 pins at the same cycle when this command is issued. To go details about block write operation, refer to "Block write and write per bit".

.Write with auto-precharge[WRIT A]: This command automatically performs a precharge operation after burst write or single write. For the full-page mode, this command is forbidden.

.Block write with auto-precharge[BWRIT A]: This command automatically performs a precharge operation after block write.

.Row address strobe and bank activate [ACTV]: This command activates the bank selected by A9 pin and determines the row address (AX0-AX8), with refer to A0-A7 and A8 pins. When BS is low, bank 0 is activated. When BS is high, bank 1 is activated.

.Row address strobe, bank activate and write per bit enable[ACTVM]: This command not only performs the operation executed by ACTV but also enables write per bit. To go detail about write per bit function, refer to "Block write and write per bit"

.Precharge selected bank[PRE]: This command starts precharge operation for the bank selected by A9. If A9 is low, bank 0 is selected. If A9 is high, bank 1 is selected.

.Precharge all banks[PALL]: This command starts a precharge operation for all banks.

.Refresh[REF/SELF]: This command starts refresh operation.There are two types of refresh operation. One is auto refresh(CBR type), the other is self-refresh. For details refer to the CKE truth table.

.Mode register set[MRS]: The HM5283206 has a mode register that defines how it operates. The mode register is specified by the address pins (A0-A9) at the mode register set cycle. For details, refer to the mode register configuration. Just after power on, the contents of the mode register are undefined so that this command should be executed.

.Special mode register set[SMRS]: By this command, color register or mask register is set, with refer to A5 and A6 pins. For details, refer to "Special mode register configuration".

DQM Truth Table

Function		CKE n-1	n	DQMi
Ith byte write enable/out put enable	ENB i	H	X	L
Ith byte write input/output disable	MASK i	H	X	H

Note: H:High level. L: Low level. X:H or L(Don't care). i=0,1,2,3
DQM0 for DQ0-DQ7, DQM1 for DQ8-DQ15, DQM2 for DQ16-DQ23, DQM3 for DQ24-DQ31

The HM5283206 series can control DQ input/output buffers with use of DQMi(i=0, 1, 2, 3). DQM0 controls DQ0-DQ7. DQM1 controls DQ8-DQ15. DQM2 controls DQ16-DQ23. DQM3 controls DQ24-DQ31. During read operation, as long as DQMi is low, corresponding DQ output buffers are kept active so that data are driven out. In order to stop data output trough DQ pins, corresponding DQM pin should be set to high to float DQ output.

During write operation, as long as DQMi pins low, data through corresponding DQ input buffers are driven into HM5283206. To stop new data through DQ input buffers to keep the previous data, corresponding DQMi pin should be set to high. For details, refer to the DQM control section of the operating instructions.

CKE Truth Table

Current State	Function		CKE n-1	CKE n	/CS	/RAS	/CAS	/WE	DSF	Address
Active	Clock suspend mode entry		H	L	X	X	X	X	X	X
Any	Clock suspend		L	L	X	X	X	X	X	X
Clock suspend	Clock suspend mode exit		L	H	X	X	X	X	X	X
Idle	auto refresh command	REF	H	H	L	L	L	H	L	X
Idle	Self refresh entry	SELF	H	L	L	L	L	H	L	X
Idle	Power down entry		H	L	L	H	H	H	L	X
Self refresh	Self refresh exit		L	H	L	H	H	H	L	X
			L	H	H	X	X	X	L	X
Power down	Power down exit		L	H	L	H	H	H	L	X
			L	H	H	X	X	X	X	X

Note: H:High level. L: Low level. X:H or L(Don't care).

.Clock suspend mode entry:
The HM5283206 enters into clock suspend mode from active mode by setting CKE to low. There are few types of clock suspend mode depends on the state when CKE level is changed from 'H' to "L'.

-ACTIVE clock suspend: If CKE-transition(1 to 0) happens during bank active states, bank active status is kept. Any input signals are ignored in this mode.

-READ and READ A suspend: If CKE transition(1 to 0) happens during read operation, read operation is kept going or DQ output data is driven out until completion. Any input signals are ignored in this mode.

-WRITE(BLOCK WRITE) and WRITE A(BLOCK WRITE A) suspend: If CKE-transition(1 to 0) happens during write operation, though any input signals include DQ input data ignored, write operation is kept going until completion. Any input signals are ignored in this mode.

.Clock suspend mode exit: By changing CKE level from 0 to 1, clock suspend mode is punctuated.

.IDLE: In this state, all banks are kept precharged and no banks are activating.

.Auto-refresh command [REF]:
When this command is input from the IDLE state, the HM5283206 starts auto-refresh operation.(The auto-refresh is the same as the CBR refresh of conventional DRAM.) During the auto-refresh operation, refresh address and bank select address is internally generated. For every auto-refresh command, the internal address counter is updated. Accordingly, 1024 times are required to refresh the entire memory. Before executing the auto-refresh command, all banks must be in the IDLE state. No precharge commands are required after auto-refresh, since the precharge for all banks is automatically performed after auto-refresh,.

.Self-refresh entry[SELF]: When this command is input during the IDLE state, the HM5283206 starts self-refresh operation. After the execution of this command, self-refresh continues while CKE is low. Since self-refresh is performed internally and automatically, external refresh operations are unnecessary.

.Power down mode entry: When this command is executed during the IDLE state, the HM5283206 enters into the power down mode. In power down mode, power consumption is suppressed by cutting off the initial input circuit.

.Power down exit: When this command is executed in the power down mode, the HM5283206 can exit from power down mode. After exiting from power down mode, the HM5283206 enters into the IDLE state.

.Self-refresh exit:
When this command is executed during self-refresh mode, the HM5283206 can exit from self-refresh mode. After existing the self-refresh mode, the HM5283206 enters into the IDLE state.

Function truth table

The following tables show how each command works and what command can be executed in the state given.

Current state	/CS	/RAS	/CAS	/WE	DSF	Address	Command	Operation
Precharge	H	X	X	X	X	X	DESL	Enter idle after tRP
	L	H	H	H	L	X	NOP	Enter idle after tRP
	L	H	H	L	L	X	BST	ILLEGAL
	L	H	L	H	L	BA, CA, A8	READ/A	ILLEGAL
	L	H	L	L	L	BA, CA, A8	WRIT/A	ILLEGAL
	L	L	H	H	L	BA, RA	ACTV	ILLEGAL
	L	L	H	L	L	BA, A8	PRE, PALL	ILLEGAL
	L	L	L	H	L	X	REF, SELF	ILLEGAL
	L	L	L	L	L	MODE	MRS	ILLEGAL
	L	L	H	H	H	BA, RA	ACTVM	ILLEGAL
	L	H	L	L	H	BA, CA, A8	BWRIT/A	ILLEGAL
	L	L	L	L	H	Special MODE	SMRS	ILLEGAL

Note: H:High level. L: Low level. X:H or L(Don't care).

Function Truth Table(cont.)

Current state	/CS	/RAS	/CAS	/WE	DSF	Address	Command	Operation
Idle	H	X	X	X	X	X	DESL	NOP
	L	H	H	H	L	X	NOP	NOP
	L	H	H	L	L	X	BST	NOP
	L	H	L	H	L	BA, CA, A8	READ/A	ILLEGAL
	L	H	L	L	L	BA, CA, A8	WRIT/A	ILLEGAL
	L	L	H	H	L	BA, RA	ACTV	Bank and row active
	L	L	H	L	L	BA, A8	PRE, PALL	NOP
	L	L	L	H	L	X	REF, SELF	Refresh
	L	L	L	L	L	MODE	MRS	Mode register set
	L	L	H	H	H	BA, RA	ACTVM	Bank and row active & write per bit enable
	L	H	L	L	H	BA, CA, A8	BWRIT/A	ILLEGAL
	L	L	L	L	H	Special Mode	SMRS	Special mode register set
Row active	H	X	X	X	X	X	DESL	NOP
	L	H	H	H	L	X	NOP	NOP
	L	H	H	L	L	X	BST	NOP
	L	H	L	H	L	BA, CA, A8	READ/A	Start read
	L	H	L	L	L	BA, CA, A8	WRIT/A	Start write
	L	L	H	H	L	BA, RA	ACTV	Other bank active Illegal on the same bank
	L	L	H	L	L	BA, A8	PRE, PALL	Precharge
	L	L	L	H	L	X	REF, SELF	ILLEGAL
	L	L	L	L	L	MODE	MRS	ILLEGAL
	L	L	H	H	H	BA, RA	ACTVM	Other bank active & write per bit enable Illegal on the same bank
	L	H	L	L	H	BA, CA, A8	BWRIT/A	Start block write
	L	L	L	L	H	Special Mode	SMRS	Special mode register set

Note: H:High level. L: Low level. X:H or L(Don't care).

Function Truth Table(cont.)

Current state	/CS	/RAS	/CAS	/WE	DSF	Address	Command	Operation
Read	H	X	X	X	X	X	DESL	Continue operation
	L	H	H	H	L	X	NOP	Continue operation
	L	H	H	L	L	X	BST	Burst stop in full page
	L	H	L	H	L	BA, CA, A8	READ/A	Start new read
	L	H	L	L	L	BA, CA, A8	WRIT/A	Start write
	L	L	H	H	L	BA, RA	ACTV	Other bank active Illegal on the same bank
	L	L	H	L	L	BA, A8	PRE, PALL	Precharge
	L	L	L	H	L	X	REF, SELF	ILLEGAL
	L	L	L	L	L	MODE	MRS	ILLEGAL
	L	L	H	H	H	BA, RA	ACTVM	Other bank and row active & write per bit enable Illegal on the same bank
	L	H	L	L	H	BA, CA, A8	BWRIT/A	Start block write
	L	L	L	L	H	Special Mode	SMRS	ILLEGAL
Read with auto	H	X	X	X	X	X	DESL	Continue operation
precharge	L	H	H	H	L	X	NOP	Continue operation
	L	H	H	L	L	X	BST	ILLEGAL
	L	H	L	H	L	BA, CA, A8	READ/A	ILLEGAL
	L	H	L	L	L	BA, CA, A8	WRIT/A	ILLEGAL
	L	L	H	H	L	BA, RA	ACTV	Other bank active Illegal on the same bank
	L	L	H	L	L	BA, A8	PRE, PALL	ILLEGAL
	L	L	L	H	L	X	REF, SELF	ILLEGAL
	L	L	L	L	L	MODE	MRS	ILLEGAL
	L	L	H	H	H	BA, RA	ACTVM	Other bank active & write per bit enable Illegal on the same bank
	L	H	L	L	H	BA, CA, A8	BWRIT/A	ILLEGAL
	L	L	L	L	H	Special Mode	SMRS	ILLEGAL

Note: H:High level. L: Low level. X:H or L(Don't care).

Function Truth Table(cont.)

Current state	/CS	/RAS	/CAS	/WE	DSF	Address	Command	Operation
Write/Bwrite	H	X	X	X	X	X	DESL	Continue operation
	L	H	H	H	L	X	NOP	Continue operation
	L	H	H	L	L	X	BST	Burst stop in full page
	L	H	L	H	L	BA, CA, A8	READ/A	Start read
	L	H	L	L	L	BA, CA, A8	WRIT/A	Start new write
	L	L	H	H	L	BA, RA	ACTV	Other bank active Illegal on the same bank
	L	L	H	L	L	BA, A8	PRE, PALL	Precharge
	L	L	L	H	L	X	REF, SELF	ILLEGAL
	L	L	L	L	L	MODE	MRS	ILLEGAL
	L	L	H	H	H	BA, RA	ACTVM	Other bank and row active & write per bit enable Illegal on the same bank
	L	H	L	L	H	BA, CA, A8	BWRIT/A	Start block write
	L	L	L	L	H	Special Mode	SMRS	ILLEGAL
Write/Bwrite with	H	X	X	X	X	X	DESL	Continue operation
auto precharge	L	H	H	H	L	X	NOP	Continue operation
	L	H	H	L	L	X	BST	ILLEGAL
	L	H	L	H	L	BA, CA, A8	READ/A	ILLEGAL
	L	H	L	L	L	BA, CA, A8	WRIT/A	ILLEGAL
	L	L	H	H	L	BA, RA	ACTV	Other bank active Illegal on the same bank
	L	L	H	L	L	BA, A8	PRE, PALL	ILLEGAL
	L	L	L	H	L	X	REF, SELF	ILLEGAL
	L	L	L	L	L	MODE	MRS	ILLEGAL
	L	L	H	H	H	BA, RA	ACTVM	Other bank active & write per bit enable Illegal on the same bank
	L	H	L	L	H	BA, CA, A8	BWRIT/A	ILLEGAL
	L	L	L	L	H	Special Mode	SMRS	ILLEGAL

Note: H:High level. L: Low level. X:H or L(Don't care).

Function Truth Table(cont.)

Current state	/CS	/RAS	/CAS	/WE	DSF	Address	Command	Operation
Refresh	H	X	X	X	X	X	DESL	NOP
	L	H	H	H	L	X	NOP	NOP
	L	H	H	L	L	X	BST	NOP
	L	H	L	H	L	BA, CA, A8	READ/A	ILLEGAL
	L	H	L	L	L	BA, CA, A8	WRIT/A	ILLEGAL
	L	L	H	H	L	BA, RA	ACTV	ILLEGAL
	L	L	H	L	L	BA, A8	PRE, PALL	ILLEGAL
	L	L	L	H	L	X	REF, SELF	ILLEGAL
	L	L	L	L	L	MODE	MRS	ILLEGAL
	L	L	H	H	H	BA, RA	ACTVM	ILLEGAL
	L	H	L	L	H	BA, CA, A8	BWRIT/A	ILLEGAL
	L	L	L	L	H	Special Mode	SMRS	ILLEGAL

Note: H:High level. L: Low level. X:H or L(Don't care).

From[PRECHARGE]
To [DESL], [NOP]: When these commands are executed, the HM5283206 enters into the IDLE state after tRP has elapsed from the completion of precharge.

From[IDLE]
To[DESL], [NOP], [BST], [PRE] or [PALL]: These commands result in no operation.
To[ACTV] : The bank specified by the address pins and the ROW address is activated.
To[ACTVM]: The bank specified by the address pins and the ROW address is activated. In addition, write per bit is also enabled.
To[REF], [SELF]: The HM5283206 enters into refresh mode(auto-refresh or self-refresh).
To[MRS]: The HM5283206 enters into the mode register set cycle.
To[SMRS]: The HM5283206 enters into the special mode register set cycle.

From[ROW ACTIVE]:
To [DESL], [NOP], or [BST]: These commands in no operation.
To[READ], [READA]: A read operation starts. (However, an interval of tRCD is required)
To[WRIT], [BWRIT], [WRITA] or [BWRIT A]: A write or block write operation starts. (However, an interval of tRCD is required.)
To[ACTV]: This commands makes the other bank active. (However, an interval tRRD is required.) Attempting to reactivate the current active bank is illegal.
To[ACTVM]: This commands makes the other bank active and enable write per bit. (However, an interval tRRD is required.) Attempting to reactivate the current active bank is illegal.
To[SMRS]: The HM5283206 sets the special mode register.
To [PRE], [PALL]: These commands set the HM5283206 to precharge mode. (However, an interval or tRAS is required.)

From [READ]
To[DESL], [NOP]: These commands continue read operation until the burst operation completed.
To[BST]: This command stops a full-page burst.
To[READ], [READA]: Data output by the previous read command continues to finish. After /CAS latency, the data output resulting from the next command will start.
To[WRIT], [BWRIT], [WRITA] or [BWRIT A]: These commands stop burst read and start write cycle.
To[ACTV]: This command activates the other bank. Attempting to reactivate the current active bank is illegal.
To[ACTVM]: This command activates the other bank and enables write per bit. Attempting to reactivate the current active bank is illegal.
To [PRE], [PALL]: These commands put the HM5283206 into precharge mode. (However, an interval or tRAS is required.)

From [READ with AUTO-PRECHARGE]
To [DESL], [NOP]: These commands continue read operation until burst operation is completed, then the HM5283206 enters into precharge mode.
To[ACTV]: This command activates the other bank. Attempting to reactivate the current active bank is illegal.
To[ACTVM]: This command activates the other bank and enables write per bit. Attempting to reactivate the current active bank is illegal.

From [WRITE] or [BWRITE]
To[DESL], [NOP]: These commands continue write operations until burst operation is completed.
To[BST]: This command stops a full-page burst.
To[READ] or [READ. A]: These commands stop burst write cycle and start read cycle.
To[WRIT], [BWRIT], [WRIT A] or [BWRIT A]: These commands stop burst write cycle and start new burst write or block write.
To[ACTV]: This command activates the other bank. Attempting to reactivate the current active bank is illegal.
To[ACTVM]: This command activates the other bank and enables write per bit. Attempting to reactivate the current active bank is illegal.
To[PRE] or [PALL]: These commands stop burst cycle, then the HM5283206 enters into precharge mode.

From[WRIT A] or [BWRIT A]
To[DESL], [NOP]: These commands continue current write operation until the burst operation is completed then the HM5283206 goes into the precharge process.
To[ACTV]: This commands activates the other bank. Attempting to reactivate the current active bank is illegal.
To[ACTVM]: This command activates the other bank and enables write per bit. Attempting to reactivate the current active bank is illegal.

From[REFRESH]
To[DESL], [NOP], [BST]: After the auto-refresh cycle (after tRC), the HM5283206 automatically enters into the IDLE state.

Operation of HM5283206 Series

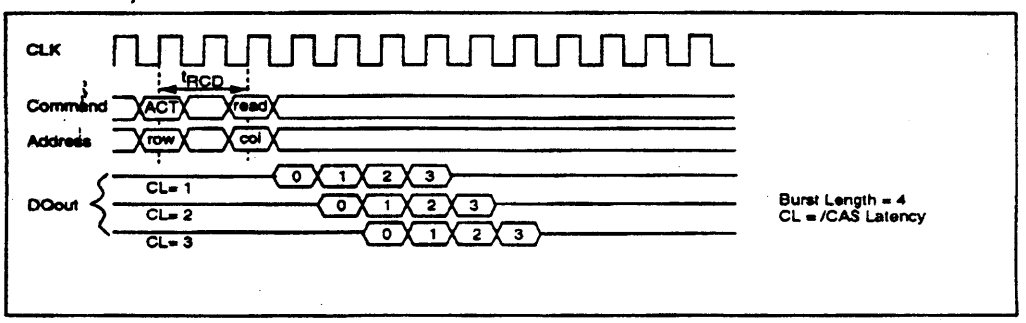
Read/Write Operations

-Bank active
Before executing a read or write operation, the corresponding bank and the row address must be activated by the bank active(ACTV, ACTIVM) command. Either bank 0 or 1 is activated according to the level on A9 pin, and the row address (AX0 to AX8) is activated by the A0-A8 pins at the bank active command cycle. An interval of tRCD is required between the bank active command input and the following read/write command input.

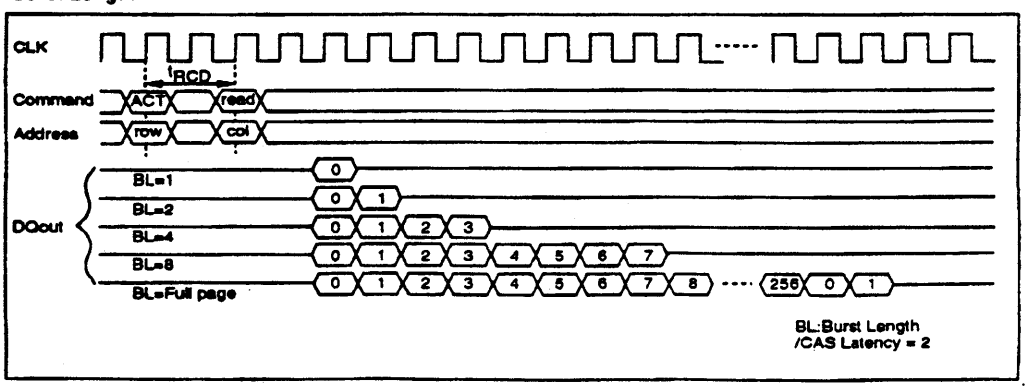
-Read operation
A read operation starts when a read command is input. Output buffers become active in the cycle after read command issued so that the HM5283206 can perform burst read operation.

The burst length can be set to 1, 2, 4, 8 or 256 (full-page). The start address of burst read is defined by the column address (AY0 to AY7) and the bank select address (A9) loaded at the cycle when the read command is issued. In read operation, data output starts after the number of cycles specified by the /CAS latency.
When the burst length is 1, 2, 4 or 8, DQ buffers automatically become High-Z at the next cycle after the successive burst read has been completed.
When the burst length is full-page(256), data are repeatedly output until the burst stop command, another read/write commands or precharge commands are input. The /CAS latency and burst length must be specified on the mode register.

/CAS Latency



Burst Length



Read / Write Operation(cont.)

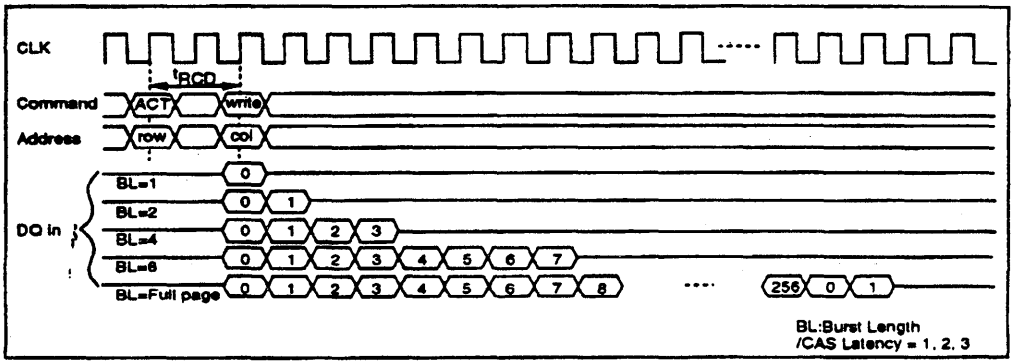
.Write operation

Burst write or single mode is selected by the OPCODE(A9, A8) of the mode register.

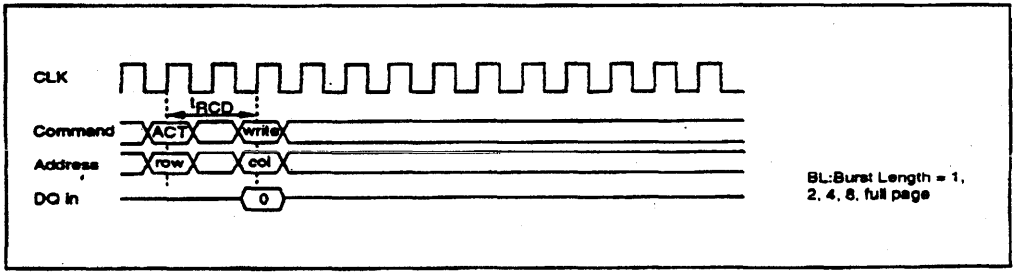
(1) Burst write: Prior to execute burst write operation, the OPCODE(A9, A8) should be set to (0, 0). The latency of data input is 0 that is burst write starts on the same cycle when the write command is issued. The burst length can be set to 1, 2, 4, 8 and 256(full-page). The start column of burst write is defined by the column address and the bank select address A9 loaded at the write command set cycle.

(2) Single write: Prior to execute single write operation, the OPCODE(A9, A8) should be set to (1, 0). In a single write operation, data are only written to the single column defined by the column address and the bank select address loaded at the write command set cycle regardless of the defined burst length. (The latency of data input is 0).

Burst Write



Single Write



Read / Write Operation(cont.)

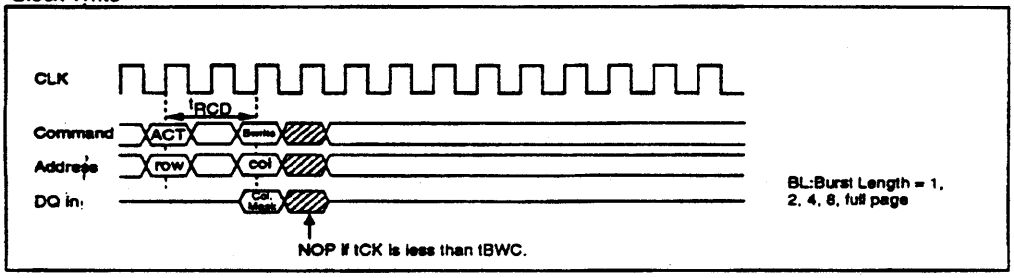
.Block Write & Write per bit Function
The HM5283206 has two graphic functions, Block write and write per bit, such as conventional VRAM has.

Block write operation:
This command enables 8 column write at one CAS cycle with the data stored in color register(32 bit). The column block composed of 8 columns is defined by AX3-AX7 loaded through A0-A7 pins when this command is issued. A0-A2 address is ignored then.
This command is executed regardless of burst length.
When this command is issued, DQ data are referred to stop writing color data to specific columns(see "column address mask data "on the next page).

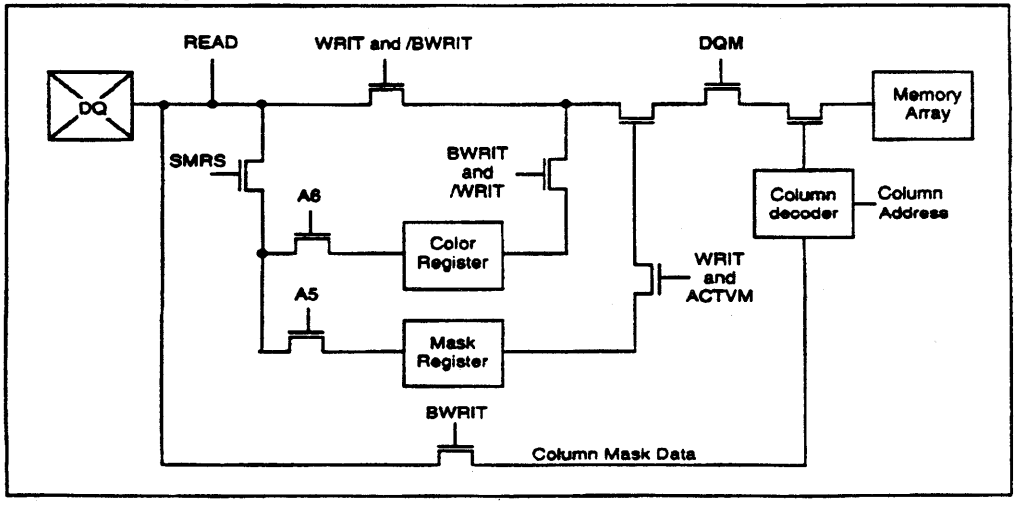
Write per bit operation:
Both for normal write and block write, additional DQ control function or write per bit function is available in the ACTVM state. The HM5283206 has the mask register(32bit). This register indicates DQ bits which will be masked through both normal write(DSF=0) and block write(DSF=1).Hence, mask register and DQM signal determine DQ bits which should be masked.

The figure at the top of the next page shows an example of block write with mask.

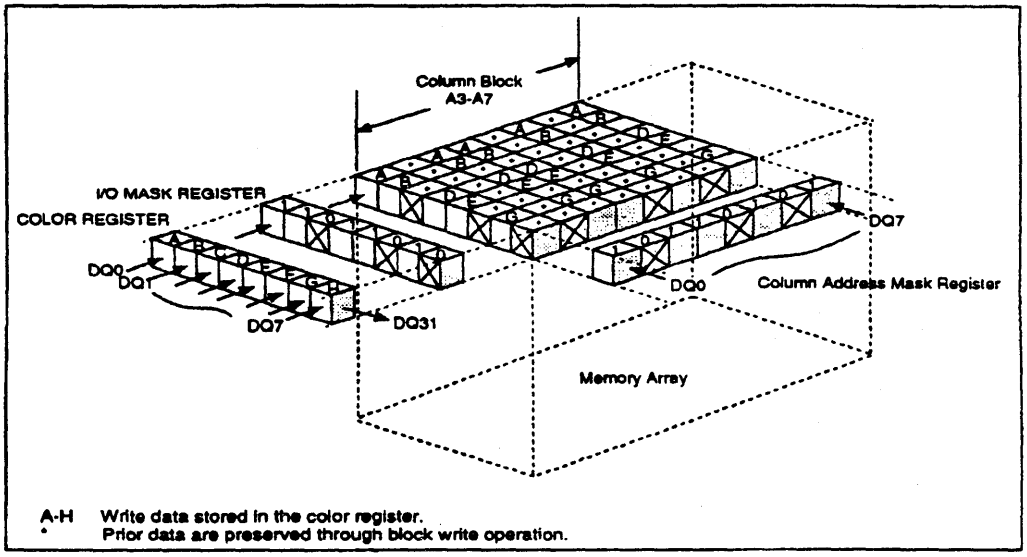
Block Write



Block diagram of graphic functions



Block write and write per bit



A-H Write data stored in the color register.
* Prior data are preserved through block write operation.

Column Address Mask Data

DQ ix8+0	Column 0 (A0=0, A1=0, A2=0) Mask Data	i_{in} Byte	Low : Mask High : Non Mask
DQ ix8+1	Column 1 (A0=1, A1=0, A2=0) Mask Data		
DQ ix8+2	Column 2 (A0=0, A1=1, A2=0) Mask Data		
DQ ix8+3	Column 3 (A0=1, A1=1, A2=0) Mask Data		
DQ ix8+4	Column 4 (A0=0, A1=0, A2=1) Mask Data		
DQ ix8+5	Column 5 (A0=1, A1=0, A2=1) Mask Data		
DQ ix8+6	Column 6 (A0=0, A1=1, A2=1) Mask Data		
DQ ix8+7	Column 7 (A0=1, A1=1, A2=1) Mask Data		

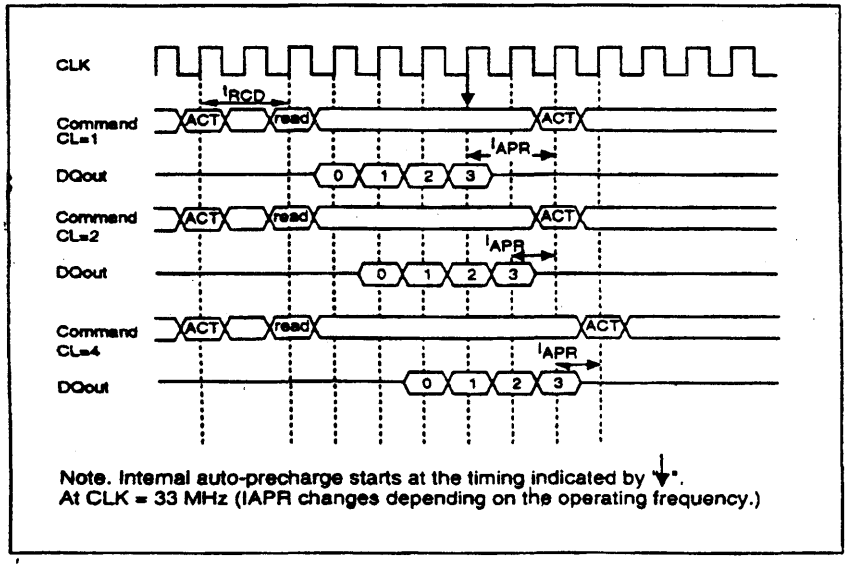
i={0,1,2,3}

Read / Write operation

.Read with auto precharge: In this operation, since precharge is automatically performed after completing a read operation, so no precharge commands are necessary after each read operation.

The command next to this command must be the bank active(ACTV, ACTVM) command. In addition, an interval defined by IAPR is required before execution of the next command.

/CAS latency	Precharge start cycle
3	2 cycle before the last data out
2	1cycle before the last data out
1	1 cycle before the last data out



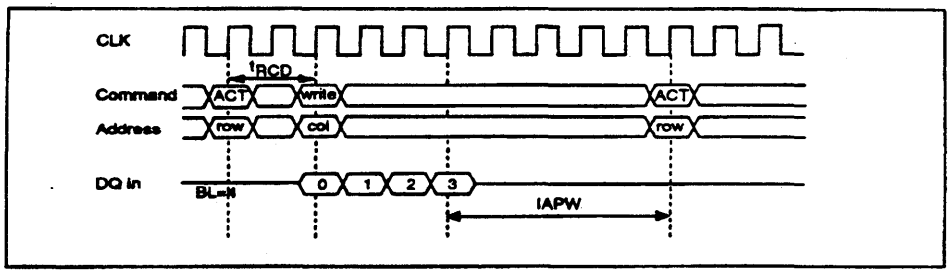
Note. Internal auto-precharge starts at the timing indicated by ▼.
At CLK = 33 MHz (IAPR changes depending on the operating frequency.)

Read /write operation(cont.)

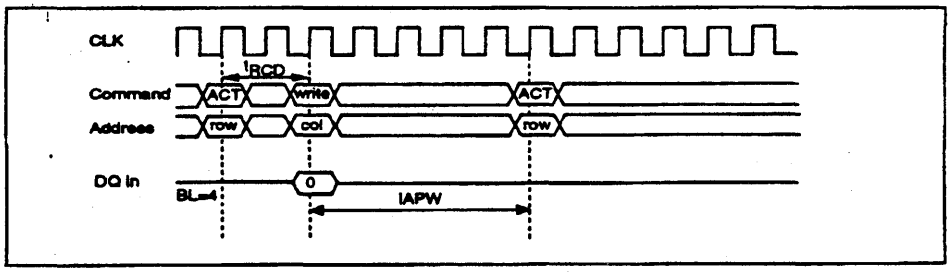
.Write with auto-precharge: In this operation, since precharge is automatically performed after completing burst write or single write operation, so no precharge commands are necessary after each write operation.

The command next to this command must be the bank active(ACTV, ACTVM) command. In addition, an interval of tAPW is required between the last valid data input and the next command.

Burst Write(Burst Length = 4)

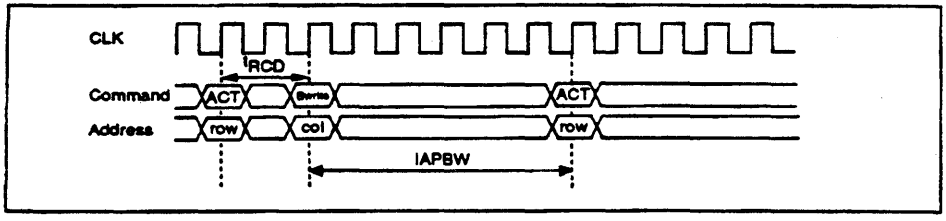


Single Write



Read /write operation(cont.)

.Block write with auto-precharge: In this operation, since precharge is automatically performed after completing block write operation, so no need to execute any precharge command. The command next to this command must be the bank active(ACTV, ACTVM)command. In addition, an interval of tAPBW is required between the last valid data and the next command.



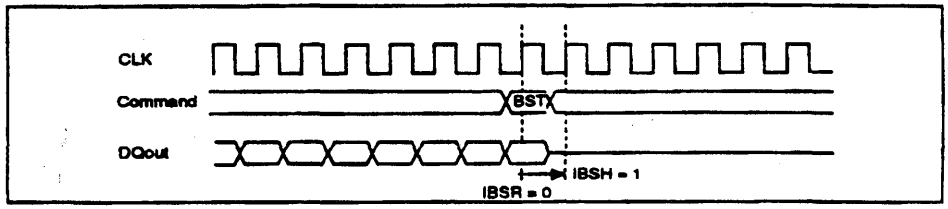
Full page burst stop

. Burst stop command during burst read:
The burst command is used to stop data output during a full-page burst. The BST command sets the output buffer to high-Z and stops the full-page burst read.

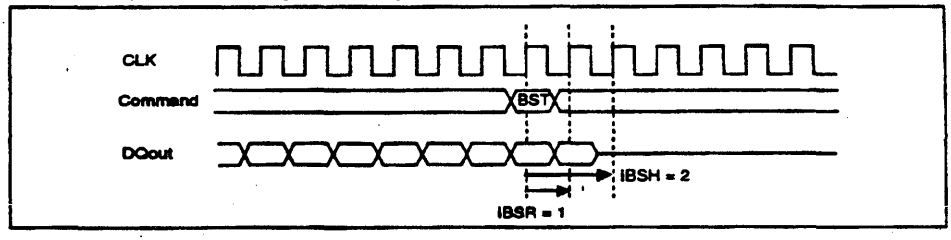
The timing, from command input to the last data, depends on the /CAS latency. When the /CAS latency is 3, the data, two cycles after the BST command, becomes invalid . The BST command is legitimate only in case full page burst mode, and is illegal in case burst length 1, 2, 4 and 8.

/CAS latency	BST to valid data	BST to high impedance
1	0	1
2	1	2
3	1	3

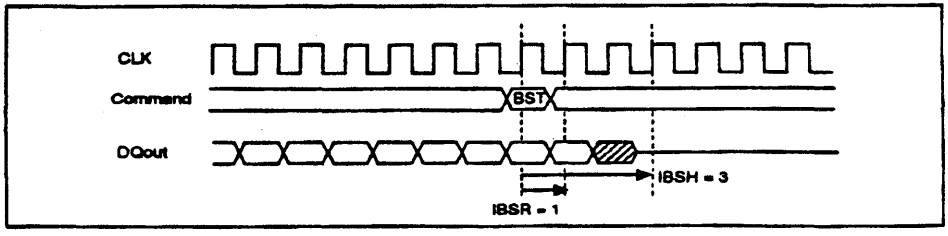
/CAS Latency = 1, Burst Length = full page



/CAS Latency = 2, Burst Length = full page



/CAS Latency = 3, Burst Length = full page

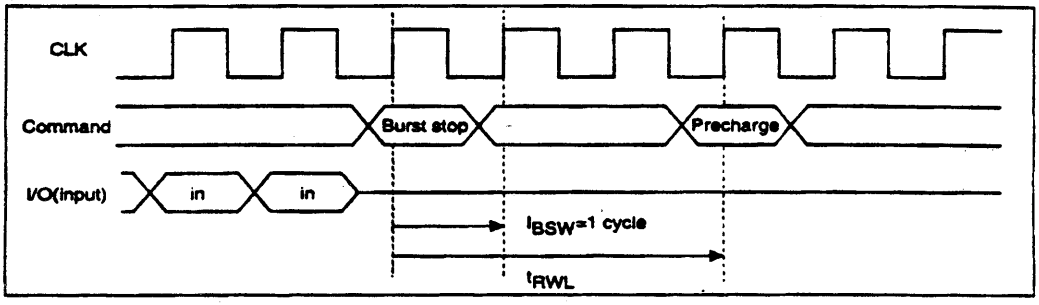


Full-page Burst Stop(cont.)

·Burst stop command at burst write:
For full page burst write cycle, when burst stop command is issued, write data at that cycle and the following write data input are ignored.

The BST command is legitimate only in case full page burst mode, and is illegal for burst length 1, 2, 4 and 8. An interval tRWL is required between the BST command and the next precharge command.

Burst Length = full page

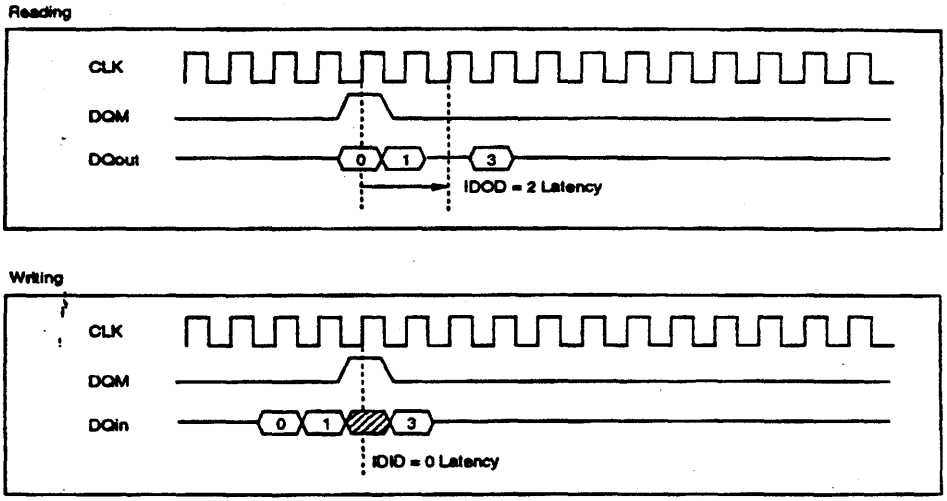


DQM control

The DQM i(i=0, 1, 2, 3) controls the ith byte of DQ data. DQM control operation for read and for write are different in terms of operation timing.

Reading: When data is read, output buffer can be controlled by DQMi.
By setting DQMi to low, corresponding DQ output buffer becomes active. By setting DQMi to high, the DQ output buffer is getting floated so that the ith byte of data are not driven out. The latency of DQM operation for read operation is two.

Writing: Input data can be controlled by DQMi. While DQMi is low, data is driven into the HM5283206. By setting DQMi to low, corresponding ith byte of DQ input data are kept from being written to the HM5283206 and the previous data are protected. The latency of DQM control operation is 0.



Refresh

.Auto-refresh

All the banks must be precharged before executing an auto-refresh command. Since the auto refresh command updates the interval counter every time when it is executed. This command also determines the bank and the ROW to be refreshed. Therefore external address specification is not necessary. The refresh cycle is 1024 cycles/16ms. (1024 cycles are required to refresh all the ROW addresses.) The output buffer becomes high-Z after auto-refresh start. no prechrage commands are not necessary after this command execution.

.Self-refresh

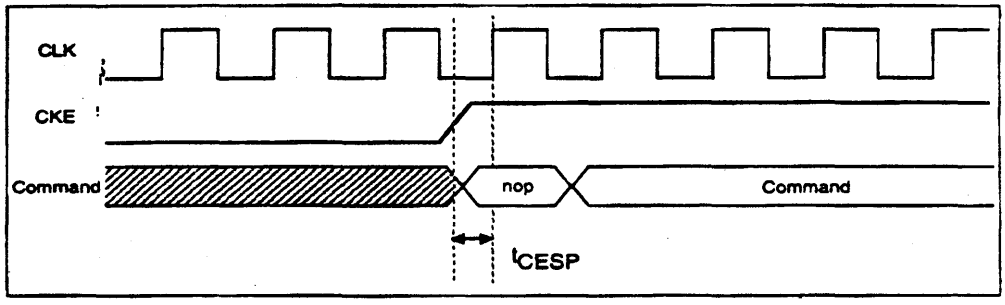
After issuing the self refresh command, self refresh operation starts by changing the level on CKE pin from 'H' to 'L'. During self-refresh operation, all data are refreshed. This operation managed by the internal refresh timer. After the self refresh, since the last ROW refreshed cannot be determined, an auto-refresh should immediately be performed for all addresses(1024 cycles).

Others

.Power down mode and clock mask

Power down mode is a state in which input buffers are made inactive and clock signal is masked to cut power dissipation. To enter into power down mode, CKE should be set to low.

Power down mode is kept as long as CKE is low. Note that during burst read or burst, only clock signal is masked. To exit from power down or clock mask state , CKE should be set to high as the timing shown bellow.



.Clock suspend mode

By driving CKE to low during a bank-active or read/write operation, the HM5283206 enters into clock suspend mode. During clock suspend mode external input signals are ignored and the internal state is maintained. When CKE is driven high, the synchronous DRAM terminates clock suspend mode, and command can be input from the next cycle. For detail, refer to the "CKE Truth Table".

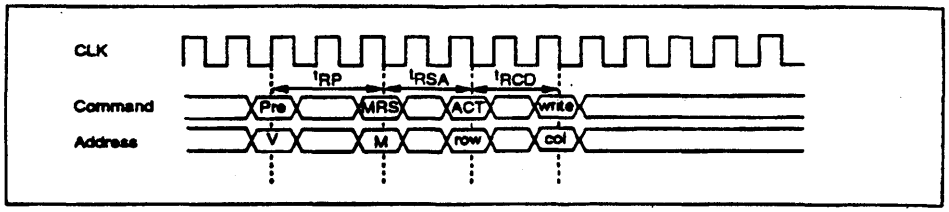
.Power-up sequence

During power-up sequence, the DQMi and the CKE must be set to high. When 100μs has past after power-on, all banks must be precharged using the precharge command. After tRSA delay, execute two auto-refresh commands as dummy, an interval of tRC is necessary between two auto-refresh commands.

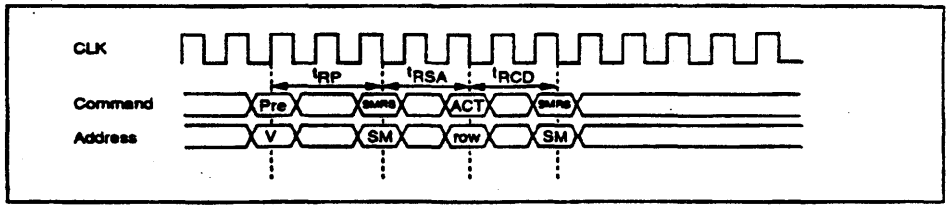
Mode Register Set:
Mode register are set through address pins during the IDLE state. A9 and A8 bits are used to define OPCODE determines write type. A7 bit isn't used and must be low level. A4 to A6 bits are used to specify LMODE or CAS latency. A3 bits is used to deefine BL or burst length. See " Mode register configuration" in the next page.

Special Mode Register Set:
Special mode register are set through address pins during the IDLE, ACTV or ACTVM state. A6 and A5 pins are used to determine whether loading color data or mask data. Other pins should be low. When special mode register set command is issued, if both A5 and A6 are equal to 1, then neither color nor mask data is assured. See "Special mode register configuration" in the next page.

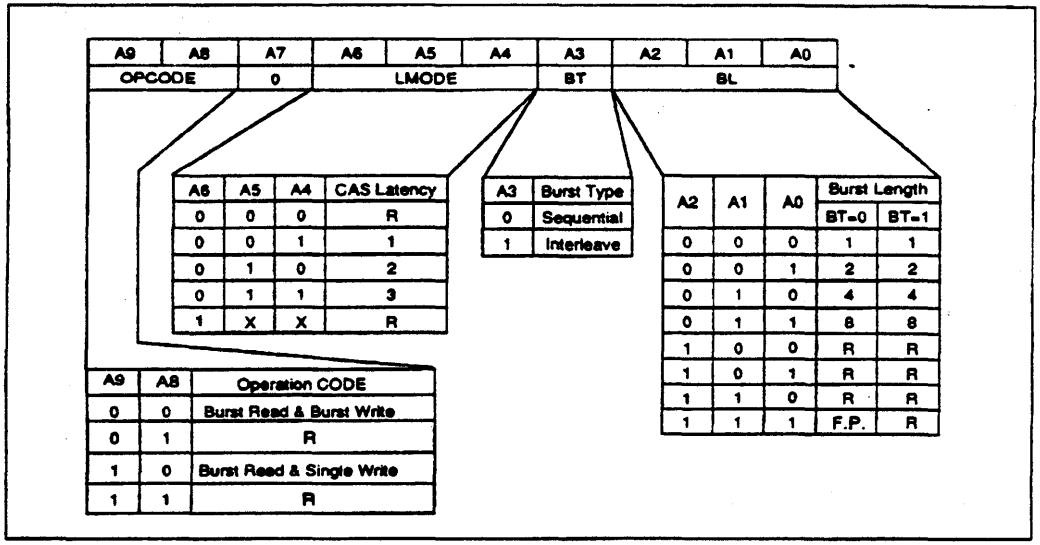
Mode register set



Special mode register set



Mode register configuration



A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
OPCODE		0	LMODE			BT	BL		

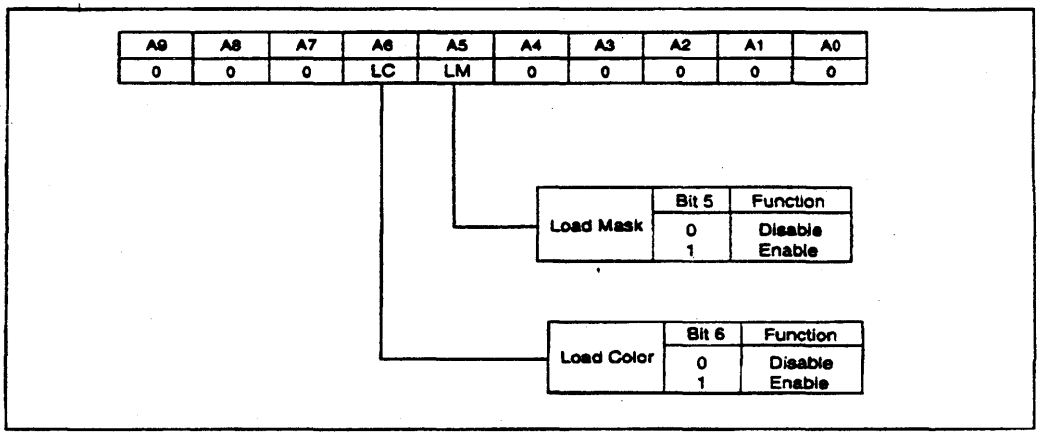
A6	A5	A4	CAS Latency
0	0	0	R
0	0	1	1
0	1	0	2
0	1	1	3
1	X	X	R

A3	Burst Type
0	Sequential
1	Interleave

A2	A1	A0	Burst Length	
			BT=0	BT=1
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	R	R
1	0	1	R	R
1	1	0	R	R
1	1	1	F.P.	R

A9	A8	Operation CODE
0	0	Burst Read & Burst Write
0	1	R
1	0	Burst Read & Single Write
1	1	R

Special mode register configuration



A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	LC	LM	0	0	0	0	0

Load Mask	Bit 5	Function
	0	Disable
	1	Enable

Load Color	Bit 6	Function
	0	Disable
	1	Enable

Burst Sequence

Burst length = 2

Stating Ad.	Addressing(decimal)	
A0	Sequence	Interleave
0	0, 1,	0, 1,
1	1, 0,	1, 0,

Burst length = 4

Stating Ad.		Addressing(decimal)	
A1	A0	Sequence	Interleave
0	0	0, 1, 2, 3,	0, 1, 2, 3,
0	1	1, 2, 3, 0,	1, 0, 3, 2,
1	0	2, 3, 0, 1,	2, 3, 0, 1,
1	1	3, 0, 1, 2,	3, 2, 1, 0,

Burst length = 8

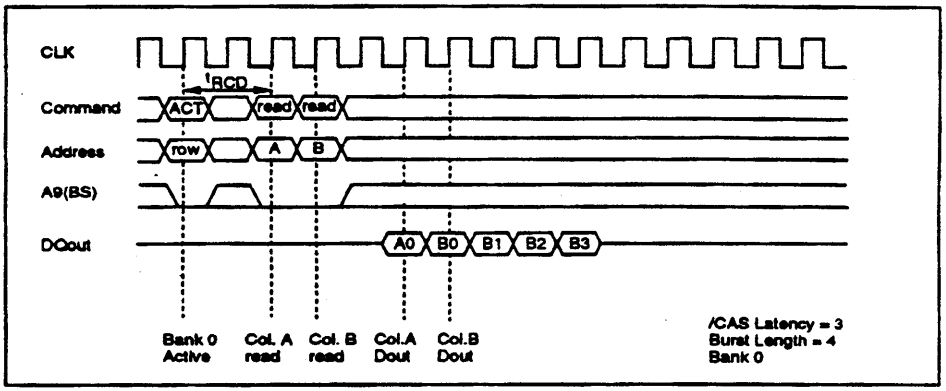
Stating Ad.			Addressing(decimal)	
A2	A1	A0	Sequence	Interleave
0	0	0	0, 1, 2, 3, 4, 5, 6, 7,	0, 1, 2, 3, 4, 5, 6, 7,
0	0	1	1, 2, 3, 4, 5, 6, 7, 0,	1, 0, 3, 2, 5, 4, 7, 6,
0	1	0	2, 3, 4, 5, 6, 7, 0, 1,	2, 3, 0, 1, 6, 7, 4, 5,
0	1	1	3, 4, 5, 6, 7, 0, 1, 2,	3, 2, 1, 0, 7, 6, 5, 4,
1	0	0	4, 5, 6, 7, 0, 1, 2, 3,	4, 5, 6, 7, 0, 1, 2, 3,
1	0	1	5, 6, 7, 0, 1, 2, 3, 4,	5, 4, 7, 6, 1, 0, 3, 2,
1	1	0	6, 7, 0, 1, 2, 3, 4, 5,	6, 7, 4, 5, 2, 3, 0, 1,
1	1	1	7, 0, 1, 2, 3, 4, 5, 6,	7, 6, 5, 4, 3, 2, 1, 0,

Command intervals

.Read command to read command interval

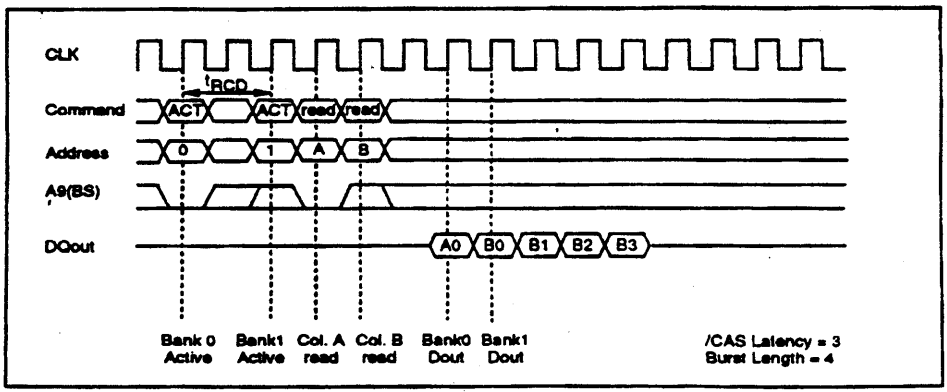
(1) Operation for the column in the same row (page): Within the same ROW (page), read command can be issued every cycle.

Note that the last read command has the priority to the preceding read command, that is, any read command can interrupt the preceding burst read operation to get valid data aimed by this interruption.



(2) Operation for the column in other ROW of the same bank: To read the data of other ROW of the same bank, it is necessary to execute a precharge command and a bank-active command before executing next read command.

(3) Operation for another bank: For another bank in active state, burst read command can be executed from the next cycle after the preceding read command is issued. If another bank is in the idle state, bank active command should be executed prior to the read command.

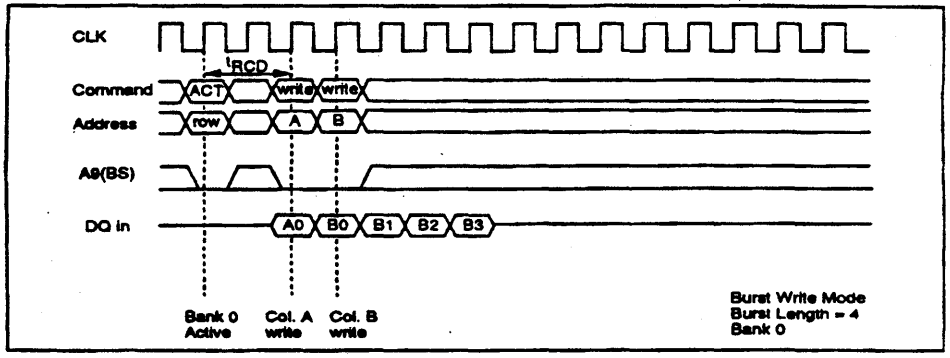


Command intervals(cont.)

.Write command to write command interval

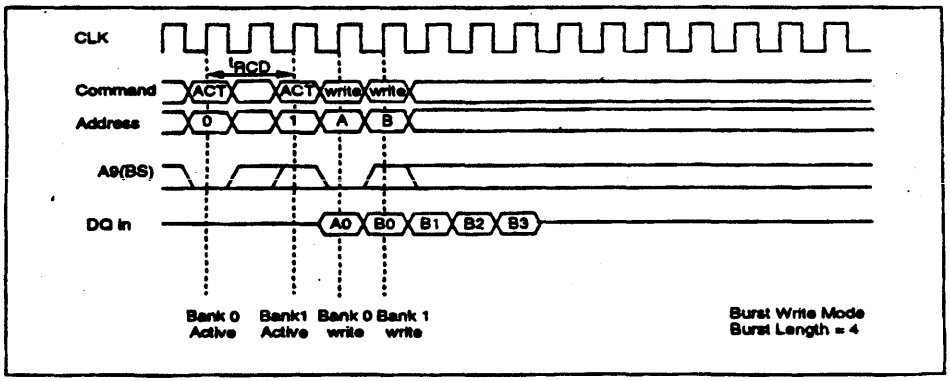
(1) Operation for the column in the same row : Within the same ROW (page), write command can be issued every cycle.

Note that the last write command has the priority to the preceding write command, that is, any write command can interrupt the preceding burst write operation to get valid data



(2) Operation for the column in other ROW of the same bank: To write data on other row of the same bank, it is necessary to execute a precharge command and bank active command before executing next write command.

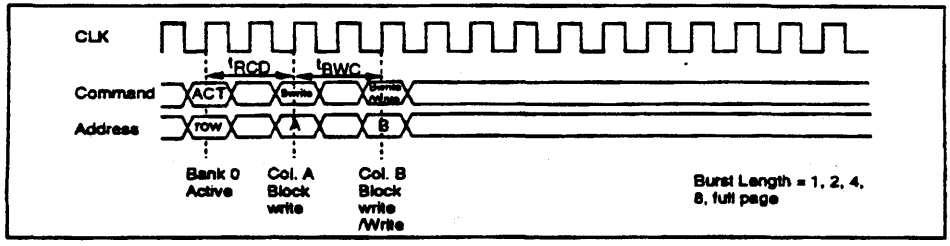
(3) Operation for another bank: For another bank in active state, burst write command can be executed from the next cycle after the preceding write command is issued. If another bank is in the idle state, bank active command should be executed.



Command intervals(cont.)

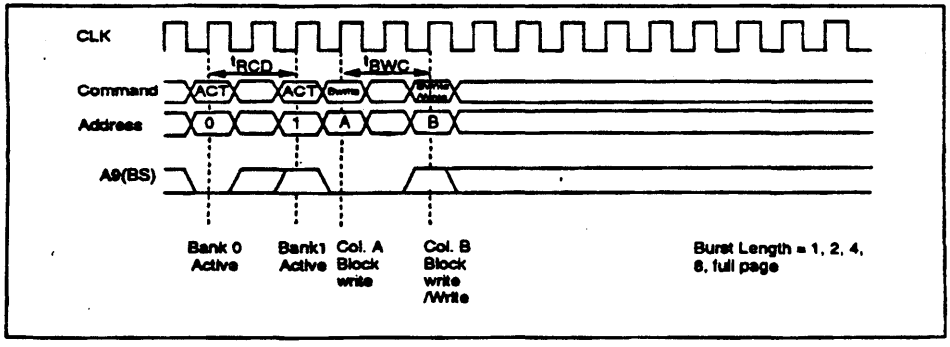
.Block Write command to write or block write command interval

(1) Operation for the column in the same row : Within the same ROW (page), it is necessary to take no less than tBWC between block write and another block write/normal write. If tCK is less than tBWC, NOP command should be issued for the cycle between the block write command and the following write or block write command.



(2) Operation for the column in other ROW of the same bank: To execute write command or another block write command for other row of the same bank, it is necessary to execute a precharge command and bank active command before write or block write operation.

(3) Operation for another bank: To execute write command or another block write command for another bank in active state, tBWC interval to the next command is necessary. If another bank is in the idle state, bank active command should be executed. If tCK is less than tBWC, NOP command should be issued for the cycle between the block write command and the following write or block write command.

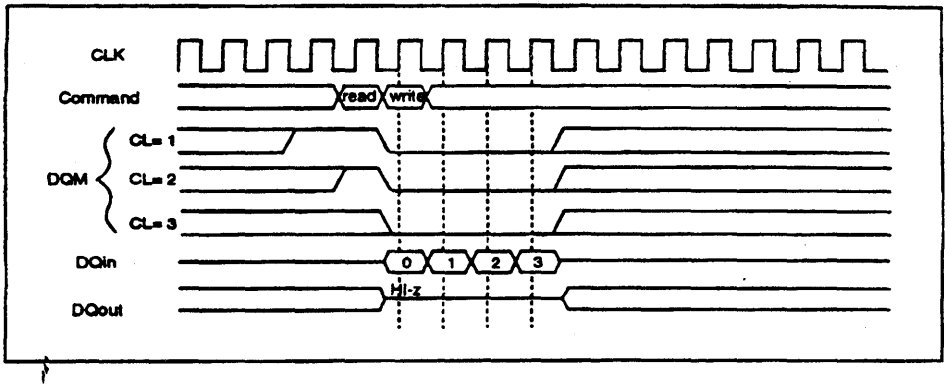


Command intervals(cont.)

.Read command to write or block write command interval

(1) Operation for the column in the same ROW: The write or block write command following the preceding read command can be performed after an interval of no less than 1 cycle. To set DQ output High-Z when data are driven in, DQM must be used depending on cas latency as the timing shown below.

Note that the last write or block write command has the priority to the preceding read command, that is, any write or block write command can interrupt the preceding burst read operation to get valid data.



(2) Operation for the column in other ROW of the same bank: To execute write or block write for other row of the same bank, it is necessary to execute a precharge command and bank active command before executing these commands.

(3) Operation for another bank: For another bank in active state, burst write command can be executed from the next cycle after the preceding write command is issued. If another bank is in the idle state, bank active command should be executed.

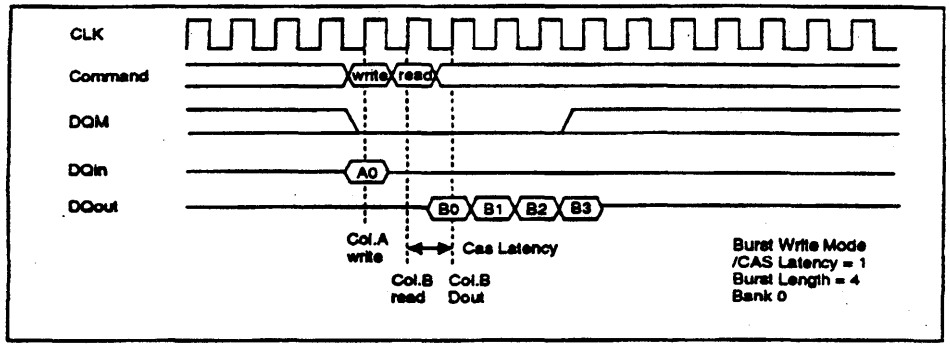
Command intervals(cont.)

.Write command to read command interval

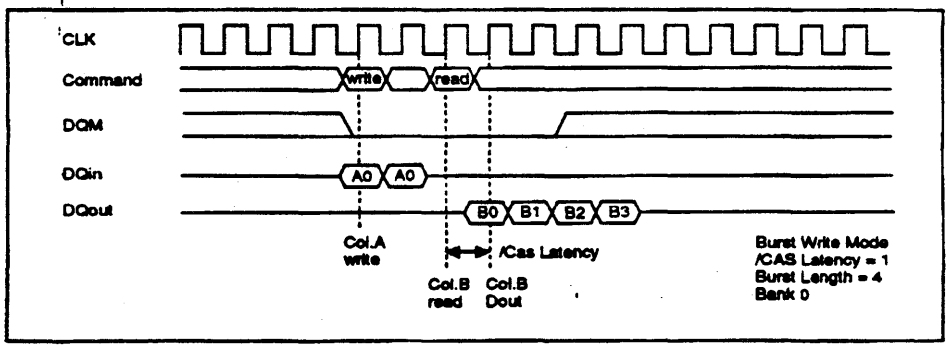
(1) Operation for the column in the same ROW: The read command following the preceding write command can be performed after an interval of no less than 1cycle.

Note that the last read command has the priority to the preceding writing command, that is, any read command can interrupt the preceding burst write operation to get valid data.

WRITE to READ Command Interval (1)



WRITE to READ Command Interval (2)



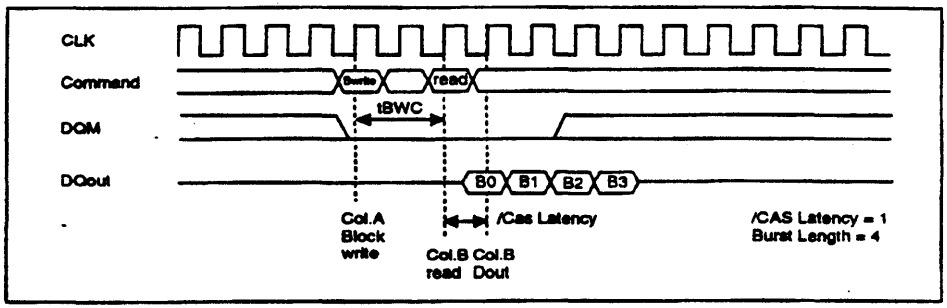
(2) Operation for the column in other ROW of the same bank: To execute read command for other row of the same bank, it is necessary to execute a precharge command and bank active command.

(3) Operation for another bank: For another bank in active state, burst read command can be executed from the next cycle after the preceding write command is issued. If another bank is in the idle state, bank active command should be executed prior to execute these command.

Command intervals(cont.)

.Block Write command to read command interval

(1) Operation for the column in the same row : Within the same ROW (page), It is necessary to take no less than tBWC between block write and the following read command. If tCK is less than tBWC, NOP command should be issued for the cycle between the block write command and the following read command.



(2) Operation for the column in other ROW of the same bank: To execute read command for other row of the same bank, It is necessary to execute a precharge command and bank active command before write or block write operation.

(3) Operation for another bank: To execute read command for another bank in active state, tBWC interval to the next command is necessary. If another bank is in the idle state, bank active command should be executed. If tCK is less than tBWC, NOP command should be issued for the cycle between the block write command and the following read command.

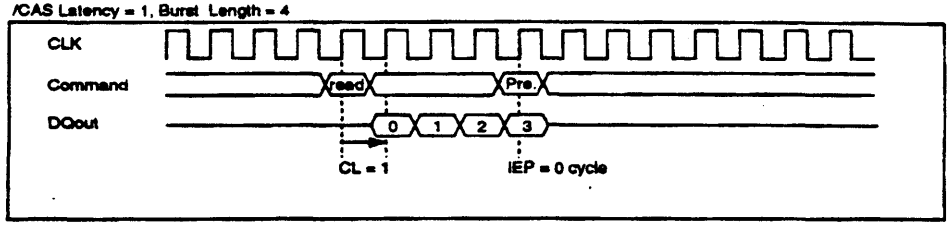
Command intervals(cont.)

.Read command to precharge command

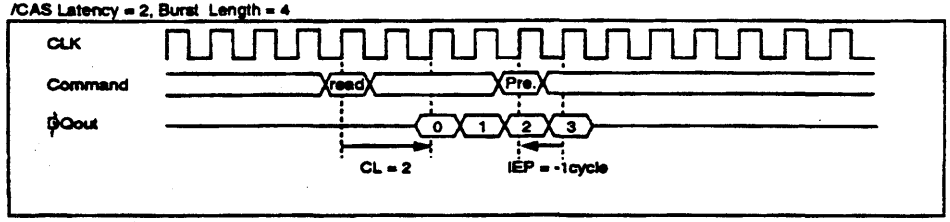
The minimum interval between read command and precharge command is one cycle. However, since the output buffer then becomes high-Z after the cycles defined by IHZP, there is a possibility that burst read data output will be interrupted, if the precharge command is input during burst read. To read all data by burst read, the cycles defined by IEP must be assured as an interval from the final data output to precharge command execution.

.READ to PRECHARGE Command Interval (same bank): To output all data

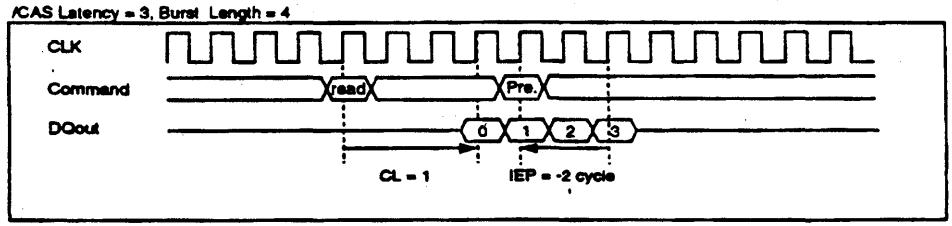
/CAS Latency = 1, Burst Length = 4



/CAS Latency = 2, Burst Length = 4



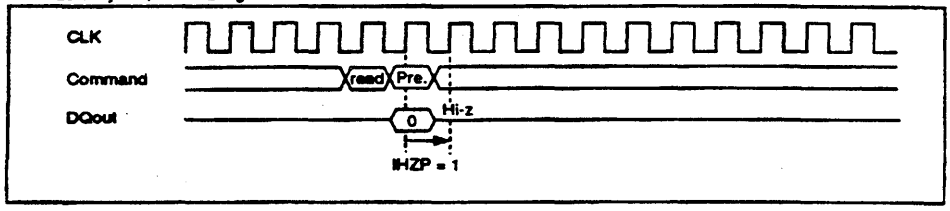
/CAS Latency = 3, Burst Length = 4



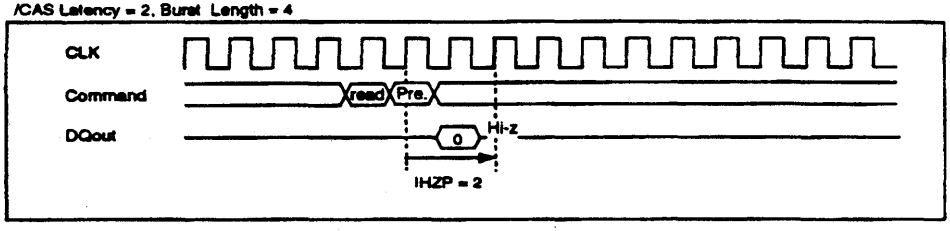
Command Intervals(cont.)

READ to PRECHARGE Command Interval (same baank): To stop output data

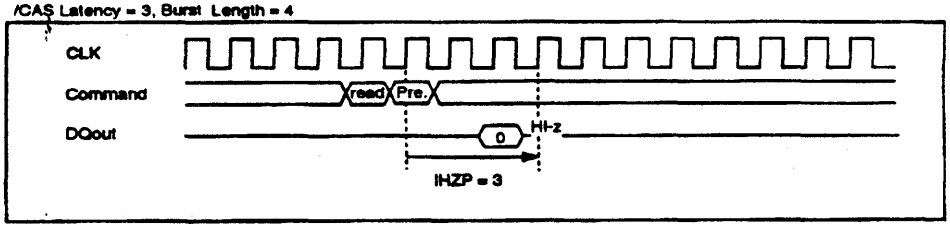
/CAS Latency = 1, Burst Length = 4



/CAS Latency = 2, Burst Length = 4



/CAS Latency = 3, Burst Length = 4



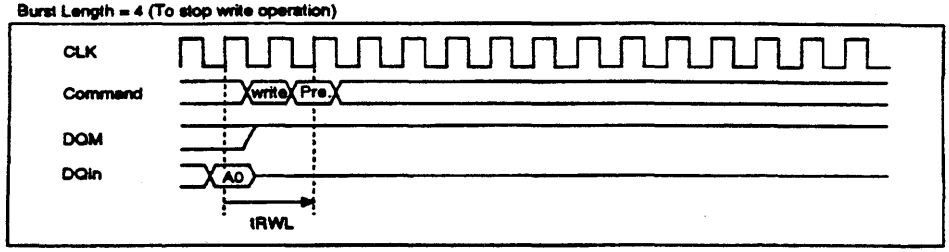
Command intervals(cont.)

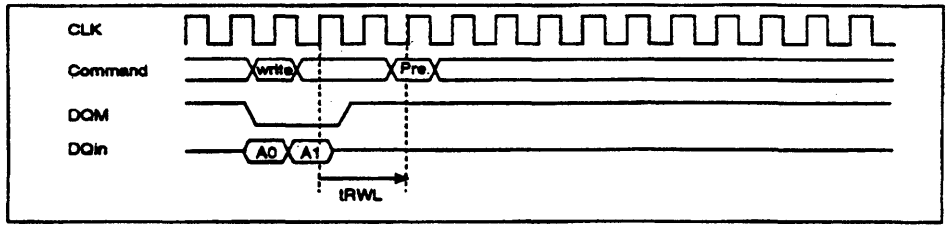
.Write command to precharge command:
The minimum interval between write command and precharge command.

However, if the burst write operation is unfinished, the input must be masked by means of DQM for assurance of the cycle defined by tRWL.

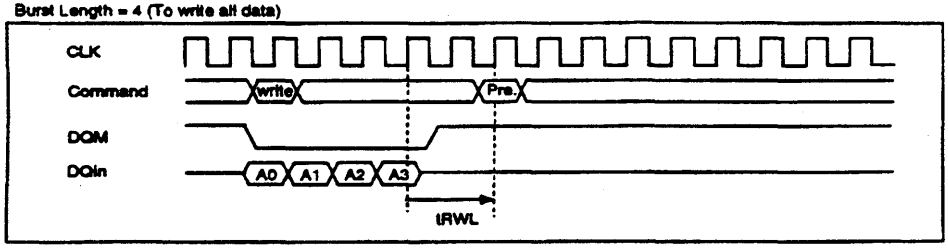
WRITE to Precharge Command Interval (same bank)

Burst Length = 4 (To stop write operation)





Burst Length = 4 (To write all data)

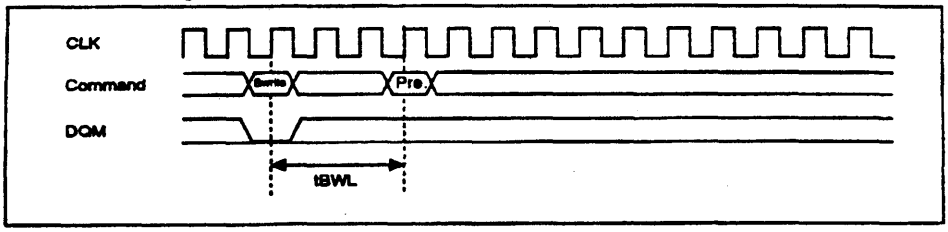


Command intervals(cont.)

.Block write command to precharge command interval:

The minimum interval between block write command and precharge command is tBWL.

WRITE to Precharge Command Interval (same bank)

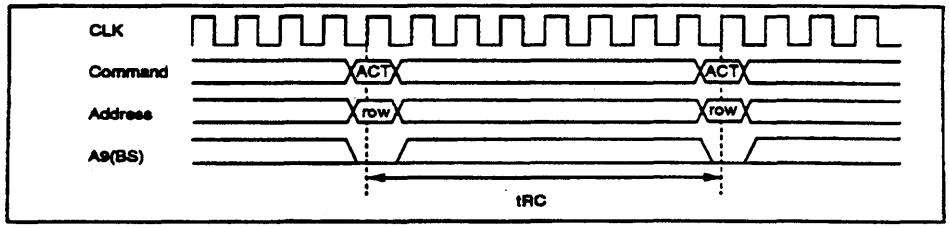


Command intervals(cont.)

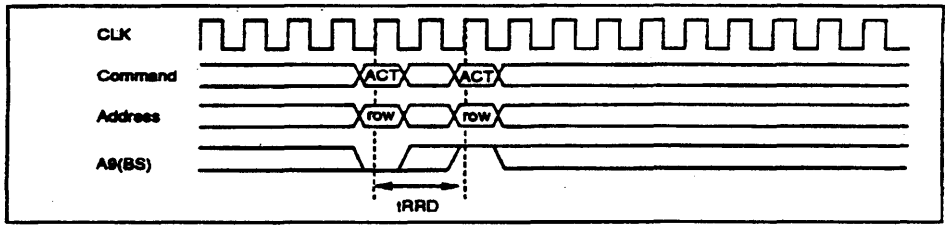
.Bank active command interval
(1) Same bank: The interval between the two bank-active commands must be no less than tRC.

(2) In the case of different bank-active commands: The interval between two bank-active commands must be no less than tRRD.

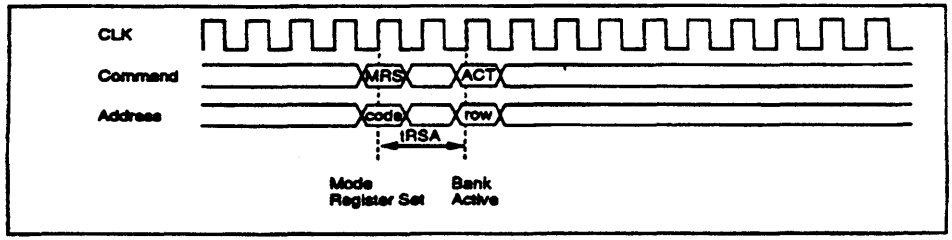
Bank active to bank active for same bank



Bank active to bank active for different bank



.Mode register set to bank-active command interval: The interval between setting the mode register and executing a bank-active command must be no less than tRSA.



DC Characteristics(Ta=0 to 70°C,Vcc=3.3V,Vss=0V)

Parameter	Symbol	HM5283206 -12 Min	HM5283206 -12 Max	HM5283206 -15 Min	HM5283206 -15 Max	HM5283206 -17 Min	HM5283206 -17 Max	HM5283206 -20 Min	HM5283206 -20 Max	Unit	Test Conditions	Notes
Operating current	Icc1	—	TBD	—	TBD	—	TBD	—	TBD	mA	Burst length=1 tRC=min	1
Standby current	Icc2	—	TBD	—	TBD	—	TBD	—	TBD	mA	CKE=VIL,tCK=min	
(Bank Disable)		—	TBD	—	TBD	—	TBD	—	TBD	mA	CKE=VIL CKE=VIL or VIH fixed	
		—	TBD	—	TBD	—	TBD	—	TBD	mA	CKE=VIH, NOP com. tCK=min	
Active standby current	Icc3	—	TBD	—	TBD	—	TBD	—	TBD	mA	CKE=VIL, tCK=min DQ=High-Z	1
(Bank actine)		—	TBD	—	TBD	—	TBD	—	TBD	mA	CKE=VIH, NOP com. tCK=min, DQ=High-Z	
Burst operating(CL=1) current (CL=2) (CL=3)	Icc4	—	TBD	—	TBD	—	TBD	—	TBD	mA	tCK=min	1
Refresh current	Icc5	—	TBD	—	TBD	—	TBD	—	TBD	mA	tRC=min	
Self refresh current	Icc6	—	2	—	2	—	2	—	2	mA	VIH≥Vcc-0.2 VIL≤0.2	
Input leakage current	ILI	-10	10	-10	10	-10	10	-10	10	uA	0≤Vin≤Vcc	
Output leakage current	ILO	-10	10	-10	10	-10	10	-10	10	uA	0≤Vout≤Vcc DQ=disable	
Output high voltage	VOH	2.4	—	2.4	—	2.4	—	2.4	—	V	IOH=-2mA	
Output low voltage	VOL	—	0.4	—	0.4	—	0.4	—	0.4	V	IOL=2mA	

Note 1: Icc depends on output load condition when the device is selected. Icc max is specified on condition that all output pins are floated.

Capacitance

parameter	Symbol	Typ.	Max.	Unit	Notes
Input capacitance(Address)	CI1	—	5	pF	1
Input capacitance(Signals)	CI2	—	5	pF	1
Output capacitance(DQ)	CO	—	7	pF	1,2

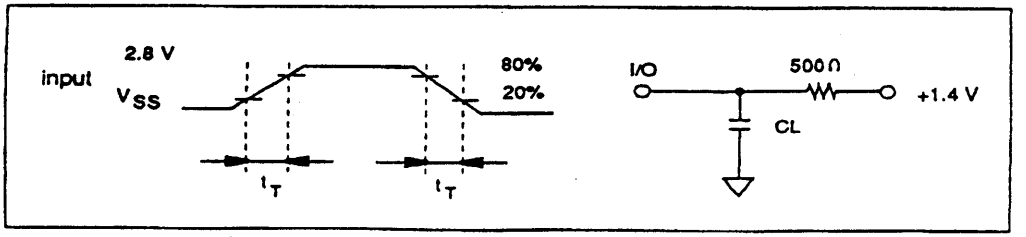
Note.1. Capacitance measured with Booton Meter or effective capacitance measuring method.
2. DQM=VIH to disable Dout

AC Characteristics(Ta=0 to 70°C,Vcc=3.3V,Vss=0V)

Parameter	Symbol	HM5283206 -12 Min	HM5283206 -12 Max	HM5283206 -15 Min	HM5283206 -15 Max	HM5283206 -17 Min	HM5283206 -17 Max	HM5283206 -20 Min	HM5283206 -20 Max	Unit	Notes
Active to precharge on full page mode	tRASC	—	80000	—	80000	—	80000	—	80000	ns	1
Active command to column command (same bank)	tRCD	25	—	30	—	35	—	40	—	ns	1
Precharge to active command period	tRP	34	—	34	—	34	—	40	—	ns	1
The last data-in to precharge lead time	tRWL	25	—	30	—	35	—	40	—	ns	1
Active(a) to active(b) command period	tRRD	25	—	30	—	35	—	40	—	ns	1
Register set to active command	tRSA	25	—	30	—	35	—	40	—	ns	1
Block write cycle time	tBWC	25	—	30	—	35	—	40	—	ns	1
Transition time(rise to fall)	tT	1	5	1	5	1	5	1	5	ns	
Refresh period	tREF	—	16	—	16	—	16	—	16	ms	

Notes: 1.AC measurement assumes tT=1ns. Reference level for timing input signals IS 1.4V.
2.Access time is measured at 1.4V. Load condition is CL=50pF with current source.
3.tHz(max)defines the time at which the outputs achieves ±200mV.
Load condition is CL=5pF with current source.
4.An initial pause of 100 us is required after power up followed by a mode resister set cycle and minimum of eight initialization cycles. (Auto refresh cycles or row active precharge command.)
5.If tT is longer than 1 ns, input timing referred level should be VIH(min)/VIL(max)and 1ns should be subtracted parameter.
6.tCES define CKE setup time to CKE rising edge except power down exit command.

HM5283206 (LVTTL)



AC Characteristics(Ta=0 to 70°C,Vcc=3.3V,Vss=0V)

Parameter		Symbol	HM5283206 -12 Min	HM5283206 -12 Max	HM5283206 -15 Min	HM5283206 -15 Max	HM5283206 -17 Min	HM5283206 -17 Max	HM5283206 -20 Min	HM5283206 -20 Max	Unit	Notes
System Clock	(CL=1)	tCK	25	—	30	—	35	—	40	—	ns	
	(CL=3)		12.5		15		17.5		20		ns	1
CLK high pulse width		tCKH	5	—	6	—	7	—	8	—	ns	1
CLK low pulse width		tCKL	5	—	6	—	7	—	8	—	ns	1
Access time from CLK	(CL=1)	tAC	—	24	—	30	—	34	—	38	ns	1,2
	(CL=2)		—	12.5	—	15	—	16.5	—	18	ns	1,2
	(CL=3)		—	11.5	—	13	—	15.5	—	18	ns	1,2
Read command to data valid time	(CL=1)	tACK	—	25	—	30	—	34	—	38	ns	1
	(CL=2,3)		—	36	—	43	—	50.5	—	58	ns	1
Data-out hold time	(CL=1)	tOH	4	—	4	—	4	—	4	—	ns	1,2
	(CL=2,3)		2	—	2	—	2	—	2	—	ns	
CLK to Data-out low impedance		tLZ	0	—	0	—	0	—	0	—	ns	1,2
CLK to Data-out high impedance		tHZ	4	12.5	4	15	4	17	4	19	ns	
			2	8	2	10	2	12	2	14	ns	1,3
Data-in setup time		tDS	4	—	4	—	4	—	4	—	ns	1
Data-in hold time		tDH	2	—	2	—	2	—	2	—	ns	1
Address setup time		tAS	4	—	4	—	4	—	4	—	ns	1
Address hold time		tAH	2	—	2	—	2	—	2	—	ns	1
CKE setup time		tCES	4	—	4	—	4	—	4	—	ns	1
CKE hold time		tCEH	2	—	2	—	2	—	2	—	ns	1
Command(/CS, /RAS, /CAS /WE, DQM, DSF)setup time		tCS	4	—	4	—	4	—	4	—	ns	1
Command(/CS, /RAS, /CAS /WE, DQM, DSF)hold time		tCH	2	—	2	—	2	—	2	—	ns	1
Ref/Active to Ref/active command period		tRC	100	—	110	—	120	—	130	—	ns	1
Active to precharge command period		tRAS	65	10000	70	10000	75	10000	80	10000	ns	1

Relationship Between Frequency and Minimum Latency

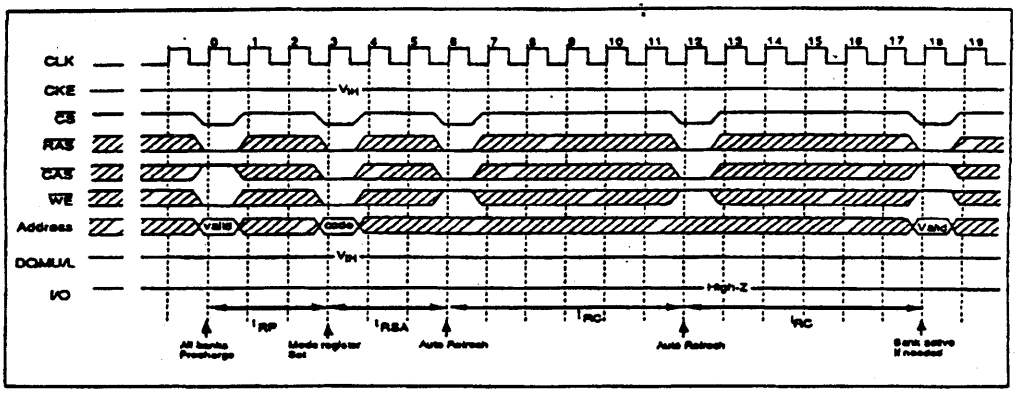
Parameter		HM5283206 -12		HM5283206 -15		HM5283206 -17		HM5283206 -20		
Frequency(MHz)		80	33	66	33	57	28.5	50	25	
tCK(ns)	Symbol	12.5	25	15	30	17.5	35	20	40	Notes
Active command to column Command(same bank)	tRCD	2	1	2	1	2	1	2	1	
Active command to active command(same bank)	tRC	8	4	8	4	7	4	7	4	=[tRAS+tRP]
Active command to precharge command(same bank)	tRAS	5	3	5	3	5	3	4	2	
Precharge command to active command(same bank)	tRP	3	2	3	2	2	1	2	1	
Last data in to active command (same bank)	tRWL	2	1	2	1	2	1	2	1	
Block write to precharge command (same bank)	tBWL	3	2	3	2	3	2	3	2	=[tRWL+1]
Active command to active command(different bank)	tRRD	2	1	2	1	2	1	2	1	
Last data in to active command (Auto precharge, same bank)	tAPW	5	3	5	3	4	2	4	2	=[tRWL+tRP]
Block write to active command (Auto precharge, same bank)	tAPBW	6	4	6	4	5	3	5	3	=[tBWL+tRP]
Self refresh exit to command input	tSEC	8	4	8	4	7	4	7	4	=tRC
Precharge command to high impedance	tHZP									
(CL=3)		3	3	3	3	3	3	3	3	
(CL=2)		2	2	2	2	2	2	2	2	
(CL=1)		—	1	—	1	—	1	—	1	
Last data out to active command	tAPR									
(CL=2,3)		2	1	2	1	1	0	1	0	=[tRP]-1
(CL=1)		—	2	—	2	—	1	—	1	=[tRP]
Last data out to precharge	tEP									
(CL=3)		-2	-2	-2	-2	-2	-2	-2	-2	
(CL=2)		-1	-1	-1	-1	-1	-1	-1	-1	
(early precharge) (CL=1)		—	0	—	0	—	0	—	0	
Column command to column command	tCCD	1	1	1	1	1	1	1	1	
Write command to data in latency	tWCD	0	0	0	0	0	0	0	0	
Block write cycle time	tBWC	2	1	2	1	2	1	2	1	

Relationship Between Frequency and Minimum Latency

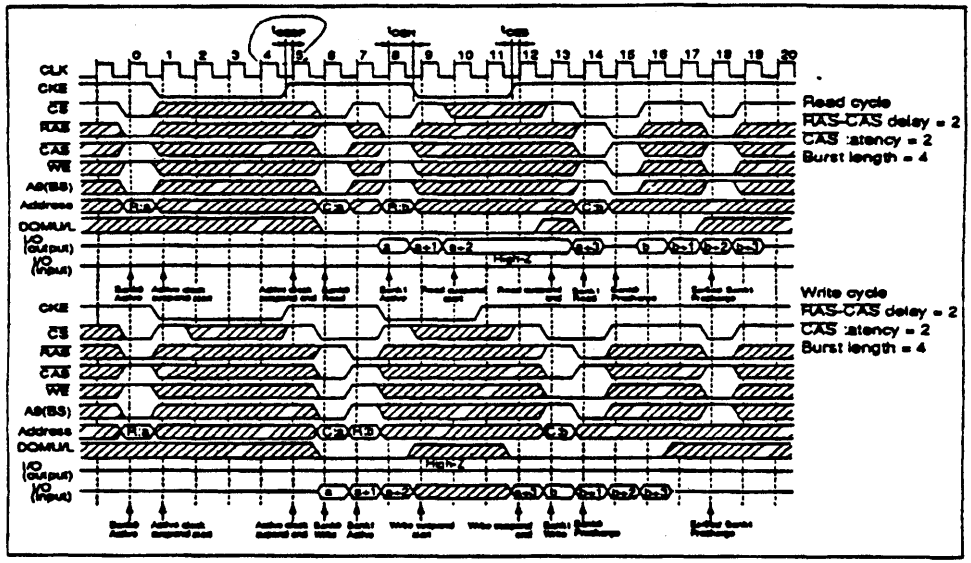
Parameter		HM5283206 -12		HM5283206 -15		HM5283206 -17		HM5283206 -20			
Frequency(MHz)		80	33	66	33	57	28.5	50	25		
tCK(ns)	Symbol	12.5	25	15	30	17.5	35	20	40	Unit	Notes
DQM to data in	IDID	0	0	0	0	0	0	0	0		
DQM to data out	IDOD	2	2	2	2	2	2	2	2		
CKE to CLK disable	ICLE	1	1	1	1	1	1	1	1		
Burst stop to output valid data hold	IBSR										
(CL=2,3)		—	0	—	0	—	0	—	0		
(CL=1)		1	1	1	1	1	1	1	1		
Burst stop to output high impedance	IBSH										
(CL=3)		—	1	—	1	—	1	—	1		
(CL=2)		2	2	2	2	2	2	2	2		
(CL=1)		3	3	3	3	3	3	3	3		
Burst stop to write data ignore	IBSW	0	0	0	0	0	0	0	0		

Note. CL=CAS latency

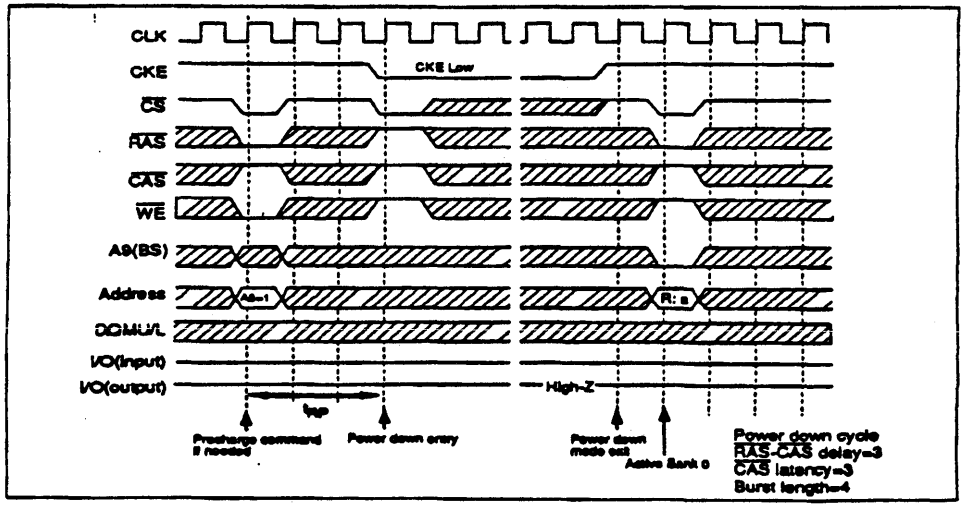
Power Up Sequence



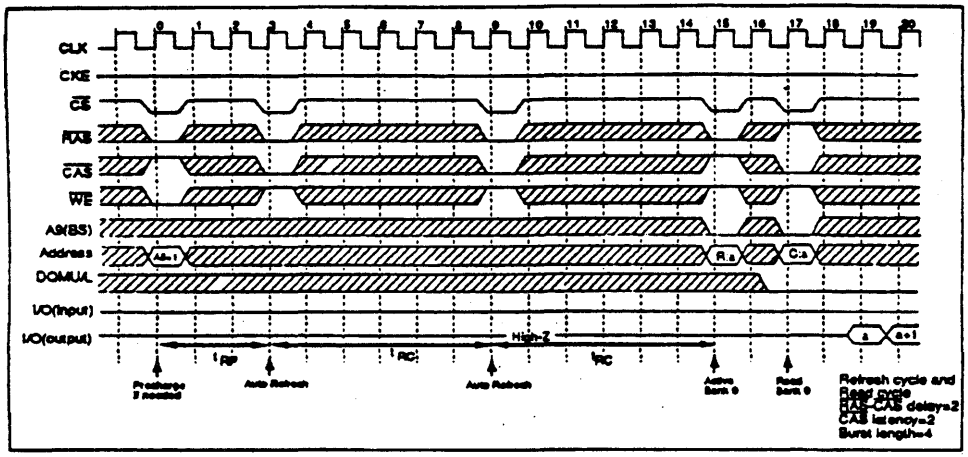
Clock Suspend Mode



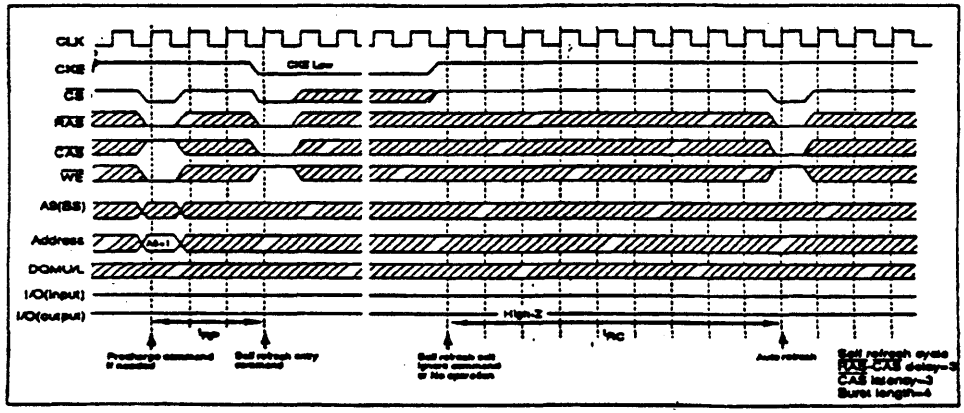
Power Down Mode



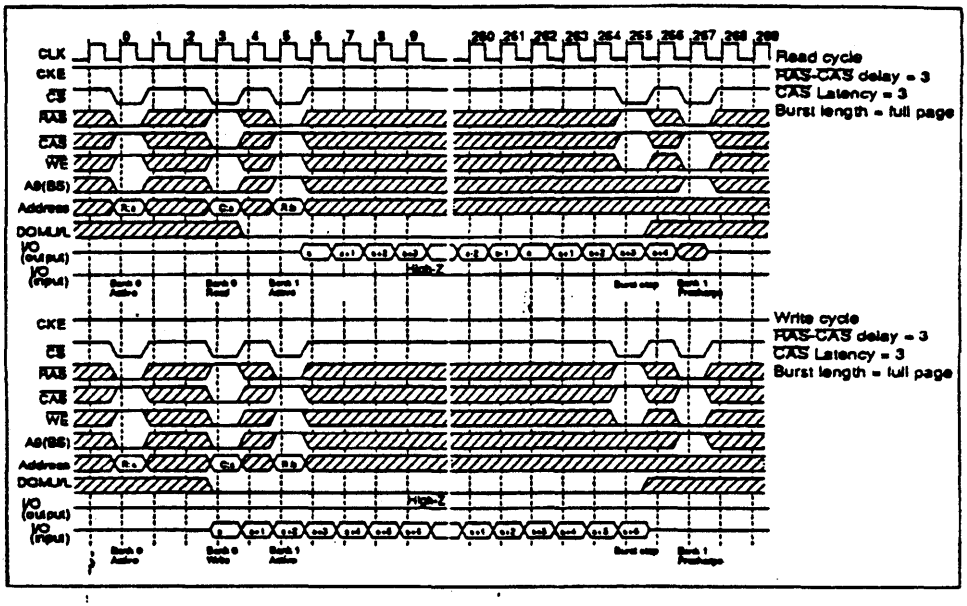
Auto Refresh Cycle



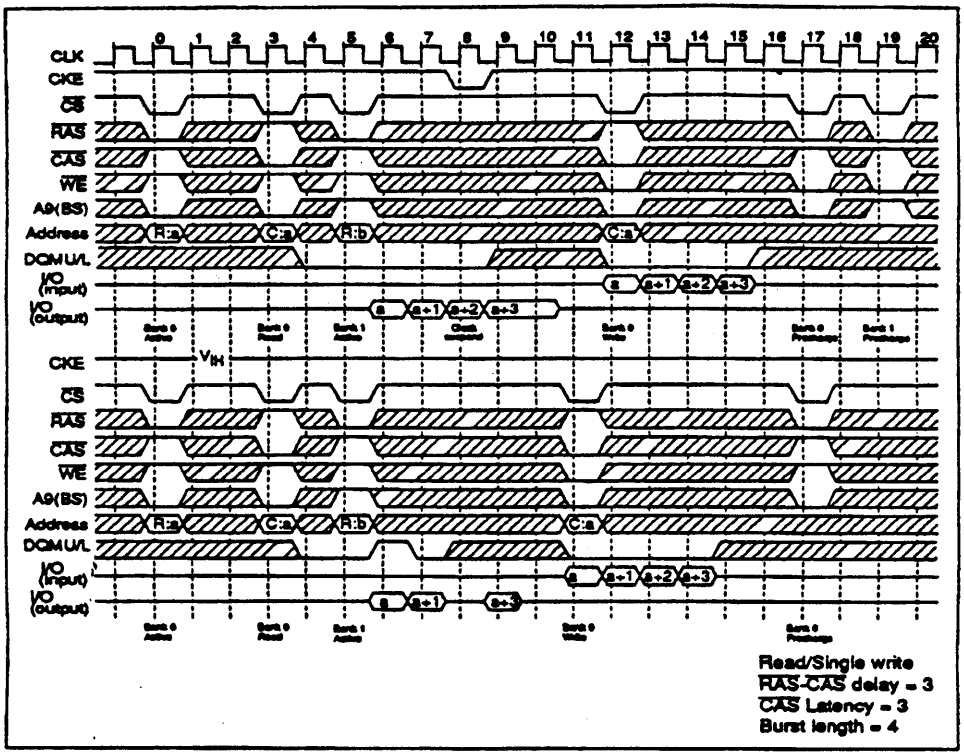
Self Refresh Cycle



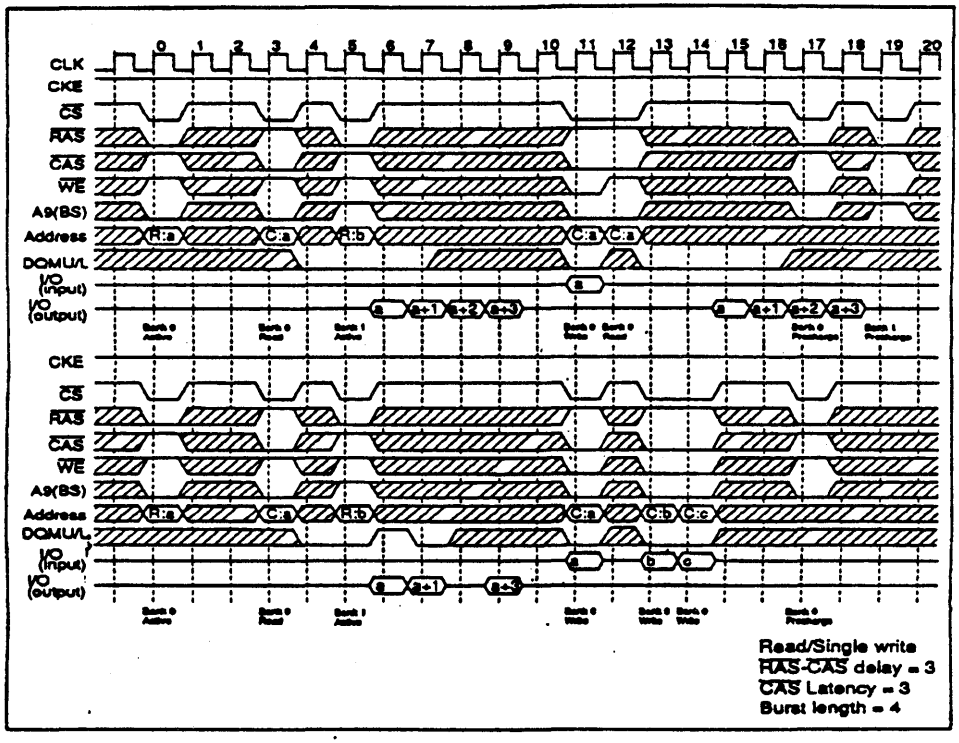
Full Page Read/Write Cycle



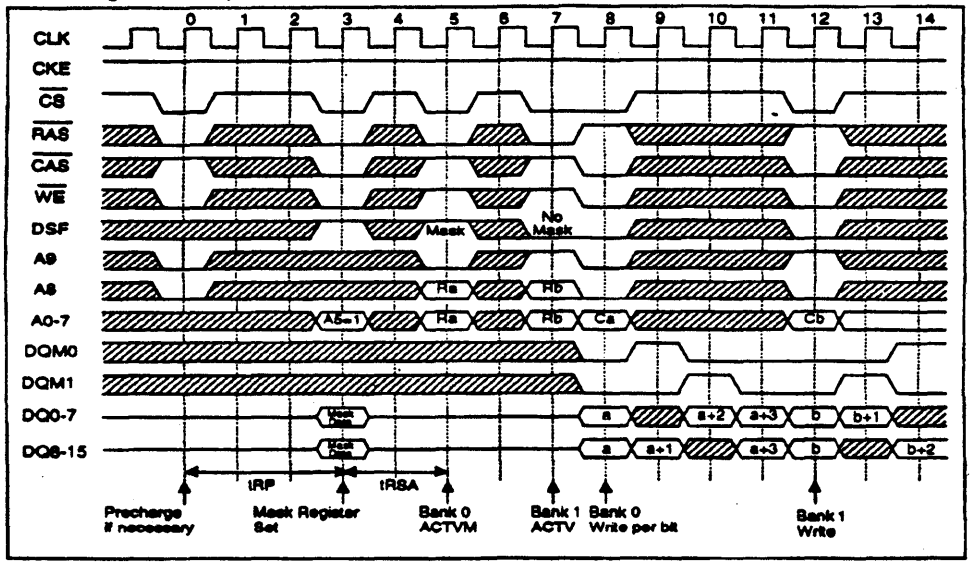
Read/Burst Write Cycle



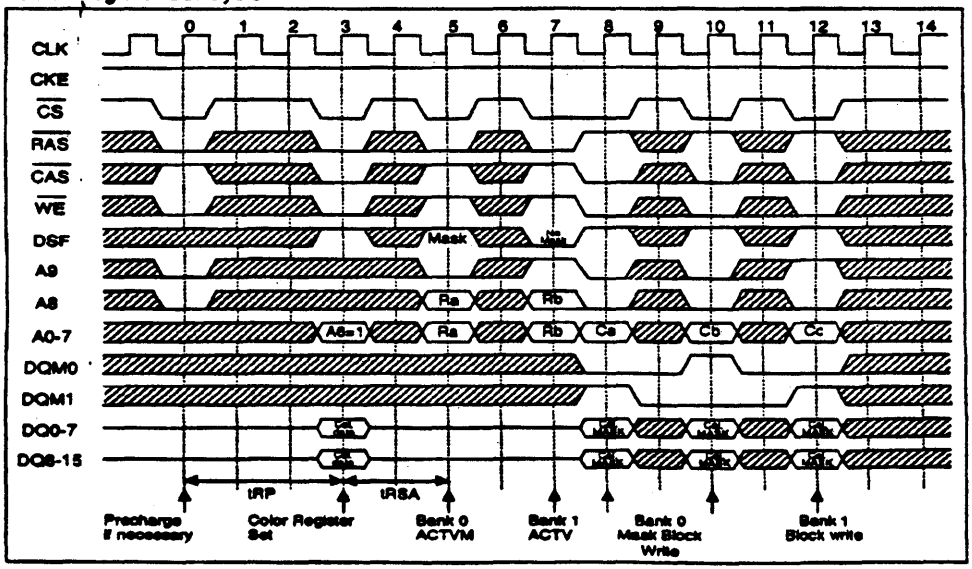
Read/Single Write Cycle



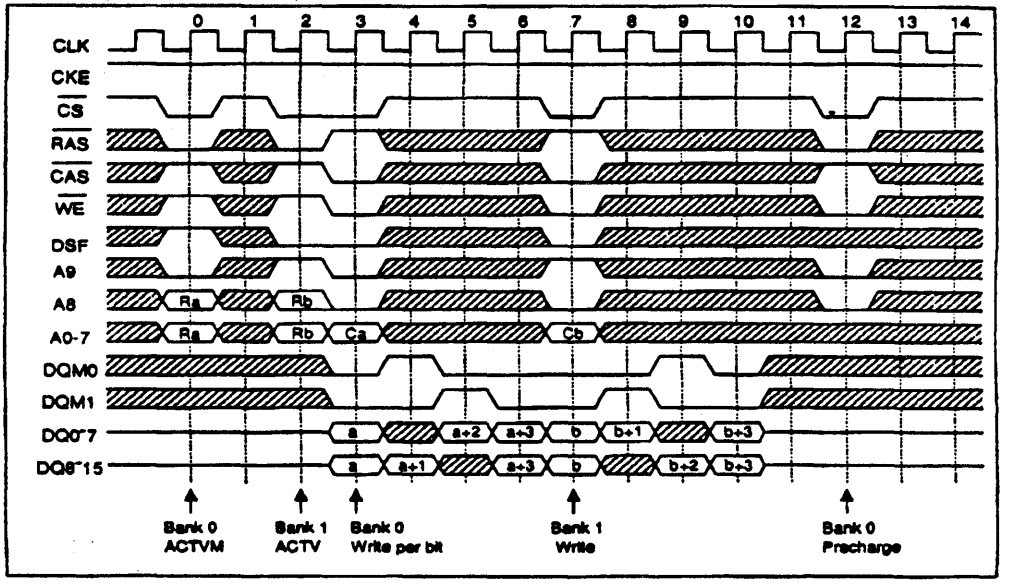
Mask Register Set Cycle



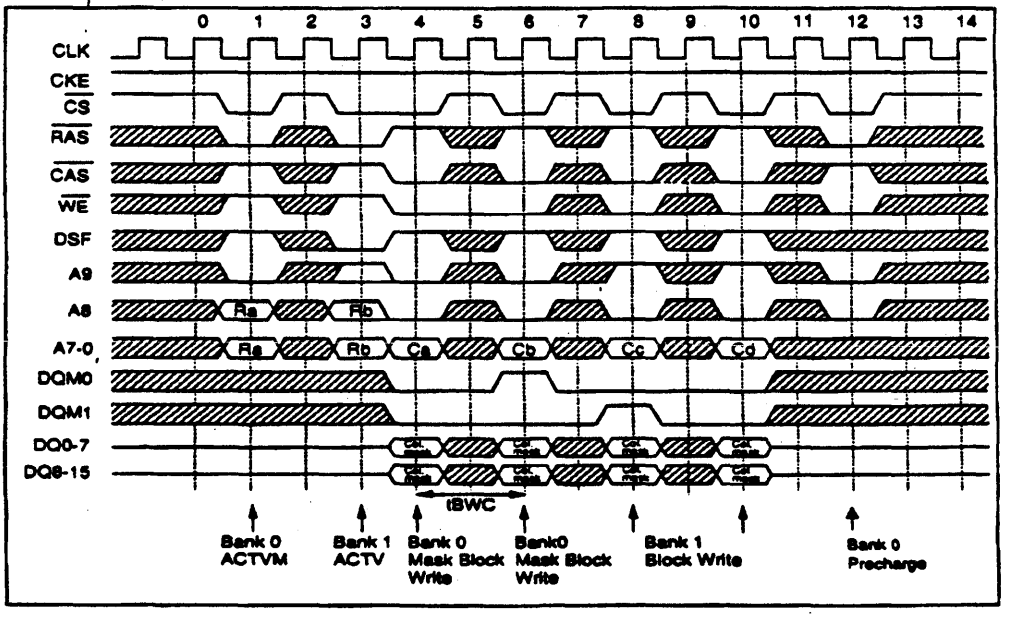
Color Register Set Cycle



Write Cycle(with I/O Mask)



Block Write Cycle



Section 2

VRAM

HM534251B Series

262144-word x 4-bit Multiport CMOS Video RAM

HITACHI

Rev. 1
Mar. 18, 1994

The HM534251B is a 1-Mbit multiport video RAM equipped with a 256-kword x 4-bit dynamic RAM and a 512-word x 4-bit SAM (serial access memory). Its RAM and SAM operate independently and asynchronously. It can transfer data between RAM and SAM and has write mask function.

Features

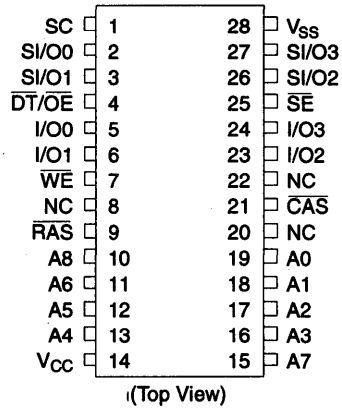
- Multiport organization
  - Asynchronous and simultaneous operation of RAM and SAM capability
    - RAM: 256 kword x 4 bit
    - SAM: 512 word x 4 bit
- Access time
  - RAM: 60 ns/70 ns/80 ns/100 ns max
  - SAM: 20 ns/22 ns/25 ns/25 ns max
- Cycle time
  - RAM: 125 ns/135 ns/150 ns/180 ns min
  - SAM: 25 ns/25 ns/30 ns/30 ns min
- Low power
  - Active RAM: 413 mW max
  - SAM: 275 mW max
  - Standby 38.5 mW max
- High-speed page mode capability
- Mask write mode capability
- Bidirectional data transfer cycle between RAM and SAM capability
- Real time read transfer cycle capability
- 3 variations of refresh (8 ms/512 cycles)
  - $\overline{\text{RAS}}$-only refresh
  - $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - Hidden refresh
- TTL compatible

Ordering Information

Type No.	Access time	Package
HM534251BJ-6	60 ns	400-mil 28-pin plastic SOJ (CP-28D)
HM534251BJ-7	70 ns	
HM534251BJ-8	80 ns	
HM534251BJ-10	100 ns	
HM534251BZ-6	60 ns	400-mil 28-pin plastic ZIP (ZP-28)
HM534251BZ-7	70 ns	
HM534251BZ-8	80 ns	
HM534251BZ-10	100 ns	
HM534251BT-6	60 ns	8 mm x 14 mm 32-pin TSOP type I (TFP-32DA)
HM534251BT-7	70 ns	
HM534251BT-8	80 ns	
HM534251BT-10	100 ns	
HM534251BR-6	60 ns	8 mm x 14 mm 32-pin TSOP type I reverse (TFP-32DAR)
HM534251BR-7	70 ns	
HM534251BR-8	80 ns	
HM534251BR-10	100 ns	

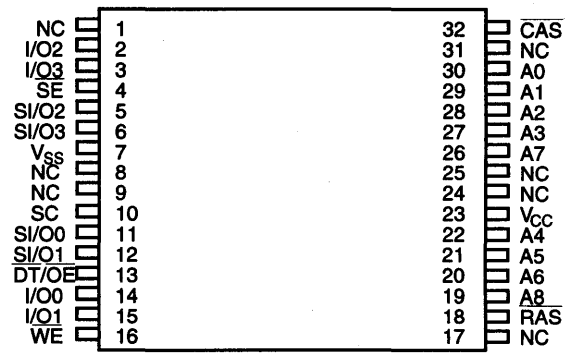
Pin Arrangement

HM534251BJ Series



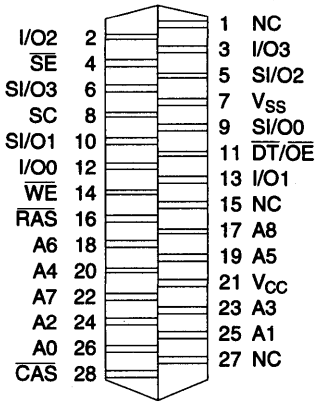
(Top View)

HM534251BT Series



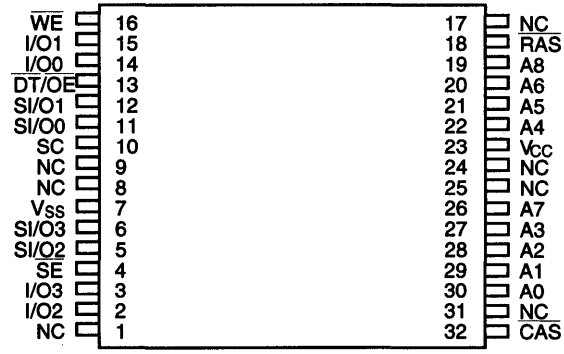
(Top View)

HM534251BZ Series



((Bottom View)

HM534251BR Series

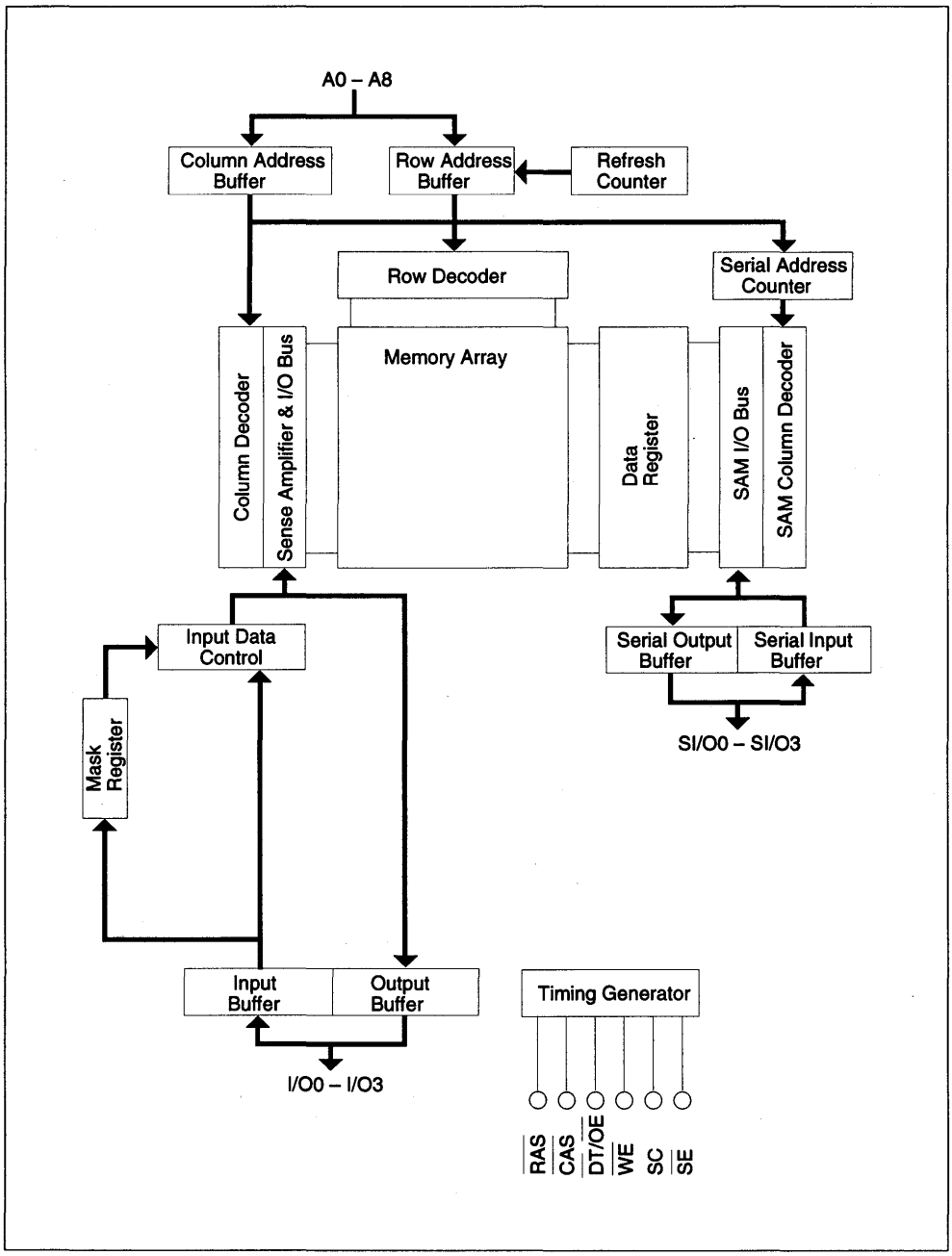


(Top View)

Pin Description

Pin name	Function	Pin name	Function
A0 – A8	Address inputs	$\overline{DT/OE}$	Data transfer/Output enable
I/O0 – I/O3	RAM port data inputs/outputs	SC	Serial clock
SI/O0 – SI/O3	SAM port data inputs/outputs	$\overline{SE}$	SAM port enable
$\overline{RAS}$	Row address strobe	V_{CC}	Power supply
$\overline{CAS}$	Column address strobe	V_{SS}	Ground
$\overline{WE}$	Write enable	NC	No connection

Block Diagram



Pin Functions

$\overline{RAS}$ (input pin): $\overline{RAS}$ is a basic RAM signal. It is active in low level and standby in high level. Row address and signals as shown in table 1 are input at the falling edge of $\overline{RAS}$. The input level of these signals determine the operation cycle of the HM534251B.

Table 1. Operation Cycles of the HM534251B

Input level at the falling edge of $\overline{RAS}$				
$\overline{CAS}$	$\overline{DT/OE}$	$\overline{WE}$	$\overline{SE}$	Operation mode
L	X	X	X	CBR refresh
H	L	L	L	Write transfer
H	L	L	H	Pseudo transfer
H	L	H	X	Read transfer
H	H	L	X	Read/mask write
H	H	H	X	Read/write

Note: X : Don't care.

$\overline{CAS}$ (input pin): Column address is fetched into chip at the falling edge of $\overline{CAS}$. $\overline{CAS}$ controls output impedance of I/O in RAM.

A0–A8 (input pins): Row address is determined by A0–A8 level at the falling edge of $\overline{RAS}$. Column address is determined by A0-A8 level at the falling edge of $\overline{CAS}$. In transfer cycles, row address is the address on the word line which transfers data with SAM data register, and column address is the SAM start address after transfer.

$\overline{WE}$ (input pin): $\overline{WE}$ pin has two functions at the falling edge of $\overline{RAS}$ and after. When $\overline{WE}$ is low at the falling edge of $\overline{RAS}$, the HM534251B turns to mask write mode. According to the I/O level at the time, write on each I/O can be masked. ($\overline{WE}$ level at the falling edge of $\overline{RAS}$ is don't care in read cycle.) When $\overline{WE}$ is high at the falling edge of $\overline{RAS}$, a normal write cycle is executed. After that, $\overline{WE}$ switches read/write cycles as in a standard DRAM. In a transfer cycle, the direction of transfer is determined by $\overline{WE}$ level at the falling edge of $\overline{RAS}$. When $\overline{WE}$ is low, data is transferred from SAM to RAM (data is written into RAM), and when $\overline{WE}$ is high, data is transferred from RAM to SAM (data is read from RAM).

I/O0 – I/O3 (input/output pins): I/O pins function as mask data at the falling edge of $\overline{RAS}$ (in mask write mode). Data is written only to high I/O pins. Data on low I/O pins are masked and internal data are retained. After that, they function as input/output pins as those of a standard DRAM.

$\overline{DT/OE}$ (input pin): $\overline{DT/OE}$ pin functions as $\overline{DT}$ (data transfer) pin at the falling edge of $\overline{RAS}$ and as $\overline{OE}$ (output enable) pin after that. When $\overline{DT}$ is low at the falling edge of $\overline{RAS}$, this cycle becomes a transfer cycle. When $\overline{DT}$ is high at the falling edge of $\overline{RAS}$, RAM and SAM operate independently.

SC (input pin): SC is a basic SAM clock. In a serial read cycle, data outputs from an SI/O pin synchronously with the rising edge of SC. In a serial write cycle, data on an SI/O pin at the rising edge of SC is fetched into the SAM data register.

$\overline{SE}$ (input pin): $\overline{SE}$ pin activates SAM. When $\overline{SE}$ is high, SI/O is in the high impedance state in serial read cycle and data on SI/O is not fetched into the SAM data register in serial write cycle. $\overline{SE}$ can be used as a mask for serial write because internal pointer is incremented at the rising edge of SC.

SI/O0-SI/O3 (input/output pins): SI/Os are input/output pins in SAM. Direction of input/output is determined by the previous transfer cycle. When it was a read transfer cycle, SI/O outputs data. When it was a pseudo transfer cycle or write transfer cycle, SI/O inputs data.

Operation of HM534251B

RAM Read Cycle ($\overline{DT/OE}$ high and $\overline{CAS}$ high at the falling edge of $\overline{RAS}$)

Row address is entered at the $\overline{RAS}$ falling edge and column address at the $\overline{CAS}$ falling edge to the device as in standard DRAM. Then, when $\overline{WE}$ is high and $\overline{DT/OE}$ is low while $\overline{CAS}$ is low, the selected address data outputs through I/O pin. At the falling edge of $\overline{RAS}$, $\overline{DT/OE}$ and $\overline{CAS}$ become high to distinguish RAM read cycle from transfer cycle and CBR refresh cycle. Address access time (t_{AA}) and $\overline{RAS}$ to column address delay time (t_{RAD}) specifications are added to enable high-speed page mode.

RAM Write Cycle (Early Write, Delayed Write, Read-Modify-Write)
($\overline{DT}/\overline{OE}$ high and $\overline{CAS}$ high at the falling edge of $\overline{RAS}$)

- Normal Mode Write Cycle ($\overline{WE}$ high at the falling edge of $\overline{RAS}$)

When $\overline{CAS}$ and $\overline{WE}$ are set low after driving $\overline{RAS}$ low, a write cycle is executed and I/O data is written in the selected addresses. When all 4 I/Os are written, $\overline{WE}$ should be high at the falling edge of $\overline{RAS}$ to distinguish normal mode from mask write mode.
If $\overline{WE}$ is set low before the $\overline{CAS}$ falling edge, this cycle becomes an early write cycle and I/O becomes in high impedance. Data is entered at the $\overline{CAS}$ falling edge.
If $\overline{WE}$ is set low after the $\overline{CAS}$ falling edge, this cycle becomes a delayed write cycle. Data is input at the $\overline{WE}$ falling. I/O does not become high impedance in this cycle, so data should be entered with $\overline{OE}$ in high.
If $\overline{WE}$ is set low after t_{CWD} (min) and t_{AWD} (min) after the $\overline{CAS}$ falling edge, this cycle becomes a read-modify-write cycle and enables read/write at the same address in one cycle. In this cycle also, to avoid I/O contention, data should be input after reading data and driving $\overline{OE}$ high.

- Mask Write Mode ($\overline{WE}$ low at the falling edge of $\overline{RAS}$)

If $\overline{WE}$ is set low at the falling edge of $\overline{RAS}$, the cycle becomes a mask write mode cycle which writes only to selected I/O. Whether or not an I/O is written depends on I/O level (mask data) at the falling edge of $\overline{RAS}$. Then the data is written in high I/O pins and masked in low ones and internal data is retained. This mask data is effective during the $\overline{RAS}$ cycle. So, in high-speed page mode cycle, the mask data is retained during the page access.

High-Speed Page Mode Cycle ($\overline{DT}/\overline{OE}$ high and $\overline{CAS}$ high at the falling edge of $\overline{RAS}$)

High-speed page mode cycle reads/writes the data of the same row address at high speed by toggling $\overline{CAS}$ while $\overline{RAS}$ is low. Its cycle time is one third of the random read/write cycle. Note that address access time (t_{AA}), $\overline{RAS}$ to column address delay time (t_{RAD}), and access time from $\overline{CAS}$ precharge (t_{ACP}) are added. In one $\overline{RAS}$ cycle, 512-word memory cells of the same row address can be accessed. It is necessary to specify access frequency within t_{RASP} max (100 µs).

Transfer Operation

The HM534251B provides the read transfer cycle, pseudo transfer cycle and write transfer cycle as data transfer cycles. These transfer cycles are set by driving $\overline{CAS}$ high and $\overline{DT}/\overline{OE}$ low at the falling edge of $\overline{RAS}$. They have following functions:

(1) Transfer data between row address and SAM data register (except for pseudo transfer cycle)
Read transfer cycle: RAM to SAM
Write transfer cycle: SAM to RAM
(2) Determine SI/O state
Read transfer cycle: SI/O output
Pseudo transfer cycle
and write transfer cycle: SI/O input
(3) Determine first SAM address to access after transferring at column address (SAM start address).
SAM start address must be determined by read transfer cycle or pseudo transfer cycle after power on, and determined for each transfer cycle.

Read Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low and $\overline{WE}$ high at the falling edge of $\overline{RAS}$)

This cycle becomes read transfer cycle by driving $\overline{DT}/\overline{OE}$ low and $\overline{WE}$ high at the falling edge of $\overline{RAS}$. The row address data (512 x 4-bit) determined by this cycle is transferred to SAM data register synchronously at the rising edge of $\overline{DT}/\overline{OE}$. After the rising edge of $\overline{DT}/\overline{OE}$, the new address data outputs from SAM start address determined by column address. In read transfer cycle, $\overline{DT}/\overline{OE}$ must be risen to transfer data from RAM to SAM.
This cycle can access SAM even during transfer (real time read transfer). In this case, the timing t_{SDD} (min) specified between the last SAM access before transfer and $\overline{DT}/\overline{OE}$ rising edge and t_{SDH} (min) specified between the first SAM access and $\overline{DT}/\overline{OE}$ rising edge must be satisfied. (See figure 1.).

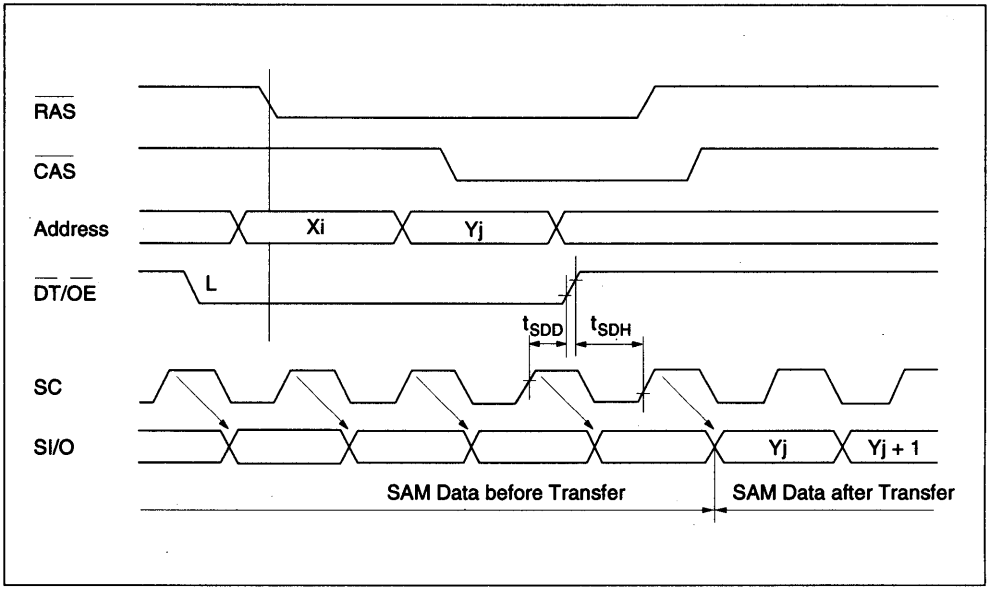


Figure 1. Real Time Read Transfer

When read transfer cycle is executed, SI/O becomes output state by first SAM access. Input must be set high impedance before t_{SZS} (min) of the first SAM access to avoid data contention.

Pseudo Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low and $\overline{SE}$ high at the falling edge of $\overline{RAS}$)

Pseudo transfer cycle switches SI/O to input state and set SAM start address without data transfer to RAM.
This cycle starts when $\overline{CAS}$ is high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low and $\overline{SE}$ high at the falling edge of $\overline{RAS}$. Data should be input to SI/O later than t_{SID} (min) after $\overline{RAS}$ becomes low to avoid data contention. SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. In this cycle, SAM access is inhibited during $\overline{RAS}$ low, therefore, SC must not be risen.

Write Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low and $\overline{SE}$ low at the falling edge of $\overline{RAS}$)

Write transfer cycle can transfer a row of data input by serial write cycle to RAM. The row address of data transferred into RAM is determined by the address at the falling edge of $\overline{RAS}$. The column address is specified as the first address for serial write after terminating this cycle. Also in this cycle, SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. SAM access is inhibited during $\overline{RAS}$ low. In this period, SC must not be risen.
Data transferred to SAM by read transfer cycle can be written to other address of RAM by write transfer cycle. However, the address to write data must be the same MSB of row address (AX8) as that of the read transfer cycle.

SAM Port Operation

Serial Read Cycle

SAM port is in read mode when the previous data transfer cycle is read transfer cycle. Access is synchronized with SC rising, and SAM data is output from SI/O. When $\overline{SE}$ is set high, SI/O becomes high impedance, and the internal pointer is incremented by the SC rising. After indicating the last address (address 511), the internal pointer indicates address 0 at the next access.

Serial Write Cycle

If previous data transfer cycle is pseudo transfer cycle or write transfer cycle, SAM port goes into write mode. In this cycle, SI/O data is fetched into data register at the SC rising edge like in the serial read cycle. If $\overline{SE}$ is high, SI/O data isn't fetched into data register. Internal pointer is incremented by the SC rising, so $\overline{SE}$ high can be used as mask data for SAM. After indicating the last address (address 511), the internal pointer indicates address 0 at the next access.

Refresh

RAM Refresh

RAM, which is composed of dynamic circuits, requires refresh to retain data. Refresh is executed by accessing all 512 row addresses within 8 ms. There are three refresh cycles: (1) $\overline{RAS}$-only refresh cycle, (2) $\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh cycle, and (3) Hidden refresh cycle. Besides them, the cycles which activate $\overline{RAS}$ such as read/write cycles or transfer cycles can refresh the row address. Therefore, no refresh cycle is required when all row addresses are accessed within 8 ms.

(1) $\overline{RAS}$-Only Refresh Cycle: $\overline{RAS}$-only refresh cycle is executed by activating only $\overline{RAS}$ cycle with $\overline{CAS}$ fixed to high after inputting the row address (= refresh address) from external circuits. To distinguish this cycle from data transfer cycle, $\overline{DT/OE}$ must be high at the falling edge of $\overline{RAS}$.

(2) CBR Refresh Cycle: CBR refresh cycle is set by activating $\overline{CAS}$ before $\overline{RAS}$. In this cycle, refresh address need not to be input through external circuits because it is input through an internal refresh counter. In this cycle, output is in high impedance and power dissipation is lowered because $\overline{CAS}$ circuits don't operate.

(3) Hidden Refresh Cycle: Hidden refresh cycle executes CBR refresh with the data output by reactivating $\overline{RAS}$ when $\overline{DT/OE}$ and $\overline{CAS}$ keep low in normal RAM read cycles.

SAM Refresh

SAM parts (data register, shift register and selector), organized as fully static circuitry, require no refresh.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal voltage*1	V_T	−1.0 to +7.0	V
Power supply voltage*1	V_{CC}	−0.5 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C

Note: 1. Relative to V_{SS}.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage*1	V_{CC}	4.5	5.0	5.5	V
Input high voltage*1	V_{IH}	2.4	—	6.5	V
Input low voltage*1	V_{IL}	–0.5*2	—	0.8	V

Notes: 1. All voltages referenced to V_{SS}.
2. –3.0 V for pulse width ≤ 10 ns.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

		HM534251B										
		-6		-7		-8		-10			Test conditions	
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	RAM port	SAM port
Operating current	I_{CC1}	—	75	—	70	—	60	—	55	mA	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC7}	—	125	—	120	—	100	—	95	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = min
Standby current	I_{CC2}	—	7	—	7	—	7	—	7	mA	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC8}	—	50	—	50	—	40	—	40	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = min
$\overline{RAS}$-only refresh current	I_{CC3}	—	75	—	70	—	60	—	55	mA	$\overline{RAS}$ cycling $\overline{CAS}$ = V_{IH} t_{RC} = min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC9}	—	125	—	120	—	100	—	95	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = min
Page mode current	I_{CC4}	—	80	—	80	—	70	—	65	mA	$\overline{CAS}$ cycling $\overline{RAS}$ = V_{IL} t_{PC} = min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC10}	—	130	—	130	—	110	—	105	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = min
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC5}	—	50	—	45	—	40	—	35	mA	$\overline{RAS}$ cycling t_{RC} = min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC11}	—	100	—	95	—	80	—	75	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = min
Data transfer current	I_{CC6}	—	80	—	75	—	65	—	60	mA	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC12}	—	130	—	125	—	105	—	100	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = min

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V) (cont)

		HM534251B									
		-6		-7		-8		-10			Test conditions
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	RAM port / SAM port
Input leakage current	I_{LI}	−10	10	−10	10	−10	10	−10	10	µA	
Output leakage current	I_{LO}	−10	10	−10	10	−10	10	−10	10	µA	
Output high voltage	V_{OH}	2.4	—	2.4	—	2.4	—	2.4	—	V	I_{OH} = −2 mA
Output low voltage	V_{OL}	—	0.4	—	0.4	—	0.4	—	0.4	V	I_{OL} = 4.2 mA

Note: 1. I_{CC} depends on output loading condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed once while $\overline{RAS}$ is low and $\overline{CAS}$ is high.

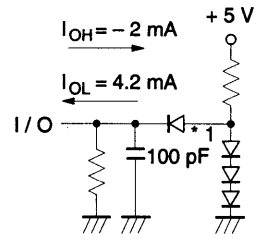
Capacitance (Ta = 25°C, V_{CC} = 5 V, f = 1 MHz, Bias: Clock, I/O = V_{CC}, address = V_{SS})

Item	Symbol	Min	Typ	Max	Unit
Address	C_{I1}	—	—	5	pF
Clock	C_{I2}	—	—	5	pF
I/O, SI/O	$C_{I/O}$	—	—	7	pF

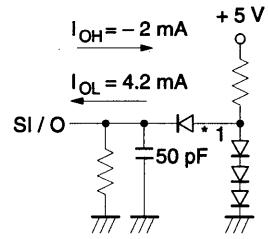
AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ±10%, V_{SS} = 0 V) *1, *16

Test Conditions

- Input rise and fall time: 5 ns
- Output load: See figures
- Input pulse levels : V_{SS} to 3.0 V
- Input timing reference levels: 0.8 V, 2.4 V
- Output timing reference levels: 0.8 V, 2.0 V



Output Load (A)



Output Load (B)

Note: 1. Including scope & jig.

Common Parameter

Item	Symbol	HM534251B -6 Min	-6 Max	-7 Min	-7 Max	-8 Min	-8 Max	-10 Min	-10 Max	Unit	Notes
Random read or write cycle time	t_{RC}	125	—	135	—	150	—	180	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	55	—	55	—	60	—	70	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	—	20	—	20	—	25	—	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	15	—	15	—	15	—	15	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	20	60	20	75	ns	2
$\overline{RAS}$ hold time referenced to $\overline{CAS}$	t_{RSH}	20	—	20	—	20	—	25	—	ns	
$\overline{CAS}$ hold time referenced to $\overline{RAS}$	t_{CSH}	60	—	70	—	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	10	—	10	—	ns	
Transition time (rise to fall)	t_T	3	50	3	50	3	50	3	50	ns	3
Refresh period	t_{REF}	—	8	—	8	—	8	—	8	ms	
$\overline{DT}$ to $\overline{RAS}$ setup time	t_{DTS}	0	—	0	—	0	—	0	—	ns	
$\overline{DT}$ to $\overline{RAS}$ hold time	t_{DTH}	10	—	10	—	10	—	10	—	ns	
Data-in to $\overline{CAS}$ delay time	t_{DZC}	0	—	0	—	0	—	0	—	ns	4
Data-in to $\overline{OE}$ delay time	t_{DZO}	0	—	0	—	0	—	0	—	ns	4
Output buffer turn-off delay referenced to $\overline{CAS}$	t_{OFF1}	—	20	—	20	—	20	—	20	ns	5
Output buffer turn-off delay referenced to $\overline{OE}$	t_{OFF2}	—	20	—	20	—	20	—	20	ns	5

Read Cycle (RAM), Page Mode Read Cycle

		HM534251B									
		-6		-7		-8		-10			
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Access time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	ns	6, 7
Access time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	20	—	25	ns	7, 8
Access time from $\overline{OE}$	t_{OAC}	—	20	—	20	—	20	—	25	ns	7
Address access time	t_{AA}	—	35	—	35	—	40	—	45	ns	7, 9
Read command setup time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	0	—	0	—	ns	10
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	10	—	ns	10
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	35	15	40	15	55	ns	2
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	—	35	—	40	—	45	—	ns	
Column address to $\overline{CAS}$ lead time	t_{CAL}	35	—	35	—	40	—	45	—	ns	
Page mode cycle time	t_{PC}	45	—	45	—	50	—	55	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	—	10	—	10	—	10	—	ns	
Access time from $\overline{CAS}$ precharge	t_{ACP}	—	40	—	40	—	45	—	50	ns	
Page mode $\overline{RAS}$ pulse width	t_{RASP}	60	100000	70	100000	80	100000	100	100000	ns	

Write Cycle (RAM), Page Mode Write Cycle

		HM534251B									
		-6		-7		-8		-10			
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Write command setup time	t_{WCS}	0	—	0	—	0	—	0	—	ns	11
Write command hold time	t_{WCH}	15	—	15	—	15	—	15	—	ns	
Write command pulse width	t_{WP}	15	—	15	—	15	—	15	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	—	20	—	20	—	20	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	—	20	—	20	—	20	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	0	—	ns	12
Data-in hold time	t_{DH}	15	—	15	—	15	—	15	—	ns	12
$\overline{WE}$ to $\overline{RAS}$ setup time	t_{WS}	0	—	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ hold time	t_{WH}	10	—	10	—	10	—	10	—	ns	
Mask data to $\overline{RAS}$ setup time	t_{MS}	0	—	0	—	0	—	0	—	ns	
Mask data to $\overline{RAS}$ hold time	t_{MH}	10	—	10	—	10	—	10	—	ns	
$\overline{OE}$ hold time referenced to $\overline{WE}$	t_{OEH}	20	—	20	—	20	—	20	—	ns	
Page mode cycle time	t_{PC}	45	—	45	—	50	—	55	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ to data-in delay time	t_{CDD}	20	—	20	—	20	—	20	—	ns	13
Page mode $\overline{RAS}$ pulse width	t_{RASP}	60	100000	70	100000	80	100000	100	100000	ns	

Read-Modify-Write Cycle

Item	Symbol	HM534251B -6 Min	-6 Max	-7 Min	-7 Max	-8 Min	-8 Max	-10 Min	-10 Max	Unit	Notes
Read-modify-write cycle time	t_{RWC}	175	—	185	—	200	—	230	—	ns	
$\overline{RAS}$ pulse width (read-modify-write cycle)	t_{RWS}	110	10000	120	10000	130	10000	150	10000	ns	
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	45	—	45	—	45	—	50	—	ns	14
Column address to $\overline{WE}$ delay time	t_{AWD}	60	—	60	—	65	—	70	—	ns	14
$\overline{OE}$ to data-in delay time	t_{ODD}	20	—	20	—	20	—	20	—	ns	12
Access time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	ns	6, 7
Access time form $\overline{CAS}$	t_{CAC}	—	20	—	20	—	20	—	25	ns	7, 8
Access time from $\overline{OE}$	t_{OAC}	—	20	—	20	—	20	—	25	ns	7
Address access time	t_{AA}	—	35	—	35	—	40	—	45	ns	7, 9
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	35	15	40	15	55	ns	
Read command setup time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	—	20	—	20	—	20	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	—	20	—	20	—	20	—	ns	
Write command pulse width	t_{WP}	15	—	15	—	15	—	15	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	0	—	ns	12
Data-in hold time	t_{DH}	15	—	15	—	15	—	15	—	ns	12
$\overline{OE}$ hold time referenced to $\overline{WE}$	t_{OEH}	20	—	20	—	20	—	20	—	ns	

Refresh Cycle

Item	Symbol	HM534251B -6 Min	-6 Max	-7 Min	-7 Max	-8 Min	-8 Max	-10 Min	-10 Max	Unit	Notes
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10	—	10	—	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	—	10	—	10	—	10	—	ns	

Read Transfer Cycle

Item	Symbol	HM534251B -6 Min	-6 Max	-7 Min	-7 Max	-8 Min	-8 Max	-10 Min	-10 Max	Unit	Notes
$\overline{DT}$ hold time referenced to $\overline{RAS}$	t_{RDH}	50	10000	60	10000	65	10000	80	10000	ns	
$\overline{DT}$ hold time referenced to $\overline{CAS}$	t_{CDH}	20	—	20	—	20	—	25	—	ns	
$\overline{DT}$ hold time referenced to column address	t_{ADH}	25	—	25	—	30	—	30	—	ns	
$\overline{DT}$ precharge time	t_{DTP}	20	—	20	—	20	—	30	—	ns	
$\overline{DT}$ to $\overline{RAS}$ delay time	t_{DRD}	65	—	65	—	70	—	80	—	ns	
SC to $\overline{RAS}$ setup time	t_{SRS}	25	—	25	—	30	—	30	—	ns	
1st SC to $\overline{RAS}$ hold time	t_{SRH}	60	—	70	—	80	—	100	—	ns	
1st SC to $\overline{CAS}$ hold time	t_{SCH}	25	—	25	—	25	—	25	—	ns	
1st SC to column address hold time	t_{SAH}	40	—	40	—	45	—	50	—	ns	
Last SC to $\overline{DT}$ delay time	t_{SDD}	5	—	5	—	5	—	5	—	ns	
1st SC to $\overline{DT}$ hold time	t_{SDH}	10	—	10	—	15	—	15	—	ns	
Serial data-in to 1st SC delay time	t_{SZS}	0	—	0	—	0	—	0	—	ns	
Serial clock cycle time	t_{SCC}	25	—	25	—	30	—	30	—	ns	
SC pulse width	t_{SC}	5	—	5	—	10	—	10	—	ns	
SC precharge time	t_{SCP}	10	—	10	—	10	—	10	—	ns	

Read Transfer Cycle (cont)

		HM534251B									
		-6		-7		-8		-10			
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
SC access time	t_{SCA}	—	20	—	22	—	25	—	25	ns	15
Serial data-out hold time	t_{SOH}	5	—	5	—	5	—	5	—	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	15	—	15	—	15	—	ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	35	15	40	15	55	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	—	35	—	40	—	45	—	ns	
$\overline{DT}$ high hold time from $\overline{RAS}$ precharge	t_{DTHH}	10	—	10	—	10	—	10	—	ns	

Pseudo Transfer Cycle, Write Transfer Cycle

		HM534251B									
		-6		-7		-8		-10			
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{SE}$ setup time referenced to $\overline{RAS}$	t_{ES}	0	—	0	—	0	—	0	—	ns	
$\overline{SE}$ hold time referenced to $\overline{RAS}$	t_{EH}	10	—	10	—	10	—	10	—	ns	
SC setup time referenced to $\overline{RAS}$	t_{SRS}	25	—	25	—	30	—	30	—	ns	
$\overline{RAS}$ to SC delay time	t_{SRD}	20	—	20	—	25	—	25	—	ns	
Serial output buffer turn-off time referenced to $\overline{RAS}$	t_{SRZ}	10	40	10	40	10	45	10	50	ns	
$\overline{RAS}$ to serial data-in delay time	t_{SID}	40	—	40	—	45	—	50	—	ns	
Serial clock cycle time	t_{SCC}	25	—	25	—	30	—	30	—	ns	
SC pulse width	t_{SC}	5	—	5	—	10	—	10	—	ns	
SC precharge time	t_{SCP}	10	—	10	—	10	—	10	—	ns	
SC access time	t_{SCA}	—	20	—	22	—	25	—	25	ns	15

Pseudo Transfer Cycle, Write Transfer Cycle (cont)

		HM534251B									
		-6		-7		-8		-10			
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{SE}$ access time	t_{SEA}	—	20	—	22	—	25	—	25	ns	15
Serial data-out hold time	t_{SOH}	5	—	5	—	5	—	5	—	ns	
Serial write enable setup time	t_{SWS}	5	—	5	—	5	—	5	—	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	15	—	15	—	15	—	ns	

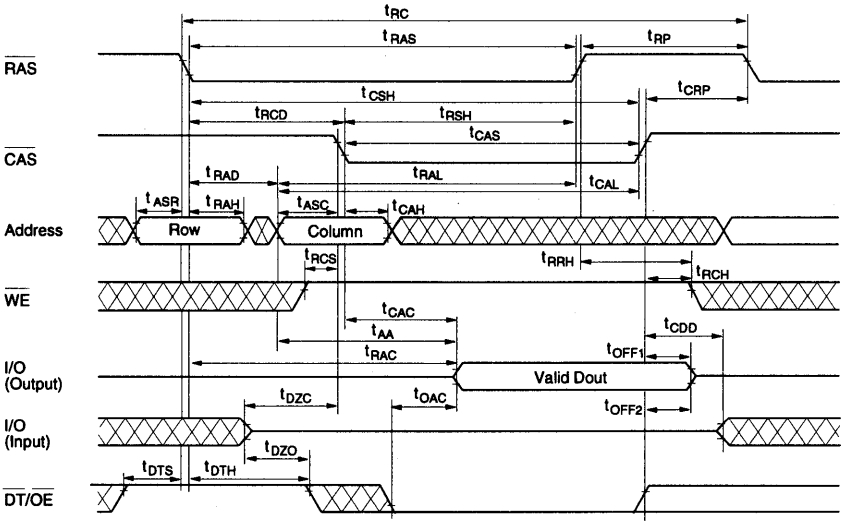
Serial Read Cycle, Serial Write Cycle

		HM534251B									
		-6		-7		-8		-10			
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Serial clock cycle time	t_{SCC}	25	—	25	—	30	—	30	—	ns	
SC pulse width	t_{SC}	5	—	5	—	10	—	10	—	ns	
SC precharge width	t_{SCP}	10	—	10	—	10	—	10	—	ns	
Access time from SC	t_{SCA}	—	20	—	22	—	25	—	25	ns	15
Access time from $\overline{SE}$	t_{SEA}	—	20	—	22	—	25	—	25	ns	15
Serial data-out hold time	t_{SOH}	5	—	5	—	5	—	5	—	ns	
Serial output buffer turn-off time referenced to $\overline{SE}$	t_{SEZ}	—	20	—	20	—	20	—	20	ns	5
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	15	—	15	—	15	—	ns	
Serial write enable setup time	t_{SWS}	5	—	5	—	5	—	5	—	ns	
Serial write enable hold time	t_{SWH}	15	—	15	—	15	—	15	—	ns	
Serial write disable setup time	t_{SWIS}	5	—	5	—	5	—	5	—	ns	
Serial write disable hold time	t_{SWIH}	15	—	15	—	15	—	15	—	ns	

Notes:
1. AC measurements assume t_T = 5 ns.
2. When $t_{RCD} > t_{RCD}$ (max) or $t_{RAD} > t_{RAD}$ (max), access time is specified by t_{CAC} or t_{AA}.
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition time t_T is measured between V_{IH} and V_{IL}.
4. Data input must be floating before output buffer is turned on. In read cycle, read-modify-write cycle and delayed write cycle, either t_{DZC} (min) or t_{DZO} (min) must be satisfied.
5. t_{OFF1} (max), t_{OFF2} (max) and t_{SEZ} (max) are defined as the time at which the output acheives the open circuit condition (V_{OH} −100 mV, V_{OL} +100 mV).
6. Assume that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
7. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
8. When $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max), access time is specified by t_{CAC}.
9. When $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max), access time is specified by t_{AA}.
10. If either t_{RCH} of t_{RRH} is satisfied, operation is guaranteed.
11. When $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle, and I/O pins remain in an open circuit (high impedance) condition.
12. These parameters are specified by the later falling edge of $\overline{CAS}$ or $\overline{WE}$.
13. Either t_{CDD} (min) or t_{ODD} (min) must be satisfied because output buffer must be turned off by $\overline{CAS}$ or $\overline{OE}$ prior to applying data to the device when output buffer is on.
14. When $t_{AWD} \geq t_{AWD}$ (min) and $t_{CWD} \geq t_{CWD}$ (min) in read-modify-write cycle, the data of the selected address outputs to an I/O pin and input data is written into the selected address. t_{ODD} (min) must be satisfied because output buffer must be turned off by $\overline{OE}$ prior to applying data to the device.
15. Measured with a load circuit equivalent to 2 TTL loads and 50 pF.
16. After power-up, pause for 100 µs or more and execute at least 8 initialization cycle (normal memory cycle or refresh cycle), then start operation.

Timing Waveforms *17

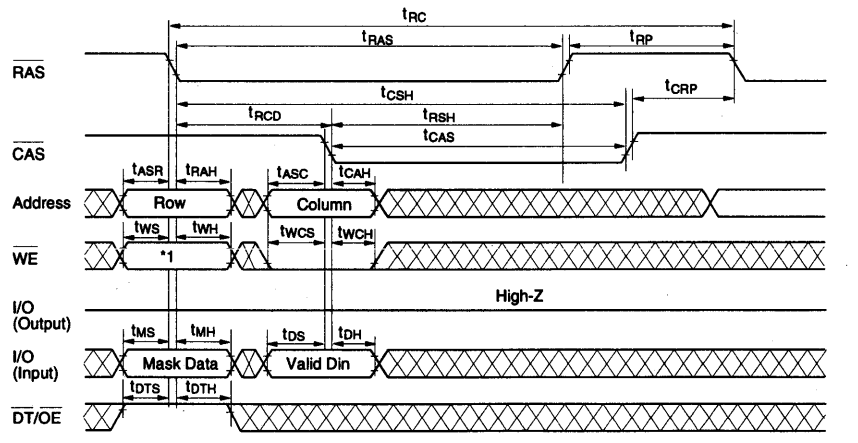
Read Cycle



Note17: H or L (H: V_{IH} (min) ≤ V_{IN} ≤ V_{IH} (max), L: V_{IL} (min) ≤ V_{IN} ≤ V_{IL} (max))

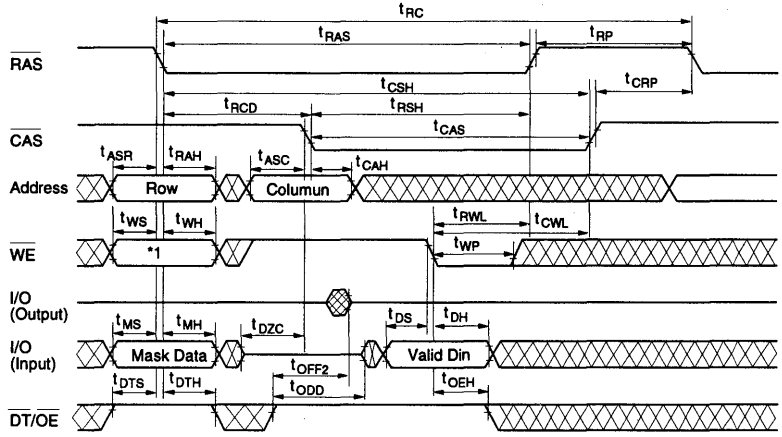
Invalid Dout

Early Write Cycle



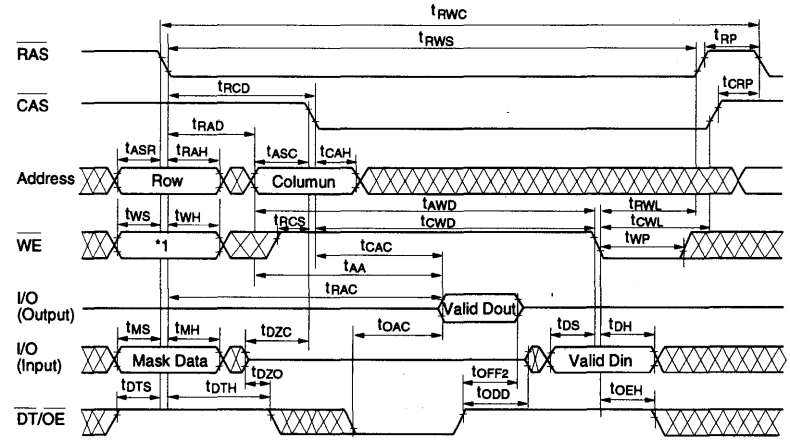
Note: 1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

Delayed Write Cycle



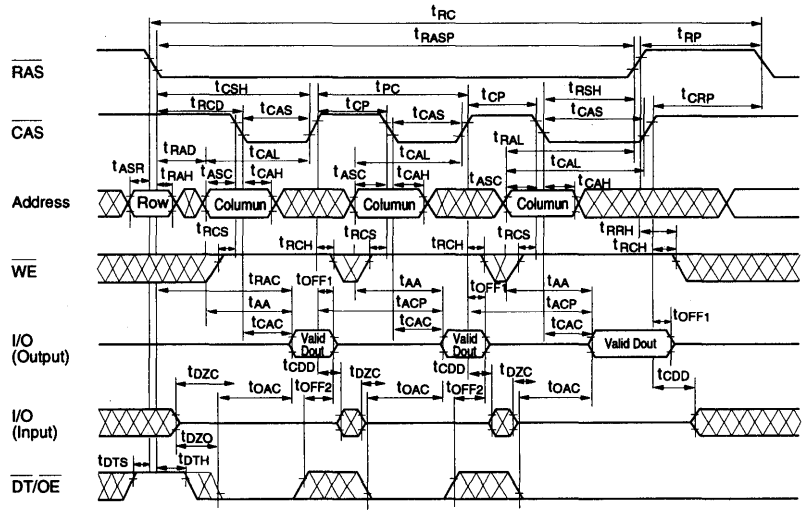
Note: 1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

Read-Modify-Write Cycle

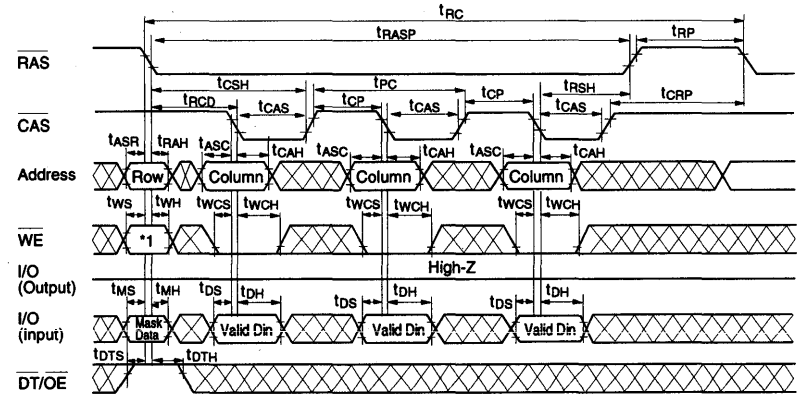


Note: 1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

Page Mode Read Cycle

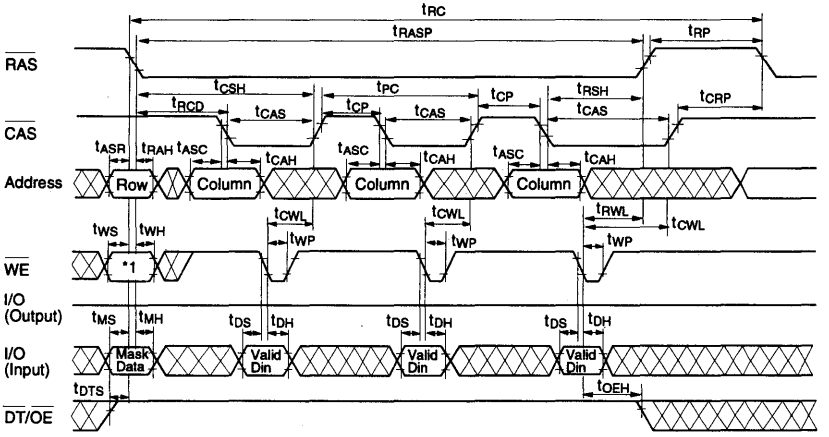


Page Mode Write Cycle (Early Write)



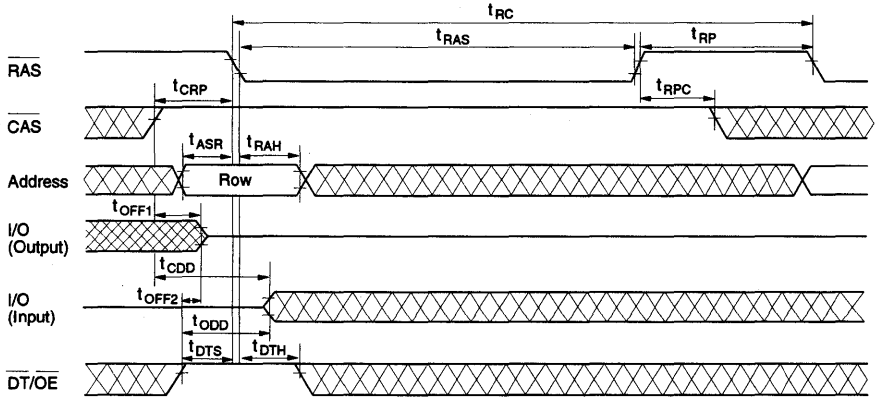
Note: 1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

Page Mode Write Cycle (Delayed Write)

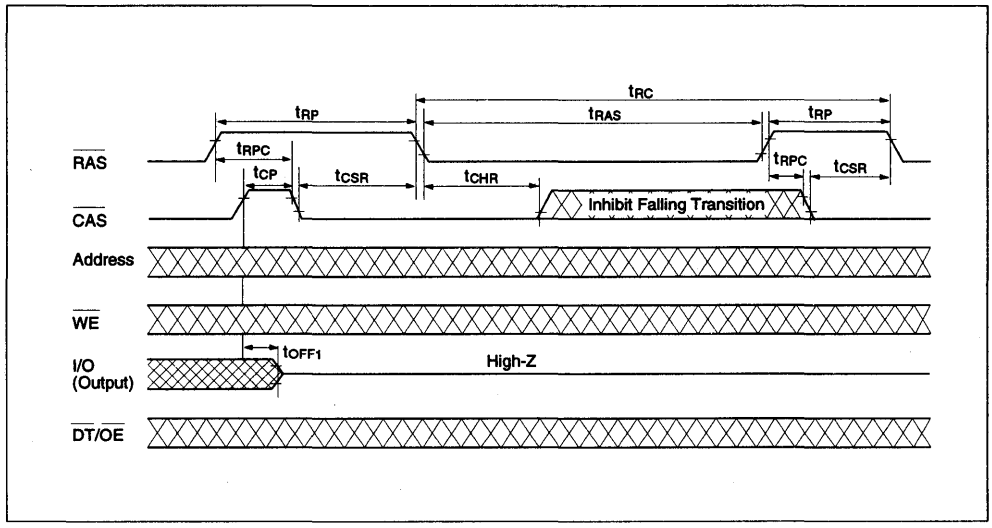


Note: 1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

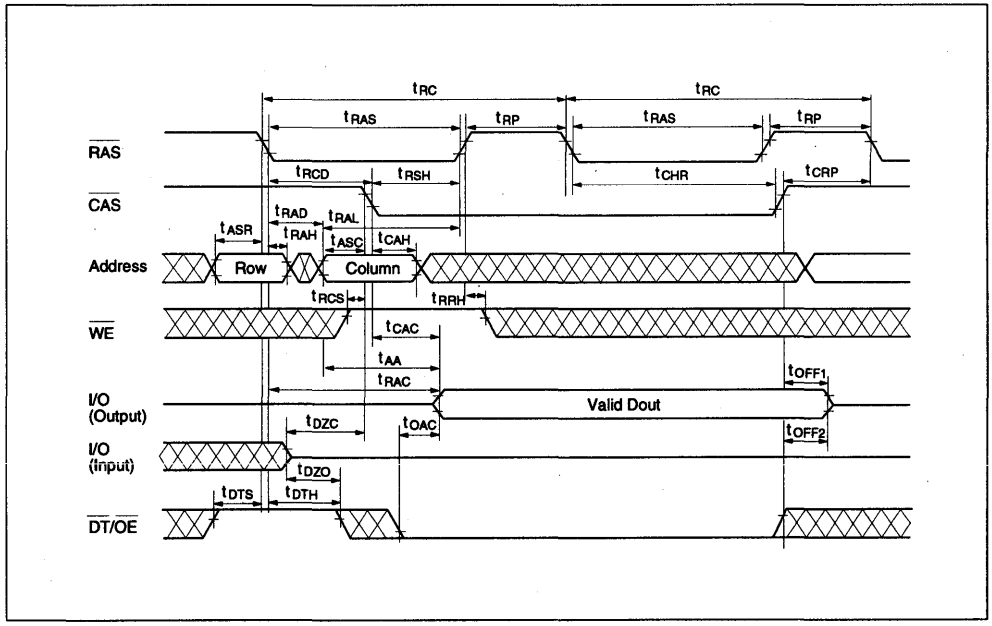
$\overline{RAS}$-Only Refresh Cycle



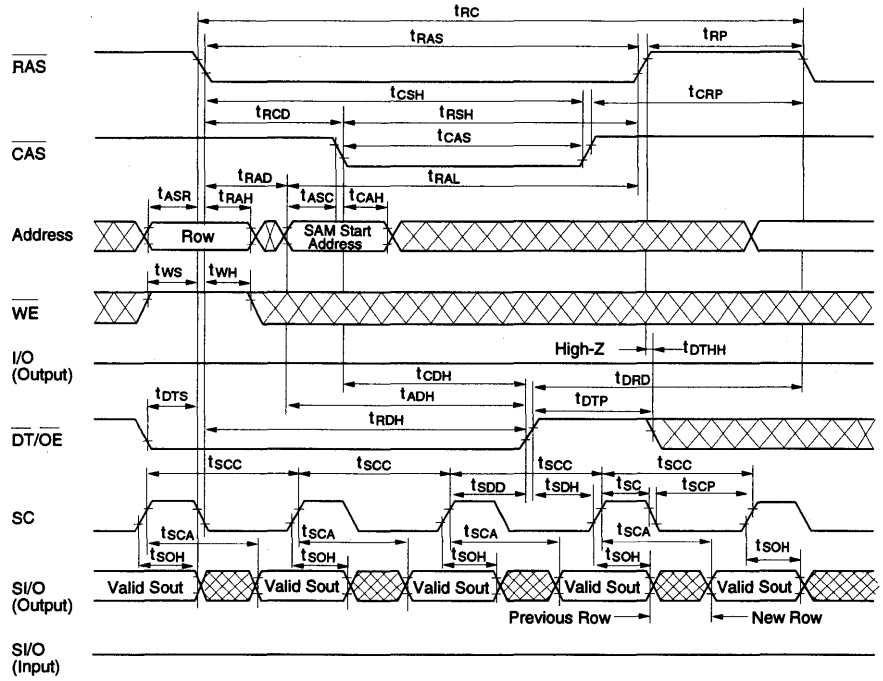
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle



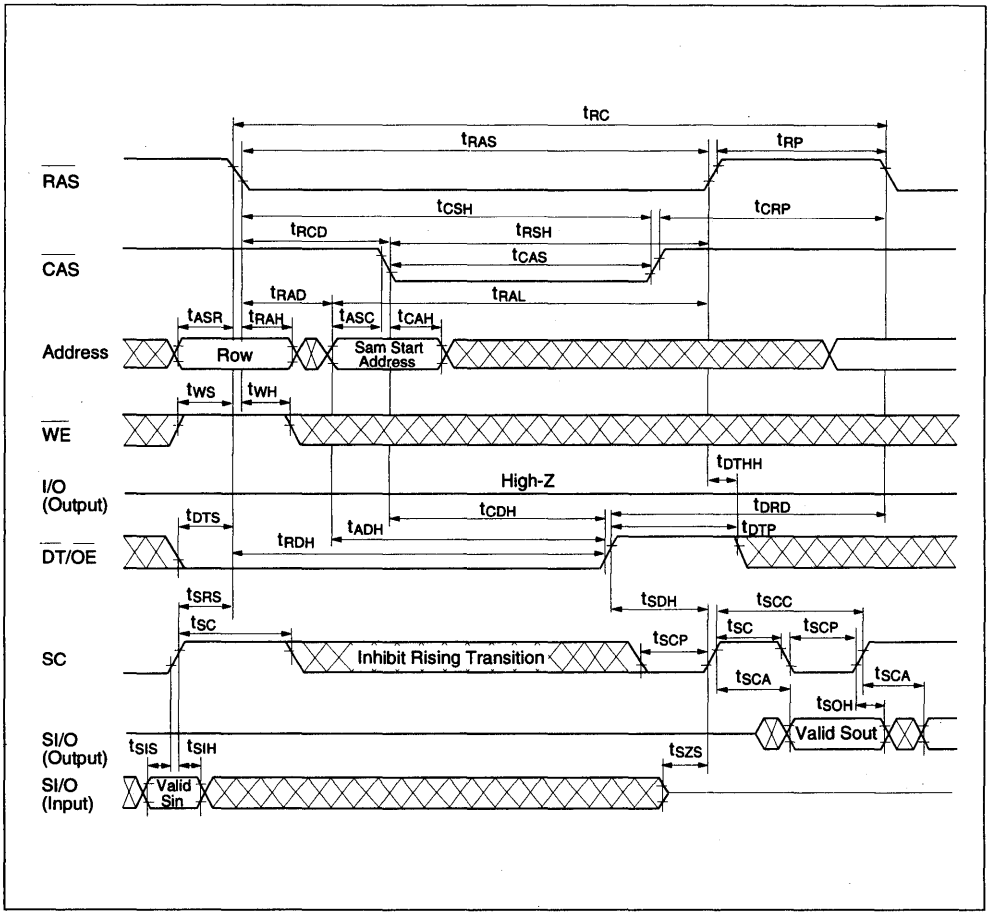
Hidden Refresh Cycle



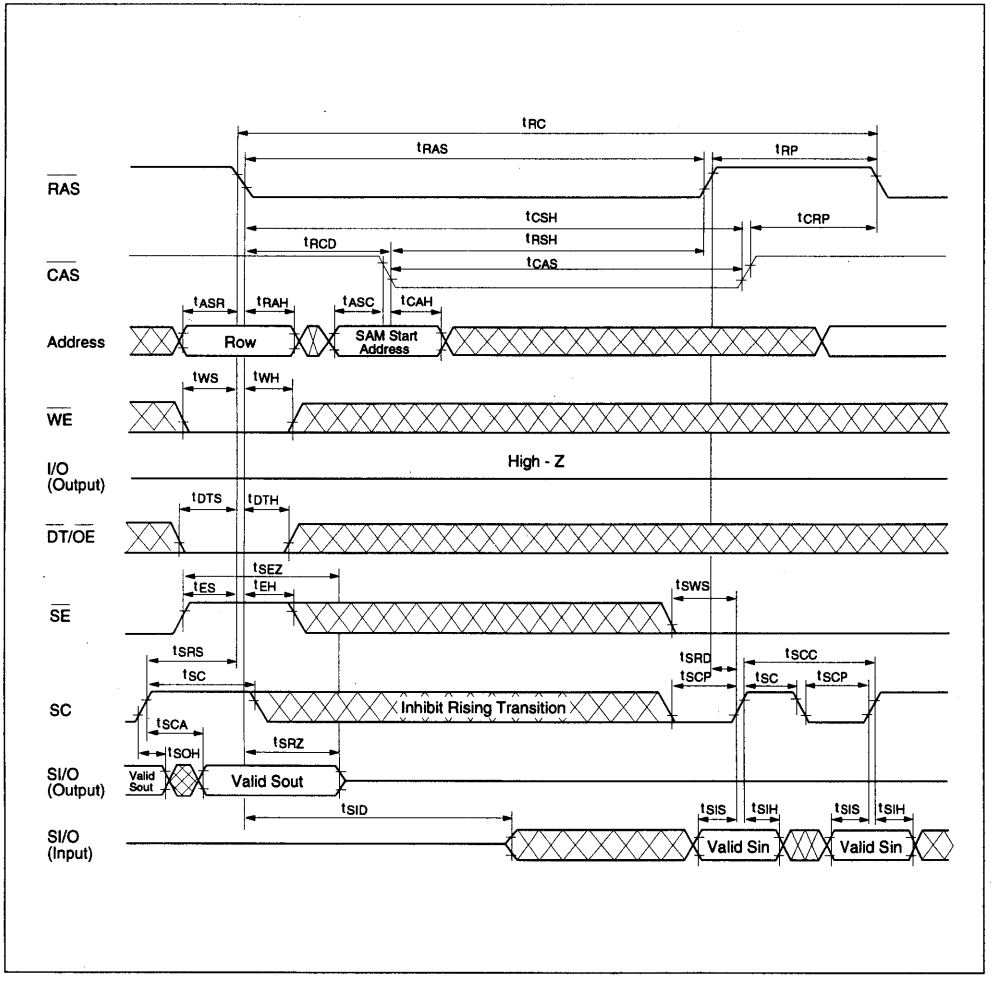
Read Transfer Cycle (1)



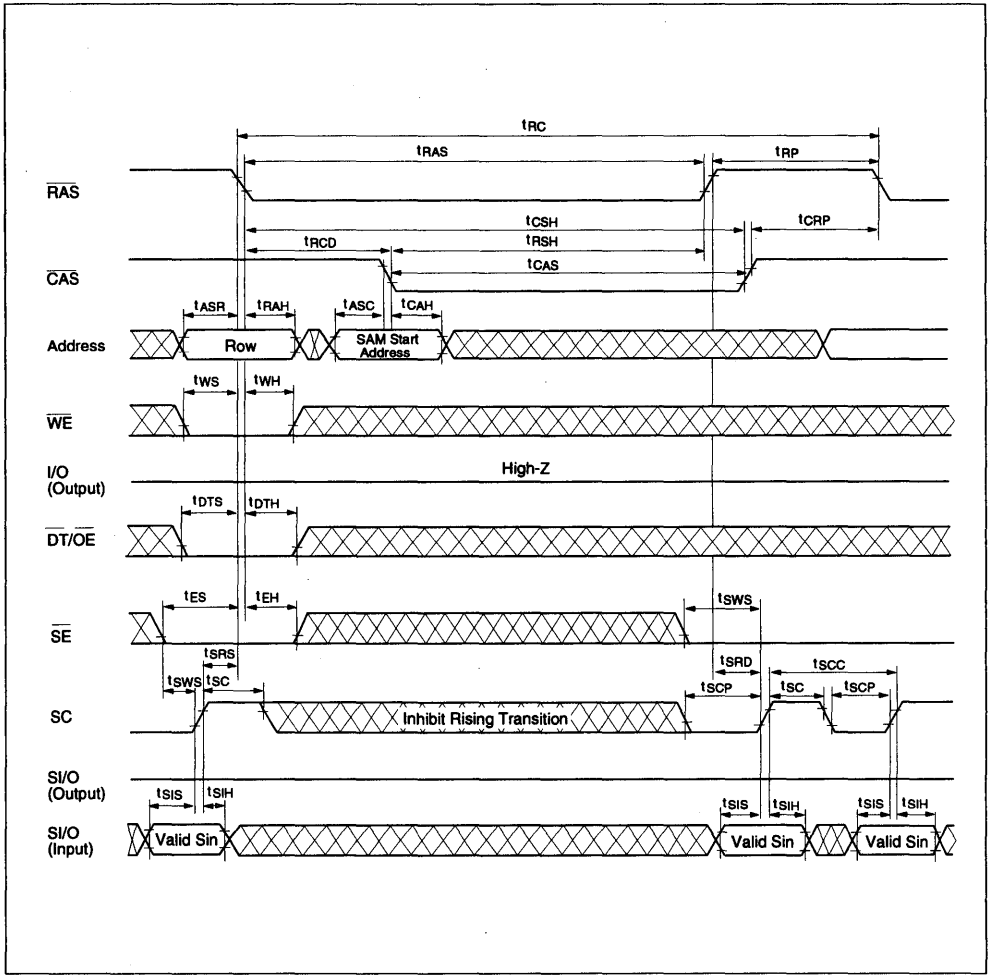
Read Transfer Cycle (2)



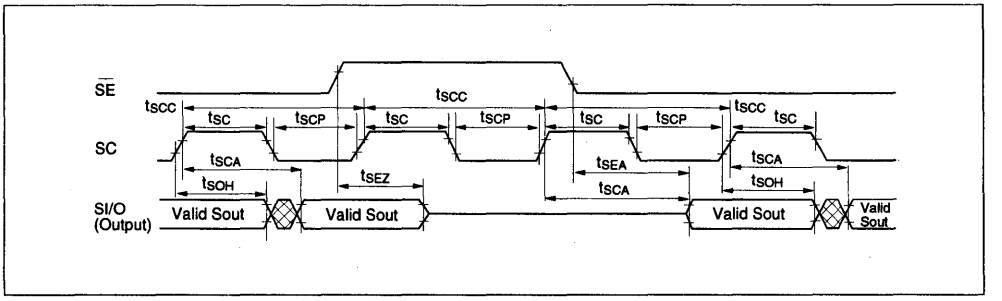
Pseudo Transfer Cycle



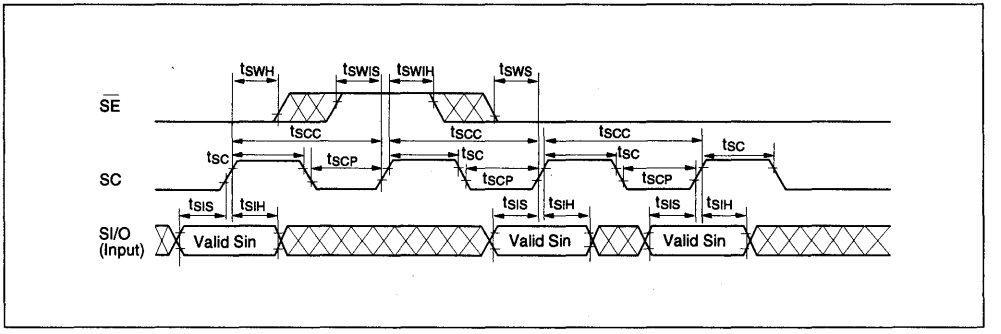
Write Transfer Cycle



Serial Read Cycle



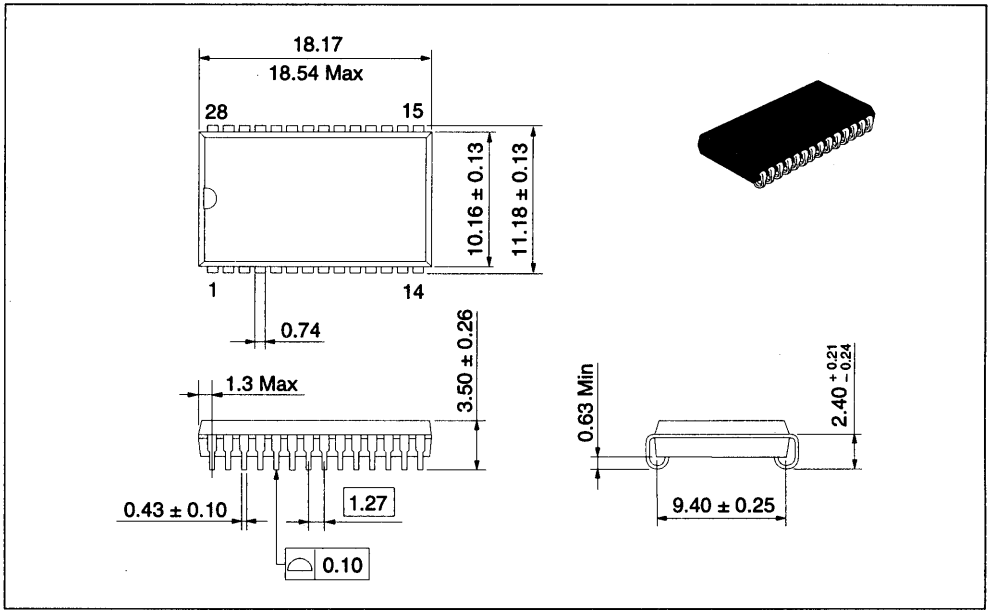
Serial Write Cycle



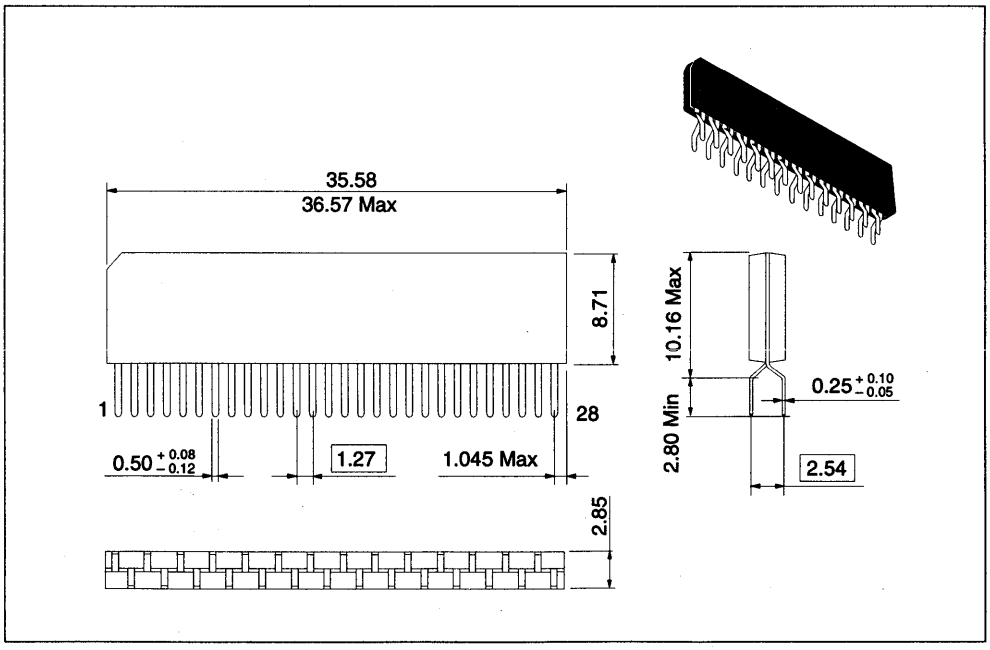
Package Dimensions

Unit: mm

HM534251BJ Series (CP-28D)



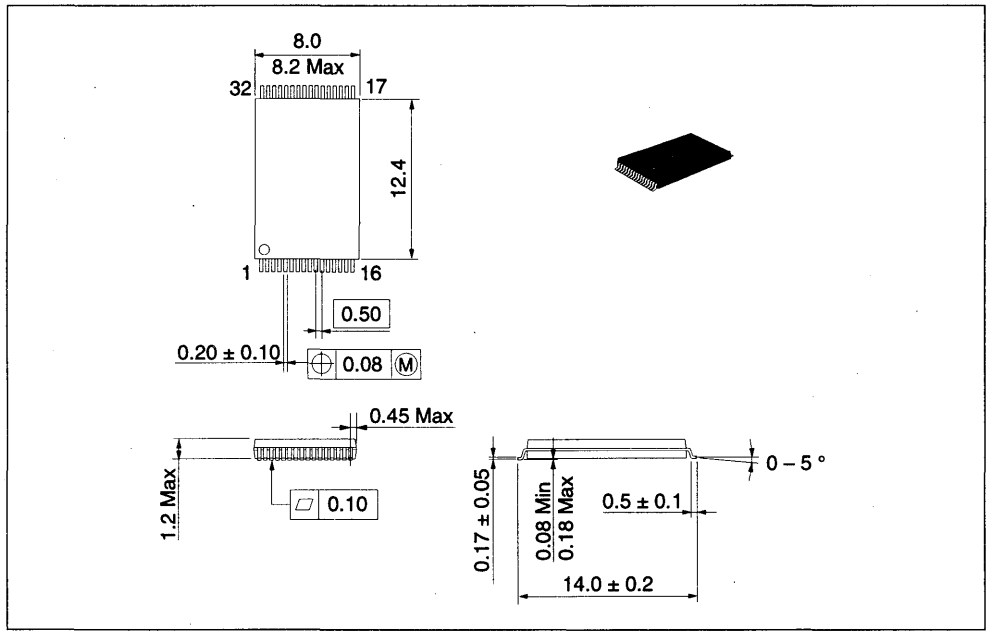
HM534251BZ Series (ZP-28)



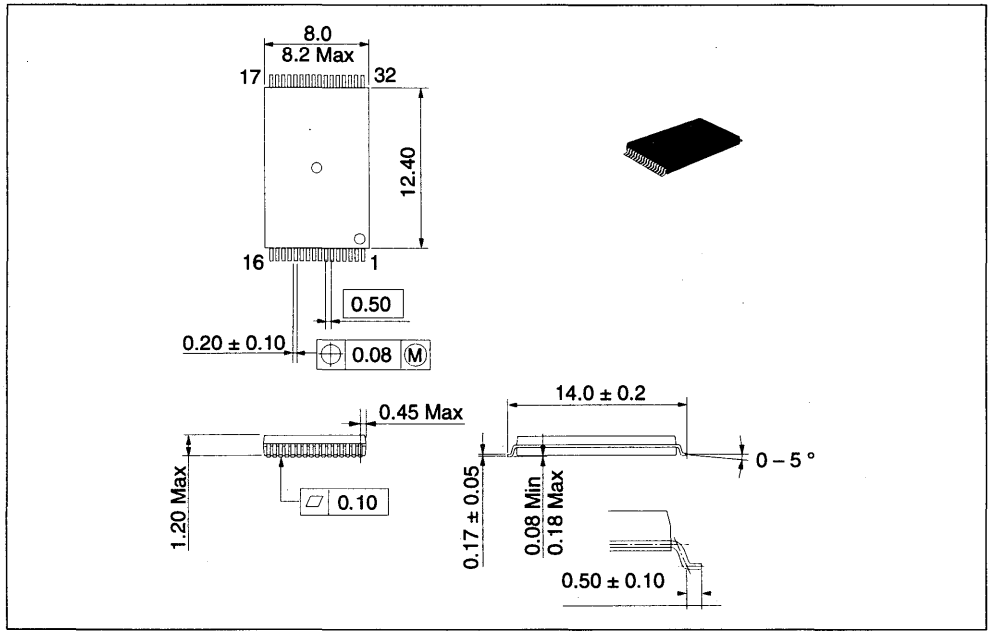
Package Dimensions (cont)

Unit: mm

HM534251BT Series (TFP-32DA)



HM534251BR Series (TFP-32DAR)



HM534253B Series

262,144-Word x 4-Bit Multiport CMOS Video RAM

HITACHI

Rev. 1
Mar, 1 1994

The HM534253B is a 1-Mbit multiport video RAM equipped with a 256-kword x 4-bit dynamic RAM and a 512-word x 4-bit SAM (serial access memory). Its RAM and SAM operate independently and asynchronously. It can transfer data between RAM and SAM. In addition, it has two modes to realize fast writing in RAM. Block write and flash write modes clear the data of 4-word x 4-bit and the data of one row (512-word x 4-bit) respectively in one cycle of RAM. And the HM534253B makes split transfer cycle possible by dividing SAM into two split buffers equipped with 256-word x 4-bit each. This cycle can transfer data to SAM which is not active, and enables a continuous serial access.

Features

- Multiport organization
  - Asynchronous and simultaneous operation of RAM and SAM capability
    - RAM: 256 kword x 4 bit
    - SAM: 512 word x 4 bit
- Access time
  - RAM: 60 ns/70 ns/80 ns/100 ns max
  - SAM: 20 ns/22 ns/25 ns/25 ns max
- Cycle time
  - RAM: 125 ns/135 ns/150 ns/180 ns min
  - SAM: 25 ns/25 ns/30 ns/30 ns min
- Low power
  - Active: RAM: 413 mW max; SAM: 275 mW max
  - Standby: 38.5 mW max
- High-speed page mode capability
- Mask write mode capability
- Bidirectional data transfer cycle between RAM and SAM capability
- Split transfer cycle capability
- Block write mode capability
- Flash write mode capability
- 3 variations of refresh (8 ms/512 cycles)
  - – $\overline{\text{RAS}}$-only refresh
  - – $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - – Hidden refresh
- TTL compatible

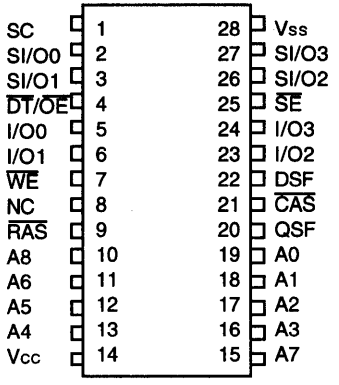
Ordering Information

Type No.	Access time	Package
HM534253BJ-6	60 ns	400-mil 28-pin plastic SOJ (CP-28D)
HM534253BJ-7	70 ns	
HM534253BJ-8	80 ns	
HM534253BJ-10	100 ns	
HM534253BZ-6	60 ns	400-mil 28-pin plastic ZIP (ZP-28)
HM534253BZ-7	70 ns	
HM534253BZ-8	80 ns	
HM534253BZ-10	100 ns	
HM534253BT-6	60 ns	8 mm x 14 mm 32-pin TSOP type I (TFP-32DA)
HM534253BT-7	70 ns	
HM534253BT-8	80 ns	
HM534253BT-10	100 ns	
HM534253BR-6	60 ns	8 mm x 14 mm 32-pin TSOP type I reverse (TFP-32DAR)
HM534253BR-7	70 ns	
HM534253BR-8	80 ns	
HM534253BR-10	100 ns	

ADE-203-204A (Z)

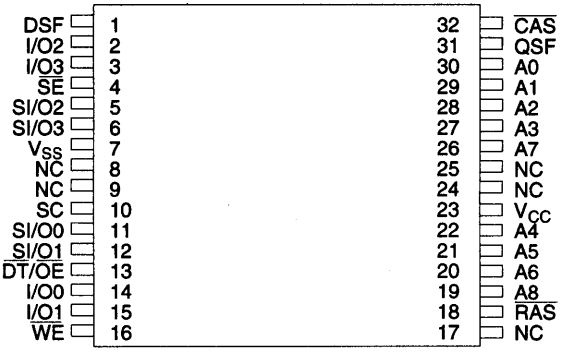
Pin Arrangement

HM534253BJ Series



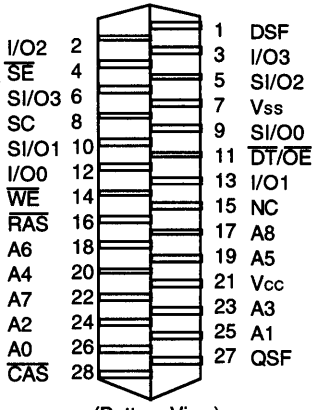
(Top View)

HM534253BT Series



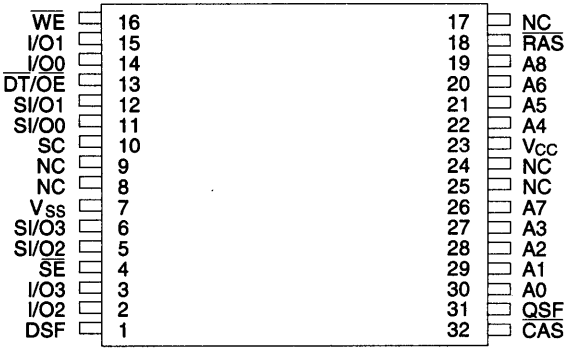
(Top View)

HM534253BZ Series



(Bottom View)

HM534253BR Series



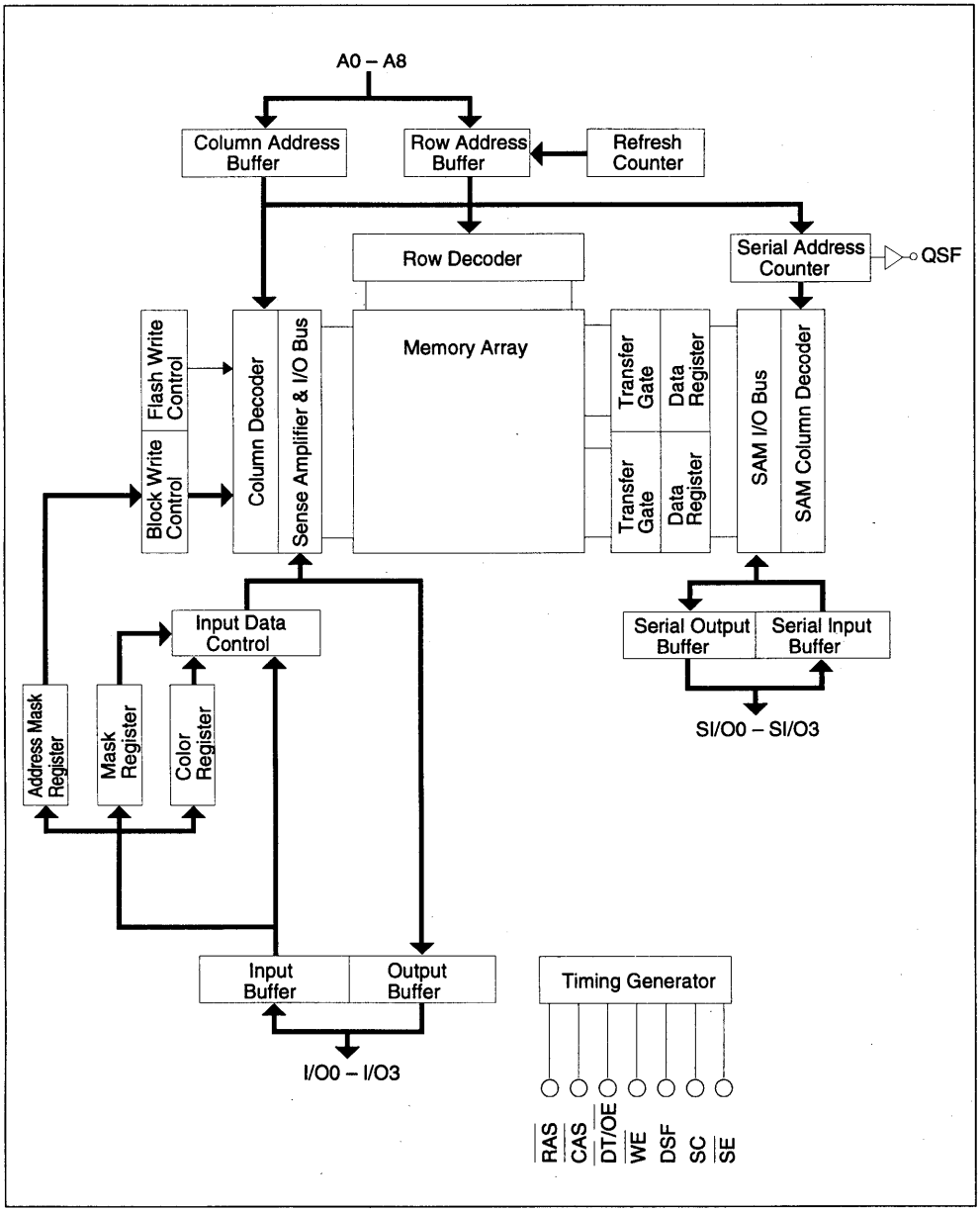
(Top View)

Pin Description

Pin name	Function
A0 – A8	Address inputs
I/O0 – I/O3	RAM port data inputs/outputs
SI/O0 – SI/O3	SAM port data inputs/outputs
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
$\overline{DT/OE}$	Data transfer/output enable

Pin name	Function
SC	Serial clock
$\overline{SE}$	SAM port enable
DSF	Special function input flag
QSF	Special function output flag
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection

Block Diagram



Pin Functions

$\overline{RAS}$ (input pin): $\overline{RAS}$ is a basic RAM signal. It is active in low level and standby in high level. Row address and signals as shown in table 1 are input at the falling edge of $\overline{RAS}$. The input level of these signals determine the operation cycle of the HM534253B.

Table 1. Operation Cycles of the HM534253B

Input level at the falling edge of $\overline{RAS}$					DSF at the falling edge of $\overline{CAS}$	Operation mode
$\overline{CAS}$	$\overline{DT/OE}$	$\overline{WE}$	$\overline{SE}$	DSF		
L	X	X	X	X	—	CBR refresh
H	L	L	L	L	X	Write transfer
H	L	L	H	L	X	Pseudo transfer
H	L	L	X	H	X	Split write transfer
H	L	H	X	L	X	Read transfer
H	L	H	X	H	X	Split read transfer
H	H	L	X	L	L	Read/mask write
H	H	L	X	L	H	Mask block write
H	H	L	X	H	X	Flash write
H	H	H	X	L	L	Read/write
H	H	H	X	L	H	Block write
H	H	H	X	H	X	Color register read/write

Note: X: Don't care.

$\overline{CAS}$ (input pin): Column address and DSF signals are fetched into chip at the falling edge of $\overline{CAS}$, which determines the operation mode of the HM534253B. $\overline{CAS}$ controls output impedance of I/O in RAM.

A0 – A8 (input pins): Row address is determined by A0 – A8 level at the falling edge of $\overline{RAS}$. Column address is determined by A0 – A8 level at the falling edge of $\overline{CAS}$. In transfer cycles, row address is the address on the word line which transfers data with SAM data register, and column address is the SAM start address after transfer.

$\overline{WE}$ (input pin): $\overline{WE}$ pin has two functions at the falling edge of $\overline{RAS}$ and after. When $\overline{WE}$ is low at the falling edge of $\overline{RAS}$, the HM534253B turns to mask write mode. According to the I/O level at the time, write on each I/O can be masked. ($\overline{WE}$ level at the falling edge of $\overline{RAS}$ is don't care in read cycle.) When $\overline{WE}$ is high at the falling edge of $\overline{RAS}$, a normal write cycle is executed. After that, $\overline{WE}$ switches read/write cycles as in a standard DRAM. In a transfer cycle, the direction of transfer is determined by $\overline{WE}$ level at the falling edge of $\overline{RAS}$. When $\overline{WE}$ is low, data is transferred from SAM to RAM (data is written into RAM), and when $\overline{WE}$ is high, data is transferred from RAM to SAM (data is read from RAM).

I/O0 – I/O3 (input/output pins): I/O pins function as mask data at the falling edge of $\overline{RAS}$ (in mask write mode). Data is written only to high I/O pins. Data on low I/O pins are masked and internal data are retained. After that, they function as input/output pins as those of a standard DRAM. In block write cycle, they function as address mask data at the falling edges of $\overline{CAS}$.

$\overline{DT/OE}$ (input pin): $\overline{DT/OE}$ pin functions as $\overline{DT}$ (data transfer) pin at the falling edge of $\overline{RAS}$ and as $\overline{OE}$ (output enable) pin after that. When $\overline{DT}$ is low at the falling edge of $\overline{RAS}$, this cycle becomes a transfer cycle. When $\overline{DT}$ is high at the falling edge of $\overline{RAS}$, RAM and SAM operate independently.

SC (input pin): SC is a basic SAM clock. In a serial read cycle, data outputs from an SI/O pin synchronously with the rising edge of SC. In a serial write cycle, data on an SI/O pin at the rising edge of SC is fetched into the SAM data register.

$\overline{SE}$ (input pin): $\overline{SE}$ pin activates SAM. When $\overline{SE}$ is high, SI/O is in the high impedance state in serial read cycle and data on SI/O is not fetched into the SAM data register in serial write cycle. $\overline{SE}$ can be used as a mask for serial write because internal pointer is incremented at the rising edge of SC.

SI/O0 – SI/O3 (input/output pins): SI/Os are input/output pins in SAM. Direction of input/output is determined by the previous transfer cycle. When it was a read transfer cycle, SI/O outputs data. When it was a pseudo transfer cycle or write transfer cycle, SI/O inputs data.

DSF (input pin): DSF is a special function data input flag pin. It is set to high at the falling edge of $\overline{RAS}$ when new functions such as color register read/write, split transfer, and flash write, are used. DSF is set to high at the falling edge of $\overline{CAS}$ when block write is executed.

QSF (output pin): QSF outputs data of address A8 in SAM. QSF is switched from low to high by accessing address 255 in SAM and from high to low by accessing 511 address in SAM.

Operation of HM534253B

RAM Port Operation

RAM Read Cycle ($\overline{DT/OE}$ high, $\overline{CAS}$ high and DSF low at the falling edge of $\overline{RAS}$, DSF low at the falling edge of $\overline{CAS}$)

Row address is entered at the $\overline{RAS}$ falling edge and column address at the $\overline{CAS}$ falling edge to the device as in standard DRAM. Then, when $\overline{WE}$ is high and $\overline{DT/OE}$ is low while $\overline{CAS}$ is low, the selected address data outputs through I/O pin. At the falling edge of $\overline{RAS}$, $\overline{DT/OE}$ and $\overline{CAS}$ become high to distinguish RAM read cycle from transfer cycle and CBR refresh cycle. Address access time (t_{AA}) and $\overline{RAS}$ to column address delay time (t_{RAD}) specifications are added to enable high-speed page mode.

RAM Write Cycle (Eraly Write, Delayed Write, Read-Modify-Write)
($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high and DSF low at the falling edge of $\overline{RAS}$, DSF low at the falling edge of $\overline{CAS}$)

- Normal Mode Write Cycle ($\overline{WE}$ high at the falling edge of $\overline{RAS}$)

When $\overline{CAS}$ and $\overline{WE}$ are set low after driving $\overline{RAS}$ low, a write cycle is executed and I/O data is written in the selected addresses. When all 4 I/Os are written, $\overline{WE}$ should be high at the falling edge of $\overline{RAS}$ to distinguish normal mode from mask write mode.
If $\overline{WE}$ is set low before the $\overline{CAS}$ falling edge, this cycle becomes an early write cycle and all I/O become in high impedance. Data is entered at the $\overline{CAS}$ falling edge.
If $\overline{WE}$ is set low after the $\overline{CAS}$ falling edge, this cycle becomes a delayed write cycle. Data is input at the $\overline{WE}$ falling. I/O does not become high impedance in this cycle, so data should be entered with $\overline{OE}$ in high.
If $\overline{WE}$ is set low after t_{CWD} (min) and t_{AWD} (min) after the $\overline{CAS}$ falling edge, this cycle becomes a read-modify-write cycle and enables read/write at the same address in one cycle. In this cycle also, to avoid I/O contention, data should be input after reading data and driving $\overline{OE}$ high.

- Mask Write Mode ($\overline{WE}$ low at the falling edge of $\overline{RAS}$)

If $\overline{WE}$ is set low at the falling edge of $\overline{RAS}$, the cycle becomes a mask write mode which writes only to selected I/O. Whether or not an I/O is written depends on I/O level (mask data) at the falling edge of $\overline{RAS}$. Then the data is written in high I/O pins and masked in low ones and internal data is retained. This mask data is effective during the $\overline{RAS}$ cycle. So, in high-speed page mode, the mask data is retained during the page access.

High-Speed Page Mode Cycle ($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high and DSF low at the falling edge of $\overline{RAS}$)

High-speed page mode cycle reads/writes the data of the same row address at high speed by toggling $\overline{CAS}$ while $\overline{RAS}$ is low. Its cycle time is one third of the random read/write cycle. In this cycle, read, write, and block write cycles can be mixed. Note that address access time (t_{AA}), $\overline{RAS}$ to column address delay time (t_{RAD}), and access time from $\overline{CAS}$ precharge (t_{ACP}) are added. In one $\overline{RAS}$ cycle, 512-word memory cells of the same row address can be accessed. It is necessary to specify access frequency within t_{RASP} max (100 µs).

Color Register Set/Read Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ high, $\overline{WE}$ high and DSF high at the falling edge of $\overline{RAS}$)

In color register set cycle, color data is set to the internal color register used in flash write cycle or block write cycle. 4 bits of internal color register are provided at each I/O. This register is composed of static circuits, so once it is set, it retains the data until reset. Color register set cycle is just as same as the usual write cycle except that DSF is set high at the falling edge of $\overline{RAS}$, and read, early write and delayed write cycle can be executed. In this cycle, the HM534253B refreshes the row address fetched at the falling edge of $\overline{RAS}$.

Flash Write Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ high, $\overline{WE}$ low, and DSF high at the falling edge of $\overline{RAS}$)

In a flash write cycle, a row of data (512 word x 4 bit) is cleared to 0 or 1 at each I/O according to the data of color register mentioned before. It is also necessary to mask I/O in this cycle. When $\overline{CAS}$ and $\overline{DT}/\overline{OE}$ is set high, $\overline{WE}$ is low, and DSF is high at the falling edge of $\overline{RAS}$, this cycle starts. Then, the row address to clear is given to row address and mask data is given to I/O. Mask data is as same as that of a RAM write cycle. High I/O is cleared, low I/O is not cleared and the internal data is retained. Cycle time is the same as those of RAM read/write cycles, so all bits can be cleared in 1/512 of the usual cycle time. (See figure 1.)

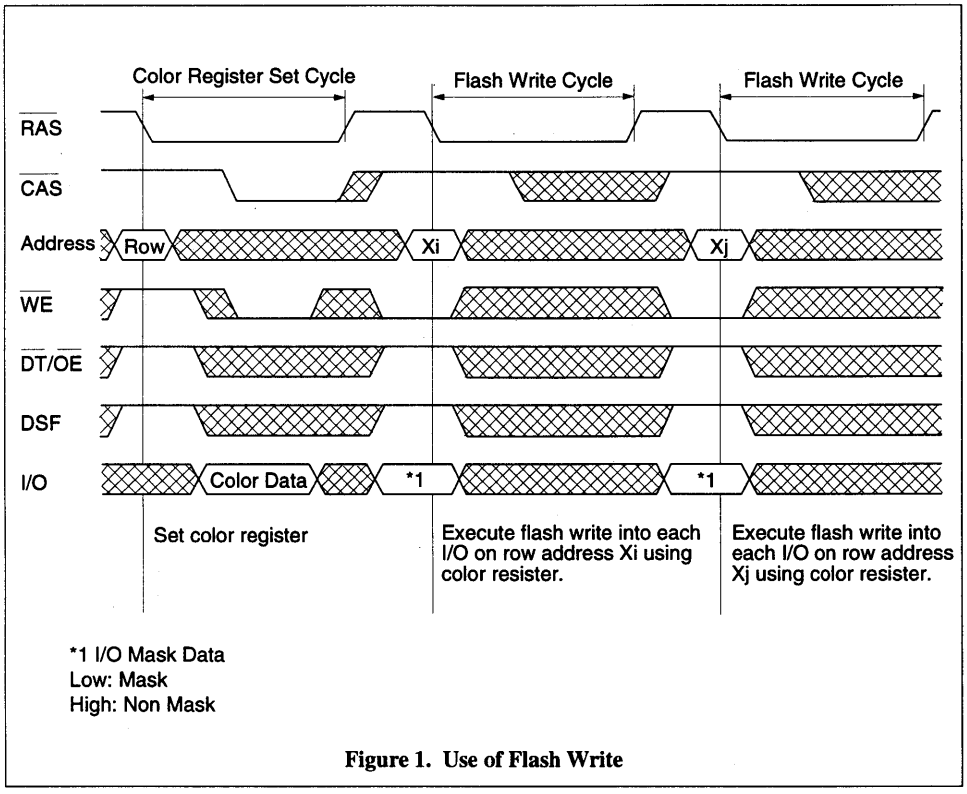


Figure 1. Use of Flash Write

Block Write cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ high and DSF low at the falling edge of $\overline{RAS}$, DSF high at the falling edge of $\overline{CAS}$)

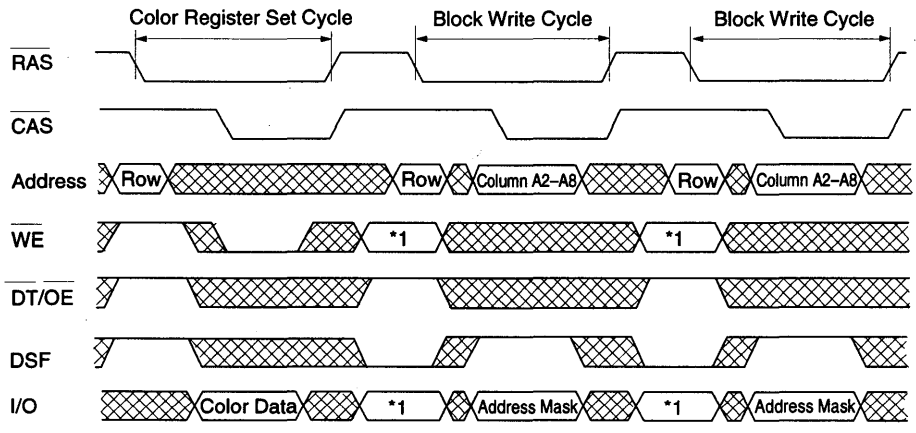
In a block write cycle, 4 columns of data (4 word x 4 bit) is cleared to 0 or 1 at each I/O according to the data of color register. Column addresses A0 and A1 are disregarded. The data on I/Os and addresses can be masked. I/O level at the falling edge of $\overline{CAS}$ determines the address to be cleared. (See figure 2.) In a page mode cycle, mixed cycle of normal Read/Write and block write can be allowed by controlling DSF.

- Normal Mode Block Write Cycle ($\overline{WE}$ high at the falling edge of $\overline{RAS}$)

The data on 4 I/Os are all cleared when $\overline{WE}$ is high at the falling edge of $\overline{RAS}$.

- Mask Block Write Mode ($\overline{WE}$ low at the falling edge of $\overline{RAS}$)

When $\overline{WE}$ is low at the falling edge of $\overline{RAS}$, the HM534253B starts mask block write mode to clear the data on an optional I/O. The mask data is the same as that of a RAM write cycle. High I/O is cleared, low I/O is not cleared and the internal data is retained. The mask data is available in the $\overline{RAS}$ cycle. In page mode block write cycle, the mask data is retained during the page access.



*1

$\overline{WE}$	I/O	Mode
Low	I/O Mask Data	Mask
High	Don't care	Non mask

I/O Mask Data
Low: Mask
High: Non Mask

Address Mask Data

I/O0	Column0 (A0 = 0, A1 = 0) Mask Data	Low: Mask
I/O1	Column1 (A0 = 1, A1 = 0) Mask Data	
I/O2	Column2 (A0 = 0, A1 = 1) Mask Data	High: Non Mask
I/O3	Column3 (A0 = 1, A1 = 1) Mask Data	

Figure 2. Use of Block Write

Transfer Operation

The HM534253B provides the read transfer cycle, split read transfer cycle,pseudo transfer cycle, write transfer cycle, and split write transfer cycle as data transfer cycles. These transfer cycles are set by driving $\overline{CAS}$ high and $\overline{DT/OE}$ low at the falling edge of $\overline{RAS}$. They have following functions:

(1) Transfer data between row address and SAM data register (except for pseudo transfer cycle)
- Read transfer cycle and split read transfer cycle: RAM to SAM
- Write transfer cycle and split write transfer cycle: SAM to RAM

(2) Determine SI/O state (except for split read transfer cycle and split write transfer cycle)
- Read transfer cycle: SI/O output
- Pseudo transfer cycle and write transfer cycle: SI/O input

(3) Determine first SAM address to access after transferring at column address (SAM start address).

SAM start address must be determined by read transfer cycle or pseudo transfer cycle (split transfer cycle isn't available) before SAM access, after power on, and determined for each transfer cycle.

Read Transfer Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ low, $\overline{WE}$ high and DSF low at the falling edge of $\overline{RAS}$)

This cycle becomes read transfer cycle by driving $\overline{DT/OE}$ low, $\overline{WE}$ high and DSF low at the falling edge of $\overline{RAS}$. The row address data (512 x 4 bits) determined by this cycle is transferred to SAM data register synchronously at the rising edge of $\overline{DT/OE}$. After the rising edge of $\overline{DT/OE}$, the new address data outputs from SAM start address determined by column address. In read transfer cycle, $\overline{DT/OE}$ must be risen to transfer data from RAM to SAM.

This cycle can access SAM even during transfer (real time read transfer). In this case, the timing t_{SDD} (min) specified between the last SAM access before transfer and $\overline{DT/OE}$ rising edge and t_{SDH} (min) specified between the first SAM access and $\overline{DT/OE}$ rising edge must be satisfied. (See figure 3.)

When read transfer cycle is executed, SI/O becomes output state by first SAM access. Input must be set high impedance before t_{SZS} (min) of the first SAM access to aviod data contention.

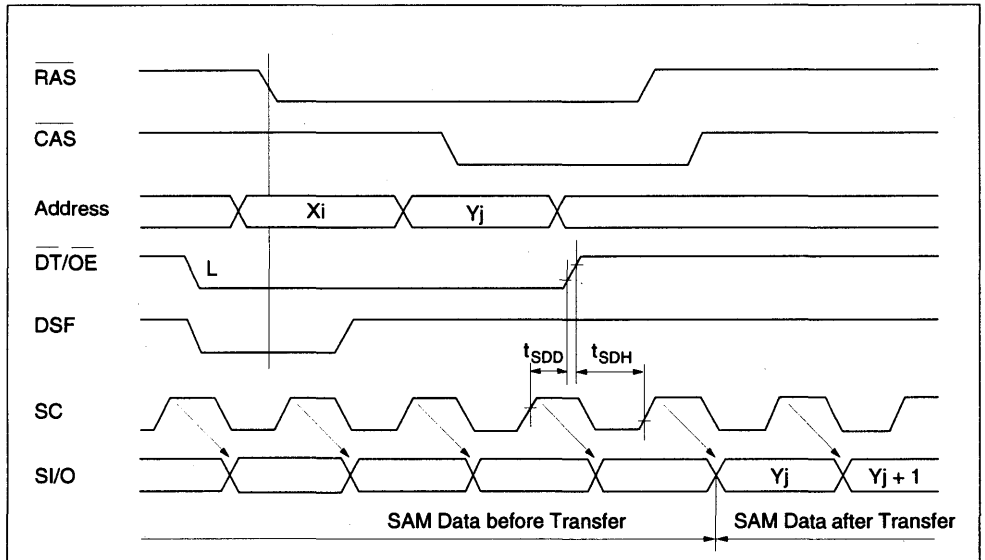


Figure 3 Real Time Read Transfer

Pseudo Transfer Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ low, $\overline{WE}$ low, $\overline{SE}$ high and DSF low at the falling edge of $\overline{RAS}$)

Pseudo transfer cycle switches SI/O to input state and set SAM start address without data transfer to RAM. This cycle starts when $\overline{CAS}$ is high, $\overline{DT/OE}$ low, $\overline{WE}$ low, $\overline{SE}$ high and DSF low at the falling edge of $\overline{RAS}$. Data should be input to SI/O later than t_{SID} (min) after $\overline{RAS}$ becomes low to avoid data contention. SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. In this cycle, SAM access is inhibited during $\overline{RAS}$ low, therefore, SC must not be risen.

Write Transfer cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ low, $\overline{WE}$ low, $\overline{SE}$ low, and DSF low at the falling edge of $\overline{RAS}$)

Write transfer cycle can transfer a row of data input by serial write cycle to RAM. The row address of data transferred into RAM is determined by the address at the falling edge of $\overline{RAS}$. The column address is specified as the first address for serial write after terminating this cycle. Also in this cycle, SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. SAM access is inhibited during $\overline{RAS}$ low. In this period, SC must not be risen. Data transferred to SAM by read transfer cycle or split read transfer cycle can be written to other addresses of RAM by write transfer cycle. However, the address to write data must be the same MSB of row address (AX8) as that of the read transfer cycle.

Split Read Transfer Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ low, $\overline{WE}$ high and DSF high at the falling edge of $\overline{RAS}$)

To execute a continuous serial read by real time read transfer, the HM534253B must satisfy SC and $\overline{DT/OE}$ timings and requires an external circuit to detect SAM last address. Split read transfer cycle makes it possible to execute a continuous serial read without the above timing limitation. Figure 4 shows the block diagram for a split transfer. SAM data register (DR) consists of 2 split buffers, whose organizations are 256-word x 4-bit each. Let us suppose that data is read from upper data reagister DR1 (The row address AX8 is 0 and SAM address A8 is 1.). When split read transfer is executed setting row address AX8 0 and SAM start addresses A0 to A7, 256-word x 4-bit data are transferred from RAM to the lower data register DR0 (SAM address A8 is 0) automatically. After data are read from data register DR1, data start to be read from SAM start addresses of data register DR0. If the next split read transfer isn't executed while data are read from data register DR0, data start to be read from SAM start address 0 of DR1 after data are read from data register DR0. If split read transfer is executed setting row address AX8 1 and SAM start addresses A0 to A7 while data are read from data register DR1, 256-word x 4-bit data are transferred to data register DR2. After data are read from data register DR1, data start to be read from SAM start addresses of data register DR2. If the next split read transfer isn't executed while data is read from data register DR2, data start to be read from SAM start address 0 of data register DR3 after data are read from data register DR2. In this time, SAM data is the one transferred to data register DR3 finally while row address AX8 is 1. In split read data transfer, the SAM start address A8 is automatically set in the data register which isn't used.

The data on SAM address A8, which will be accessed next, outputs to QSF. QSF is switched from low to high by accessing SAM last address 255 and from high to low by accessing address 511.

Split read transfer cycle is set when $\overline{CAS}$ is high, $\overline{DT}/\overline{OE}$ is low, $\overline{WE}$ is high and DSF is high at the falling edge of $\overline{RAS}$. The cycle can be executed asyncronously with SC. However, t_{STS} (min) timing specified between SC rising and $\overline{RAS}$ falling must be satisfied. SAM last address must be accessed, satisfying t_{RST} (min), t_{CST} (min), and t_{AST} (min) timings specified between $\overline{RAS}$ or $\overline{CAS}$ falling and column address. (See figure 5.)

In split read transfer, SI/O isn't switched to output state. Therefore, read transfer must be executed to switch SI/O to output state when the previous transfer cycle is pseudo transfer or write transfer cycle.

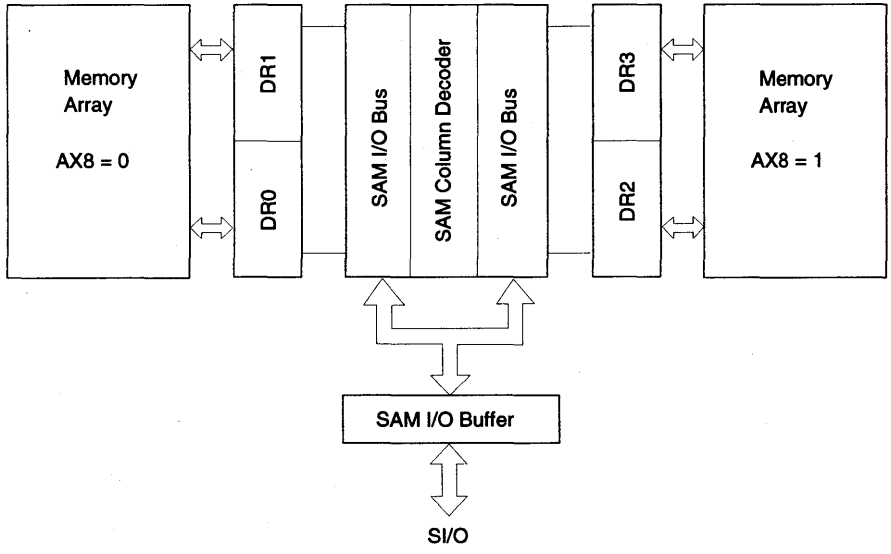


Figure 4. Block Diagram for Split Transfer

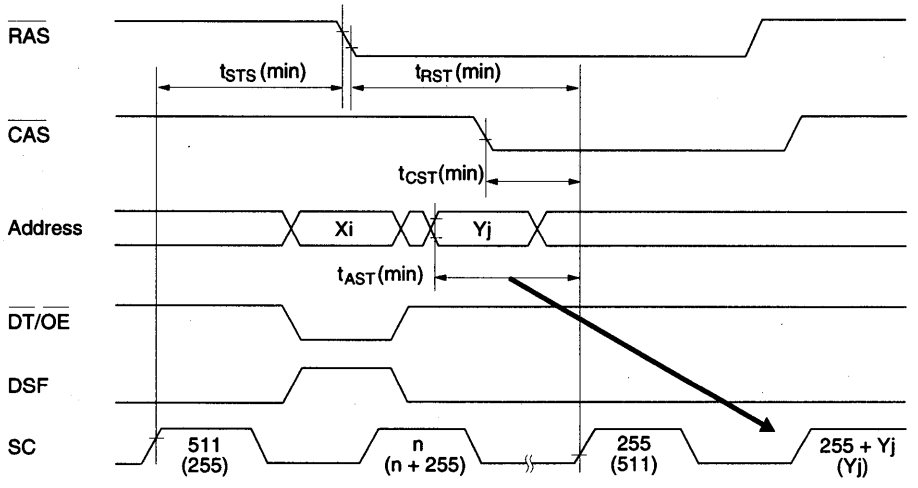


Figure 5 Limitation in Split Transfer

Split Write Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low and DSF high at the falling edge of $\overline{RAS}$)

A continuous serial write cannot be executed because accessing SAM is inhibited during $\overline{RAS}$ low in write transfer. Split write transfer cycle makes it possible. In this cycle, t_{STS} (min), t_{RST} (min), t_{CST} (min) and t_{AST} (min) timings must be satisfied like split read transfer cycle. And it is impossible to switch SI/O to input state in this cycle. If SI/O is in output state, pseudo transfer cycle should be executed to switch SI/O into input state. Data transferred to SAM by read transfer cycle or split read transfer cycle can be written to other addresses of RAM by split write transfer cycle. However, pseudo transfer cycle must be executed before split write transfer cycle. And the MSB of row address (AX8) to write data must be the same as that of the read transfer cycle or the split read transfer cycle.

SAM Port Operation

Serial Read Cycle

SAM port is in read mode when the previous data transfer cycle is read transfer cycle. Access is synchronized with SC rising, and SAM data is output from SI/O. When $\overline{SE}$ is set high, SI/O becomes high impedance, and the internal pointer is incremented by the SC rising. After indicating the last address (address 511), the internal pointer indicates address 0 at the next access.

Serial Write Cycle

If previous data transfer cycle is pseudo transfer cycle or write transfer cycle, SAM port goes into write mode. In this cycle, SI/O data is fetched into data register at the SC rising edge like in the serial read cycle. If $\overline{SE}$ is high, SI/O data isn't fetched into data register. Internal pointer is incremented by the SC rising, so $\overline{SE}$ high can be used as mask data for SAM. After indicating the last address (address 511), the internal pointer indicates address 0 at the next access.

Refresh

RAM Refresh

RAM, which is composed of dynamic circuits, requires refresh to retain data. Refresh is executed by accessing all 512 row addresses within 8 ms. There are three refresh cycles: (1) $\overline{RAS}$-only refresh cycle, (2) $\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh cycle, and (3) Hidden refresh cycle. Besides them, the cycles which activate $\overline{RAS}$ such as read/write cycles or transfer cycles can refresh the row address. Therefore, no refresh cycle is required when all row addresses are accessed within 8 ms.

(1) $\overline{RAS}$-Only Refresh Cycle: $\overline{RAS}$-only refresh cycle is executed by activating only $\overline{RAS}$ cycle with $\overline{CAS}$ fixed to high after inputting the row address (= refresh address) from external circuits. To distinguish this cycle from data transfer cycle, $\overline{DT}/\overline{OE}$ must be high at the falling edge of $\overline{RAS}$.

(2) CBR Refresh Cycle: CBR refresh cycle is set by activating $\overline{CAS}$ before $\overline{RAS}$. In this cycle, refresh address need not to be input through external circuits because it is input through an internal refresh counter. In this cycle, output is in high impedance and power dissipation is lowered because $\overline{CAS}$ circuits don't operate.

(3) Hidden Refresh Cycle: Hidden refresh cycle executes CBR refresh with the data output by reactivating $\overline{RAS}$ when $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ keep low in normal RAM read cycles.

SAM Refresh

SAM parts (data register, shift resister and selector), organized as fully static circuitry, require no refresh.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to V_{SS}	V_T	−1.0 to +7.0	V	1
Supply voltage relative to V_{SS}	V_{CC}	−0.5 to +7.0	V	1
Short circuit output current	Iout	50	mA	
Power dissipation	P_T	1.0	W	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	−55 to +125	°C	

Note 1. Relative to V_{SS}.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage*1	V_{CC}	4.5	5.0	5.5	V	1
Input high voltage*1	V_{IH}	2.4	—	6.5	V	1
Input low voltage*1	V_{IL}	−0.5*2	—	0.8	V	1

Notes: 1. All voltage referred to V_{SS}
2 −3.0 V for pulse width ≤ 10 ns.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

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		-6		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Test conditions
Operating current	I_{CC1}	—	75	—	70	—	60	—	55	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min; $SC = V_{IL}$, $\overline{SE} = V_{IH}$
	I_{CC7}	—	125	—	120	—	100	—	95	mA	$\overline{SE} = V_{IL}$, SC cycling; t_{SCC} = min
Standby current	I_{CC2}	—	7	—	7	—	7	—	7	mA	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}; $SC = V_{IL}$, $\overline{SE} = V_{IH}$
	I_{CC8}	—	50	—	50	—	40	—	40	mA	$\overline{SE} = V_{IL}$, SC cycling; t_{SCC} = min
$\overline{RAS}$-only refresh current	I_{CC3}	—	75	—	70	—	60	—	55	mA	$\overline{RAS}$ cycling; $\overline{CAS} = V_{IH}$; t_{RC} = min; $SC = V_{IL}$, $\overline{SE} = V_{IH}$
	I_{CC9}	—	125	—	120	—	100	—	95	mA	$\overline{SE} = V_{IL}$, SC cycling; t_{SCC} = min
Page mode current	I_{CC4}	—	80	—	80	—	70	—	65	mA	$\overline{CAS}$ cycling; $\overline{RAS} = V_{IL}$; t_{PC} = min; $SC = V_{IL}$, $\overline{SE} = V_{IH}$
	I_{CC10}	—	130	—	130	—	110	—	105	mA	$\overline{SE} = V_{IL}$, SC cycling; t_{SCC} = min
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC5}	—	50	—	45	—	40	—	35	mA	$\overline{RAS}$ cycling; t_{RC} = min; $SC = V_{IL}$, $\overline{SE} = V_{IH}$
	I_{CC11}	—	100	—	95	—	80	—	75	mA	$\overline{SE} = V_{IL}$, SC cycling; t_{SCC} = min
Data transfer current	I_{CC6}	—	80	—	75	—	65	—	60	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min; $SC = V_{IL}$, $\overline{SE} = V_{IH}$
	I_{CC12}	—	130	—	125	—	105	—	100	mA	$\overline{SE} = V_{IL}$, SC cycling; t_{SCC} = min
Input leakage current	I_{LI}	−10	10	−10	10	−10	10	−10	10	µA	
Output leakage current	I_{LO}	−10	10	−10	10	−10	10	−10	10	µA	
Output high voltage	V_{OH}	2.4	—	2.4	—	2.4	—	2.4	—	V	I_{OH} = −2 mA
Output low voltage	V_{OL}	—	0.4	—	0.4	—	0.4	—	0.4	V	I_{OL} = 4.2 mA

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed once while $\overline{RAS}$ is low and $\overline{CAS}$ is high.

Capacitance (Ta = 25°C, V_{CC} = 5 V, f = 1 MHz, Bias: Clock, I/O = V_{CC}, address = V_{SS})

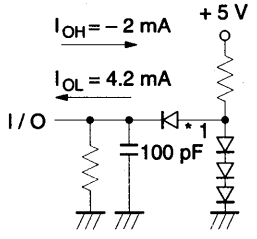
Parameter	Symbol	Typ	Max	Unit	Note
Input capacitance (Address)	C_{I1}	—	5	pF	1
Input capacitance (Clocks)	C_{I2}	—	5	pF	1
Output capacitance (I/O, SI/O, QSF)	$C_{I/O}$	—	7	pF	1

Note: 1. This parameter is sampled and not 100% tested.

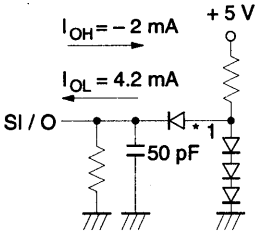
AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V) *1, *16

Test Conditions

- Input rise and fall times: 5 ns
- Input pulse levels: V_{SS} to 3.0 V
- Input timing reference levels: 0.8 V, 2.4 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: See figures



Output Load (A)



Output Load (B)

Common Parameter

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		-6		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Random read or write cycle time	t_{RC}	125	—	135	—	150	—	180	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	55	—	55	—	60	—	70	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	—	20	—	20	—	25	—	ns	

Common Parameter (cont)

		HM534253B									
		-6		-7		-8		-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Row address setup time	t_{ASR}	0	—	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	15	—	15	—	15	—	15	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	20	60	20	75	ns	2
$\overline{RAS}$ hold time referenced to $\overline{CAS}$	t_{RSH}	20	—	20	—	20	—	25	—	ns	
$\overline{CAS}$ hold time referenced to $\overline{RAS}$	t_{CSH}	60	—	70	—	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	10	—	10	—	ns	
Transition time (rise to fall)	t_T	3	50	3	50	3	50	3	50	ns	3
Refresh period	t_{REF}	—	8	—	8	—	8	—	8	ms	
$\overline{DT}$ to $\overline{RAS}$ setup time	t_{DTS}	0	—	0	—	0	—	0	—	ns	
$\overline{DT}$ to $\overline{RAS}$ hold time	t_{DTH}	10	—	10	—	10	—	10	—	ns	
DSF to $\overline{RAS}$ setup time	t_{FSR}	0	—	0	—	0	—	0	—	ns	
DSF to $\overline{RAS}$ hold time	t_{RFH}	10	—	10	—	10	—	10	—	ns	
DSF to $\overline{CAS}$ setup time	t_{FSC}	0	—	0	—	0	—	0	—	ns	
DSF to $\overline{CAS}$ hold time	t_{CFH}	15	—	15	—	15	—	15	—	ns	
Data-in to $\overline{CAS}$ delay time	t_{DZC}	0	—	0	—	0	—	0	—	ns	4
Data-in to $\overline{OE}$ delay time	t_{DZO}	0	—	0	—	0	—	0	—	ns	4
Output buffer turn-off delay referenced to $\overline{CAS}$	t_{OFF1}	—	20	—	20	—	20	—	20	ns	5
Output buffer turn-off delay referenced to $\overline{OE}$	t_{OFF2}	—	20	—	20	—	20	—	20	ns	5

Read Cycle (RAM), Page Mode Read Cycle

		HM534253B									
		-6		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Access time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	ns	6, 7
Access time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	20	—	25	ns	7, 8
Access time from $\overline{OE}$	t_{OAC}	—	20	—	20	—	20	—	25	ns	7
Address access time	t_{AA}	—	35	—	35	—	40	—	45	ns	7, 9
Read command setup time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	0	—	0	—	ns	10
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	10	—	ns	10
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	35	15	40	15	55	ns	2
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	—	35	—	40	—	45	—	ns	
Column address to $\overline{CAS}$ lead time	t_{CAL}	35	—	35	—	40	—	45	—	ns	
Page mode cycle time	t_{PC}	45	—	45	—	50	—	55	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	—	10	—	10	—	10	—	ns	
Access time from $\overline{CAS}$ precharge	t_{ACP}	—	40	—	40	—	45	—	50	ns	
Page mode $\overline{RAS}$ pulse width	t_{RASP}	60	100000	70	100000	80	100000	100	100000	ns	

Write Cycle (RAM), Page Mode Write Cycle, Color Register Set Cycle

		HM534253B									
		-6		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Write command setup time	t_{WCS}	0	—	0	—	0	—	0	—	ns	11
Write command hold time	t_{WCH}	15	—	15	—	15	—	15	—	ns	
Write command pulse width	t_{WP}	15	—	15	—	15	—	15	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	—	20	—	20	—	20	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	—	20	—	20	—	20	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	0	—	ns	12
Data-in hold time	t_{DH}	15	—	15	—	15	—	15	—	ns	12
$\overline{WE}$ to $\overline{RAS}$ setup time	t_{WS}	0	—	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ hold time	t_{WH}	10	—	10	—	10	—	10	—	ns	
Mask data to $\overline{RAS}$ setup time	t_{MS}	0	—	0	—	0	—	0	—	ns	
Mask data to $\overline{RAS}$ hold time	t_{MH}	10	—	10	—	10	—	10	—	ns	
$\overline{OE}$ hold time referenced to $\overline{WE}$	t_{OEH}	20	—	20	—	20	—	20	—	ns	
Page mode cycle time	t_{PC}	45	—	45	—	50	—	55	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ to data-in delay time	t_{CDD}	20	—	20	—	20	—	20	—	ns	13
Page mode $\overline{RAS}$ pulse width	t_{RASP}	60	100000	70	100000	80	10000	100	100000		ns

Read-Modify-Write Cycle

		HM534253B									
		-6		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Read-modify-write cycle time	t_{RWC}	175	—	185	—	200	—	230	—	ns	
$\overline{RAS}$ pulse width (read-modify-write cycle)	t_{RWS}	110	10000	120	10000	130	10000	150	10000	ns	
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	45	—	45	—	45	—	50	—	ns	14
Column address to $\overline{WE}$ delay time	t_{AWD}	60	—	60	—	65	—	70	—	ns	14
$\overline{OE}$ to data-in delay time	t_{ODD}	20	—	20	—	20	—	20	—	ns	12
Access time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	ns	6, 7
Access time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	20	—	25	ns	7, 8
Access time from $\overline{OE}$	t_{OAC}	—	20	—	20	—	20	—	25	ns	7
Address access time	t_{AA}	—	35	—	35	—	40	—	45	ns	7, 9
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	35	15	40	15	55	ns	
Read command setup time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	—	20	—	20	—	20	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	—	20	—	20	—	20	—	ns	
Write command pulse width	t_{WP}	15	—	15	—	15	—	15	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	0	—	ns	12
Data-in hold time	t_{DH}	15	—	15	—	15	—	15	—	ns	12
$\overline{OE}$ hold time referenced to $\overline{WE}$	t_{OEH}	20	—	20	—	20	—	20	—	ns	

Refresh Cycle

		HM534253B									
		-6		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10	—	10	—	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	—	10	—	10	—	10	—	ns	

Flash Write Cycle, Block Write Cycle

		HM534253B									
		-6		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{CAS}$ to data-in delay time	t_{CDD}	20	—	20	—	20	—	20	—	ns	13
$\overline{OE}$ to data-in delay time	t_{ODD}	20	—	20	—	20	—	20	—	ns	13

Read Transfer Cycle

		HM534253B									
		-6		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{DT}$ hold time referenced to $\overline{RAS}$	t_{RDH}	50	10000	60	10000	65	10000	80	10000	ns	
$\overline{DT}$ hold time referenced to $\overline{CAS}$	t_{CDH}	20	—	20	—	20	—	25	—	ns	
$\overline{DT}$ hold time referenced to column address	t_{ADH}	25	—	25	—	30	—	30	—	ns	
$\overline{DT}$ precharge time	t_{DTP}	20	—	20	—	20	—	30	—	ns	
$\overline{DT}$ to $\overline{RAS}$ delay time	t_{DRD}	65	—	65	—	70	—	80	—	ns	
SC to $\overline{RAS}$ setup time	t_{SRS}	25	—	25	—	30	—	30	—	ns	
1st SC to $\overline{RAS}$ hold time	t_{SRH}	60	—	70	—	80	—	100	—	ns	

Read Transfer Cycle (cont)

		HM534253B									
		-6		-7		-8		-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
1st SC to $\overline{CAS}$ hold time	t_{SCH}	25	—	25	—	25	—	25	—	ns	
1st SC to column address hold time	t_{SAH}	40	—	40	—	45	—	50	—	ns	
Last SC to $\overline{DT}$ delay time	t_{SDD}	5	—	5	—	5	—	5	—	ns	
1st SC to $\overline{DT}$ hold time	t_{SDH}	10	—	10	—	15	—	15	—	ns	
$\overline{RAS}$ to QSF delay time	t_{RQD}	—	65	—	70	—	75	—	85	ns	15
$\overline{CAS}$ to QSF delay time	t_{CQD}	—	35	—	35	—	40	—	40	ns	15
$\overline{DT}$ to QSF delay time	t_{DQD}	—	35	—	35	—	35	—	35	ns	15
QSF hold time referenced to $\overline{RAS}$	t_{RQH}	20	—	20	—	20	—	25	—	ns	
QSF hold time referenced to $\overline{CAS}$	t_{CQH}	5	—	5	—	5	—	5	—	ns	
QSF hold time referenced to $\overline{DT}$	t_{DQH}	5	—	5	—	5	—	5	—	ns	
Serial data-in to 1st SC delay time	t_{SZS}	0	—	0	—	0	—	0	—	ns	
Serial clock cycle time	t_{SCC}	25	—	25	—	30	—	30	—	ns	
SC pulse width	t_{SC}	5	—	5	—	10	—	10	—	ns	
SC precharge time	t_{SCP}	10	—	10	—	10	—	10	—	ns	
SC access time	t_{SCA}	—	20	—	22	—	25	—	25	ns	15
Serial data-out hold time	t_{SOH}	5	—	5	—	5	—	5	—	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	15	—	15	—	15	—	ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	35	15	40	15	55	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	—	35	—	40	—	45	—	ns	
$\overline{RAS}$ precharge to $\overline{DT}$ high hold time	t_{DTHH}	10	—	10	—	10	—	10	—	ns	18

Pseudo Transfer Cycle, Write Transfer Cycle

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		-6		-7		-8		-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
$\overline{SE}$ setup time referenced to $\overline{RAS}$	t_{ES}	0	—	0	—	0	—	0	—	ns	
$\overline{SE}$ hold time referenced to $\overline{RAS}$	t_{EH}	10	—	10	—	10	—	10	—	ns	
SC setup time referenced to $\overline{RAS}$	t_{SRS}	25	—	25	—	30	—	30	—	ns	
$\overline{RAS}$ to SC delay time	t_{SRD}	20	—	20	—	25	—	25	—	ns	
Serial output buffer turn-off time referenced to $\overline{RAS}$	t_{SRZ}	10	40	10	40	10	45	10	50	ns	
$\overline{RAS}$ to serial data-in delay time	t_{SID}	40	—	40	—	45	—	50	—	ns	
$\overline{RAS}$ to QSF delay time	t_{RQD}	—	65	—	70	—	75	—	85	ns	15
$\overline{CAS}$ to QSF delay time	t_{CQD}	—	35	—	35	—	40	—	40	ns	15
QSF hold time referenced to $\overline{RAS}$	t_{RQH}	20	—	20	—	20	—	25	—	ns	
QSF hold time referenced to $\overline{CAS}$	t_{CQH}	5	—	5	—	5	—	5	—	ns	
Serial clock cycle time	t_{SCC}	25	—	25	—	30	—	30	—	ns	
SC pulse width	t_{SC}	5	—	5	—	10	—	10	—	ns	
SC precharge time	t_{SCP}	10	—	10	—	10	—	10	—	ns	
SC access time	t_{SCA}	—	20	—	22	—	25	—	25	ns	15
$\overline{SE}$ access time	t_{SEA}	—	20	—	22	—	25	—	25	ns	15
Serial data-out hold time	t_{SOH}	5	—	5	—	5	—	5	—	ns	
Serial write enable setup time	t_{SWS}	5	—	5	—	5	—	5	—	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	15	—	15	—	15	—	ns	

Split Read Transfer Cycle, Split Write Transfer Cycle

		HM534253B									
		-6		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Split transfer setup time	t_{STS}	20	—	20	—	20	—	25	—	ns	
Split transfer hold time referenced to $\overline{RAS}$	t_{RST}	60	—	70	—	80	—	100	—	ns	
Split transfer hold time referenced to $\overline{CAS}$	t_{CST}	20	—	20	—	20	—	25	—	ns	
Split transfer hold time referenced to column address	t_{AST}	35	—	35	—	40	—	45	—	ns	
SC to QSF delay time	t_{SQD}	—	30	—	30	—	30	—	30	ns	15
QSF hold time referenced to SC	t_{SQH}	5	—	5	—	5	—	5	—	ns	
Serial clock cycle time	t_{SCC}	25	—	25	—	30	—	30	—	ns	
SC pulse width	t_{SC}	5	—	5	—	10	—	10	—	ns	
SC precharge time	t_{SCP}	10	—	10	—	10	—	10	—	ns	
SC access time	t_{SCA}	—	20	—	22	—	25	—	25	ns	15
Serial data-out hold time	t_{SOH}	5	—	5	—	5	—	5	—	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	15	—	15	—	15	—	ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	35	15	40	15	55	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	—	35	—	40	—	45	—	ns	

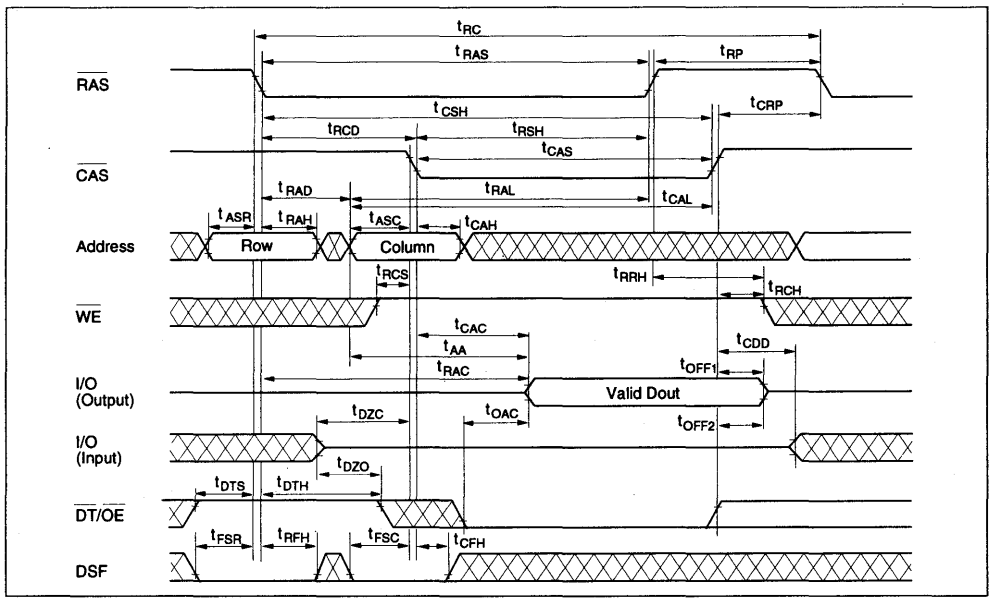
Serial Read Cycle, Serial Write Cycle

		HM534253B									
		-6		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Serial clock cycle time	t_{SCC}	25	—	25	—	30	—	30	—	ns	
SC pulse width	t_{SC}	5	—	5	—	10	—	10	—	ns	
SC precharge width	t_{SCP}	10	—	10	—	10	—	10	—	ns	
Access time from SC	t_{SCA}	—	20	—	22	—	25	—	25	ns	15
Access time from $\overline{SE}$	t_{SEA}	—	20	—	22	—	25	—	25	ns	15
Serial data-out hold time	t_{SOH}	5	—	5	—	5	—	5	—	ns	
Serial output buffer turn-off time referenced to $\overline{SE}$	t_{SEZ}	—	20	—	20	—	20	—	20	ns	5
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	15	—	15	—	15	—	ns	
Serial write enable setup time	t_{SWS}	5	—	5	—	5	—	5	—	ns	
Serial wrtie enbable hold time	t_{SWH}	15	—	15	—	15	—	15	—	ns	
Serial write disable setup time	t_{SWIS}	5	—	5	—	5	—	5	—	ns	
Serial write disable hold time	t_{SWIH}	15	—	15	—	15	—	15	—	ns	

Notes:
1. AC measurements assume t_T = 5 ns.
2. When $t_{RCD} > t_{RCD}$ (max) and $t_{RAD} > t_{RAD}$ (max), access time is specified by t_{CAC} or t_{AA}.
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition time t_T is measured between V_{IH} and V_{IL}.
4. Data input must be floating before output buffer is turned on. In read cycle, read-modify-write cycle and delayed write cycle, either t_{DZC} (min) or t_{DZO} (min) must be satisfied.
5. t_{OFF1} (max), t_{OFF2} (max), and t_{SEZ} (max) are defined as the time at which the output acheives the open circuit condition (V_{OH} – 100 mV, V_{OL} + 100 mV).
6. Assume that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
7. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
8. When $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max), access time is specified by t_{CAC}.
9. When $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max), access time is specified by t_{AA}.
10. If either t_{RCH} or t_{RRH} is satisfied, operation is guaranteed.
11. When $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle, and I/O pins remain in an open circuit (high impedance) condition.
12. These parameters are specified by the later falling edge of $\overline{CAS}$ or $\overline{WE}$.
13. Either t_{CDD} (min) or t_{ODD} (min) must be satisfied because output buffer must be turned off by $\overline{CAS}$ or $\overline{OE}$ prior to applying data to the device when output buffer is on.
14. When $t_{AWD} \geq t_{AWD}$ (min) and $t_{CWD} \geq t_{CWD}$ (min) in read-modify-write cycle, the data of the selected address outputs to an I/O pin and input data is written into the selected address. t_{ODD} (min) must be satisfied because output buffer must be turned off by $\overline{OE}$ prior to applying data to the device.
15. Measured with a load circuit equivalent to 2 TTL loads and 50 pF.
16. After power-up, pause for 100 µs or more and execute at least 8 initialization cycle (normal memory cycle or refresh cycle), then start operation.
17. When the serial write cycle is used, at least one SC pulse is requied before proper SAM operation after V_{CC} stabilized.
18. t_{DTHH} (min) must be satisfied only if $\overline{DT/OE}$ rises up before $\overline{RAS}$ rises in a read transfer cycle.

Timing Waveforms*19

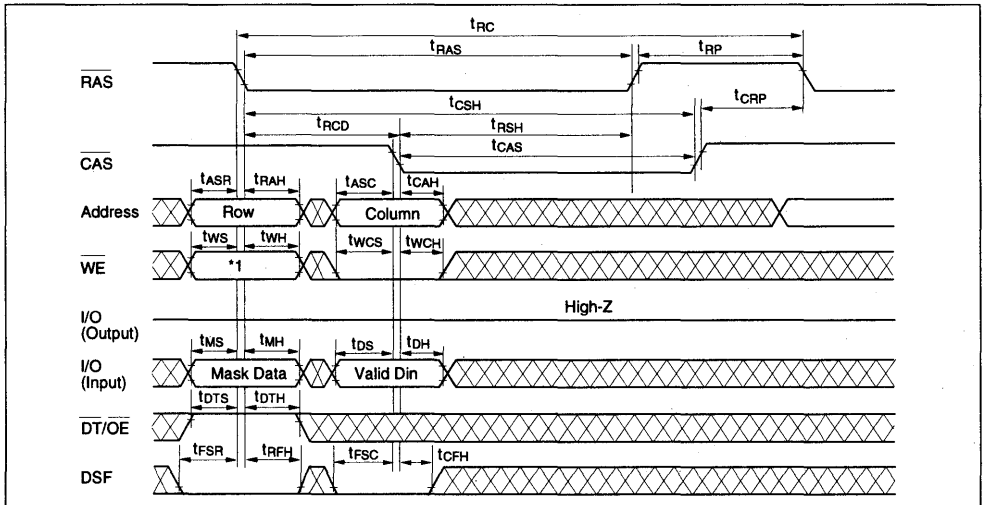
Read Cycle



Note19: H or L (H: V_{IH} (min) ≤ V_{IN} ≤ V_{IH} (max), L: V_{IL} (min) ≤ V_{IN} ≤ V_{IL} (max))

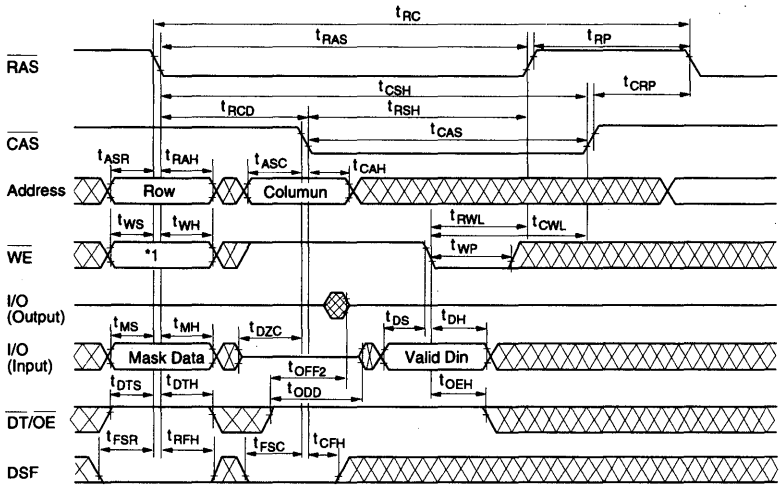
Invalid Dout

Early Write Cycle



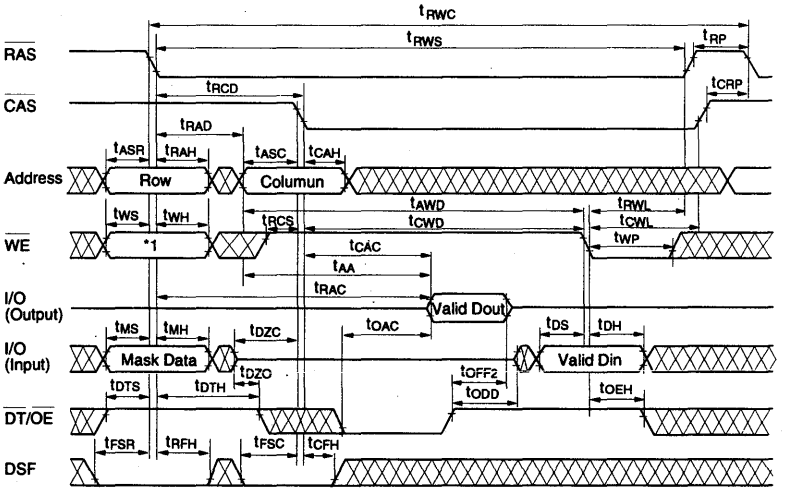
Note: 1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

Delayed Write Cycle



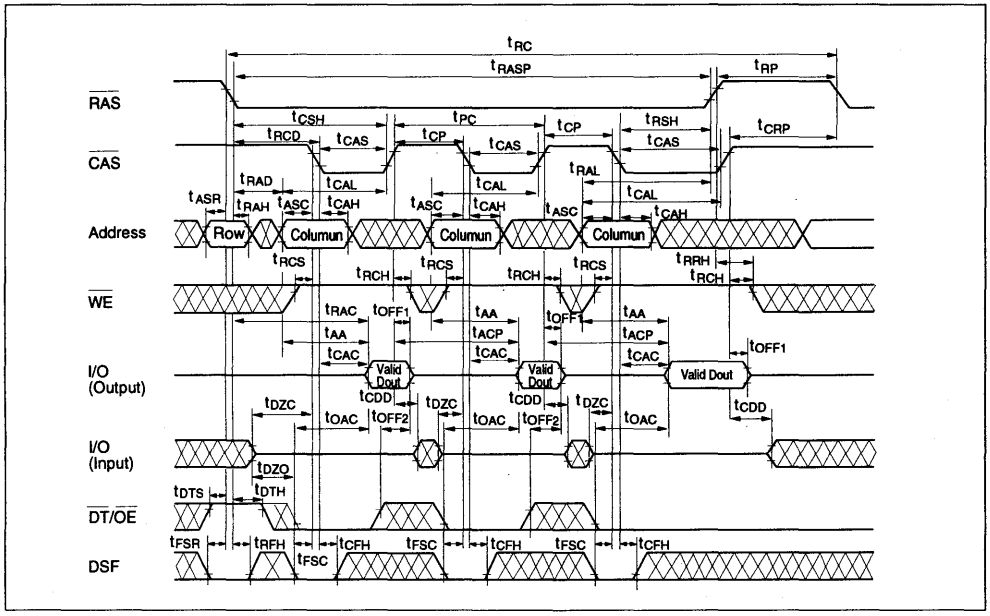
Note: 1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

Read-Modify-Write Cycle

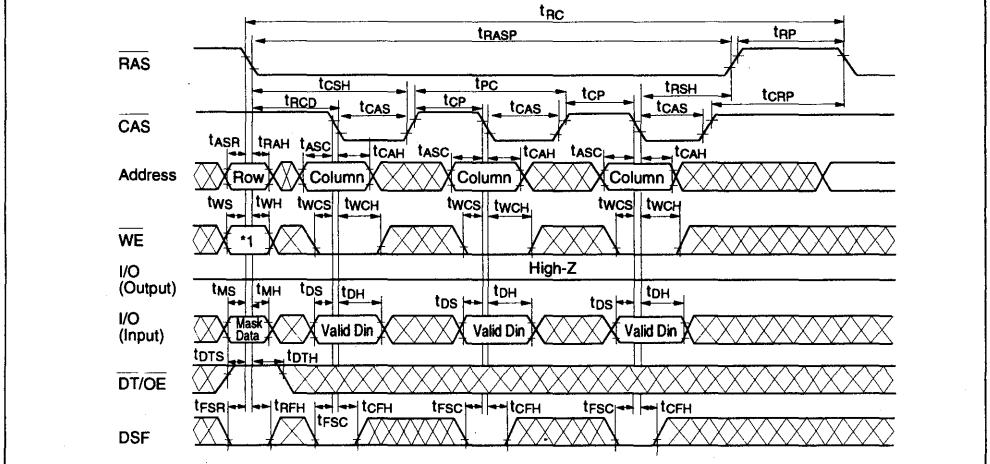


Note: 1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

Page Mode Read Cycle

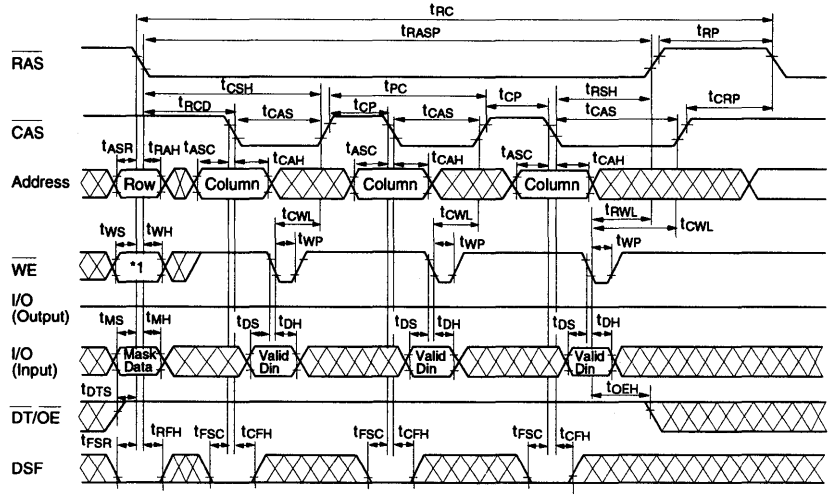


Page Mode Write Cycle (Early Write)



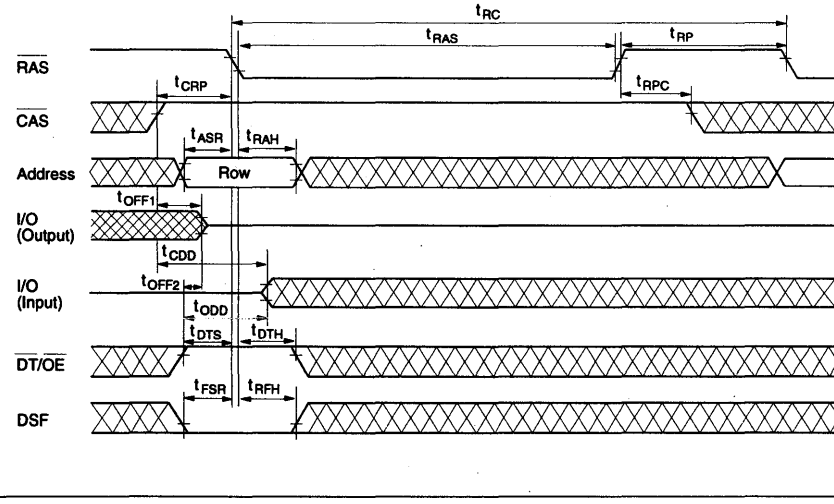
Note: 1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

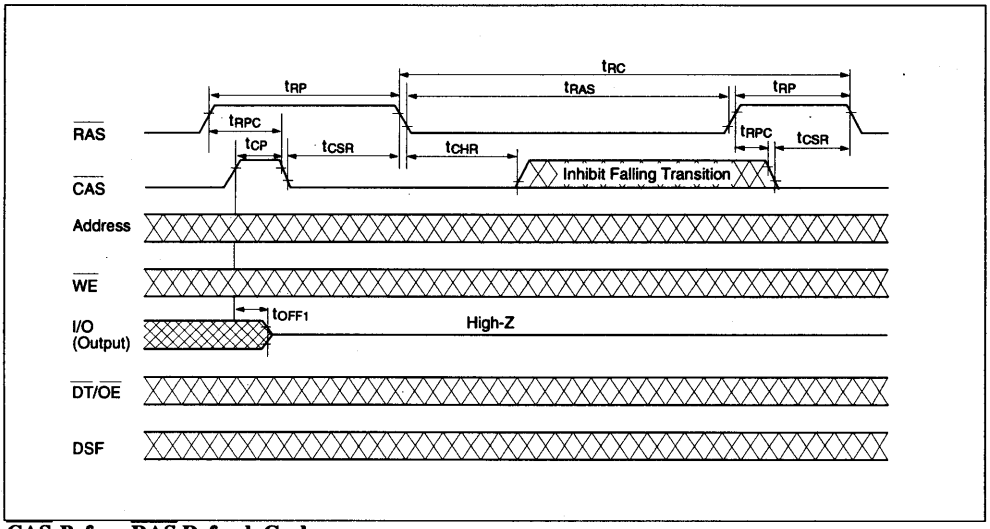
Page Mode Write Cycle (Delayed Write)



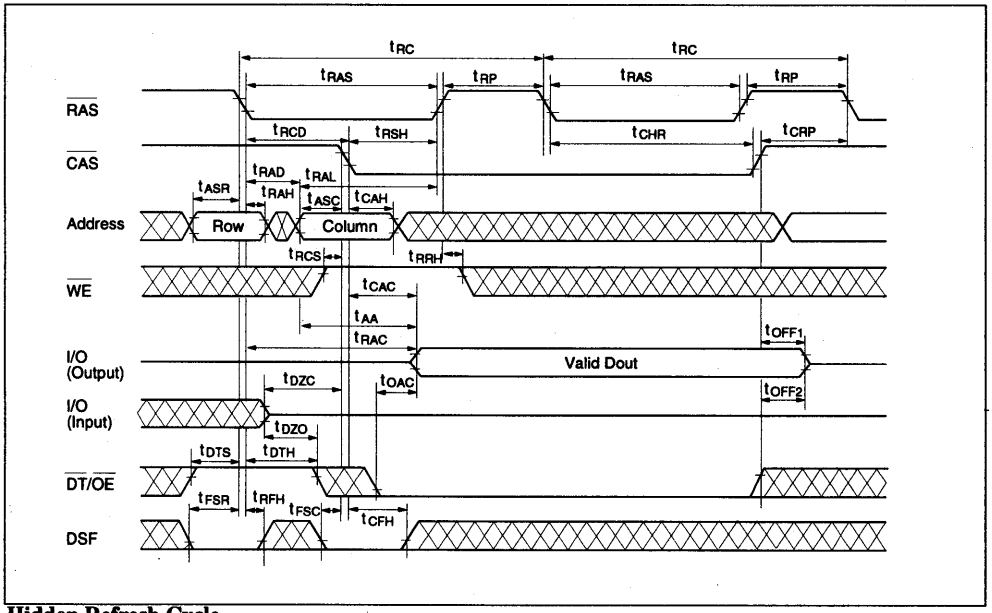
Note: 1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

$\overline{RAS}$-Only Refresh Cycle

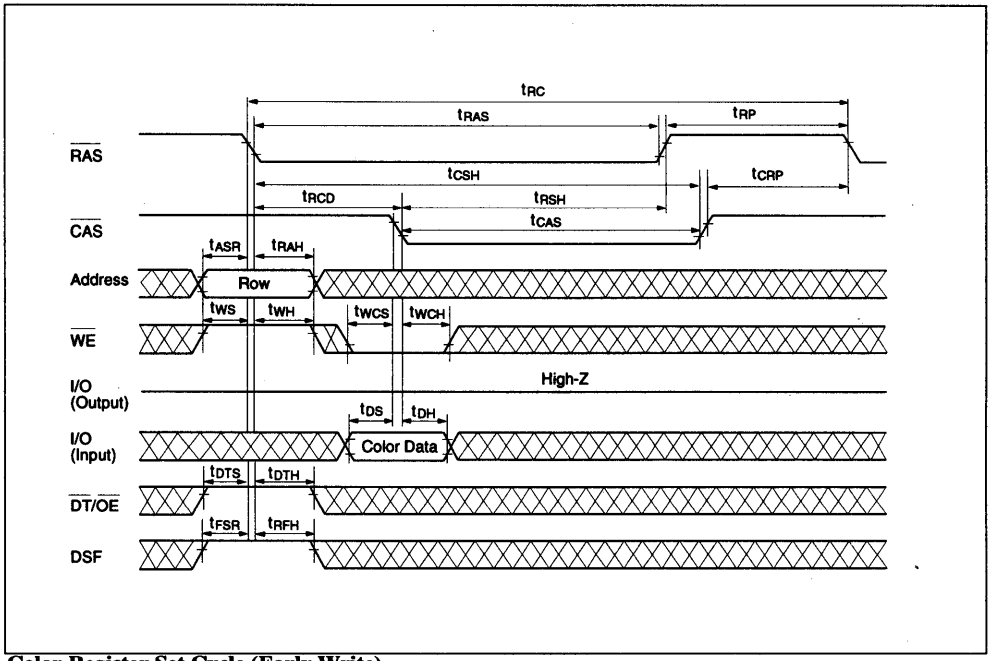




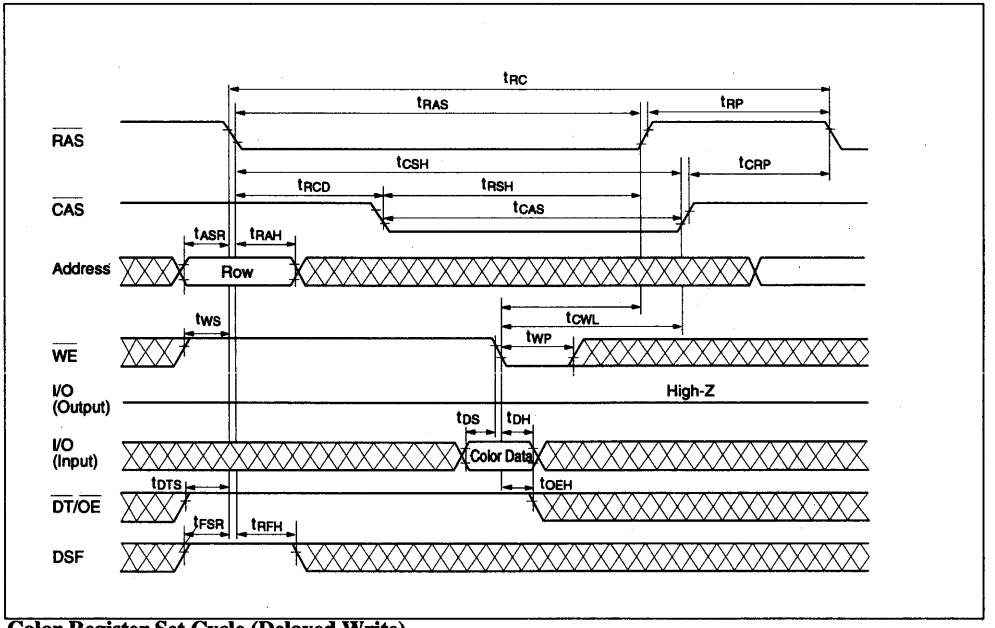
CAS-Before-RAS Refresh Cycle



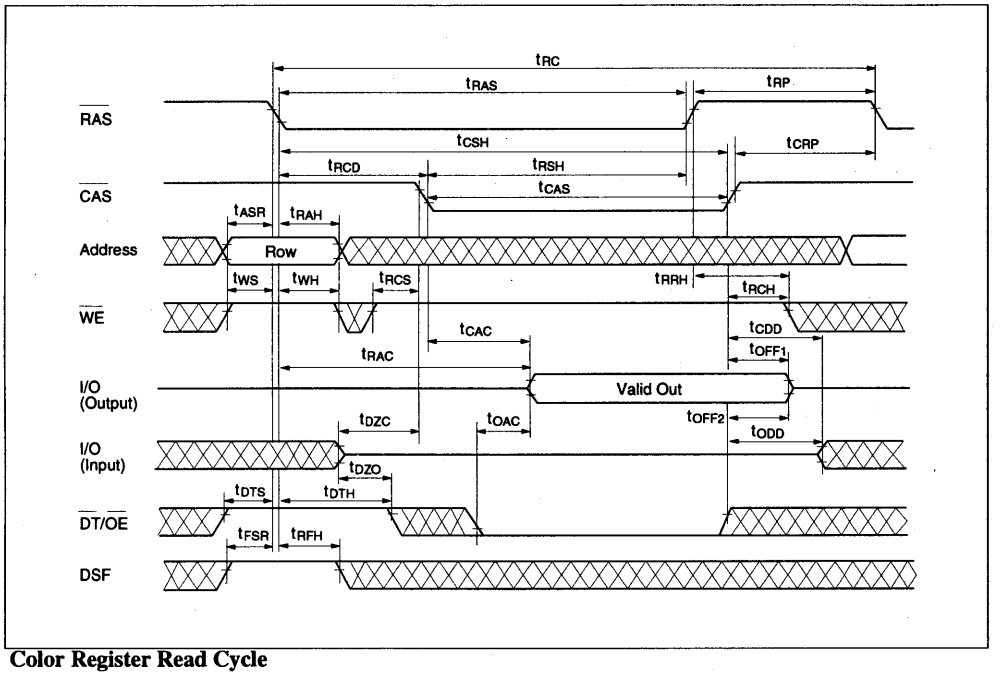
Hidden Refresh Cycle



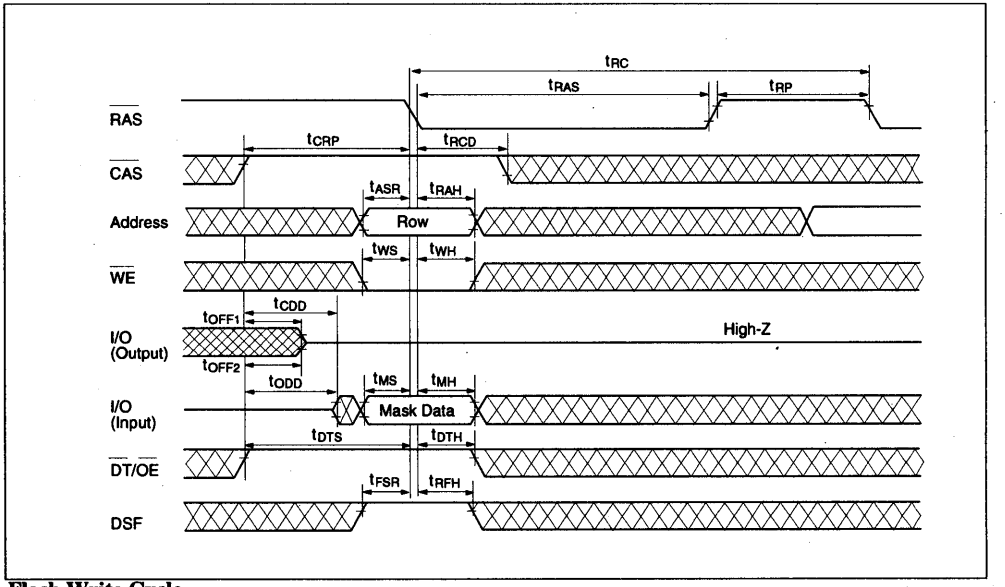
Color Register Set Cycle (Early Write)



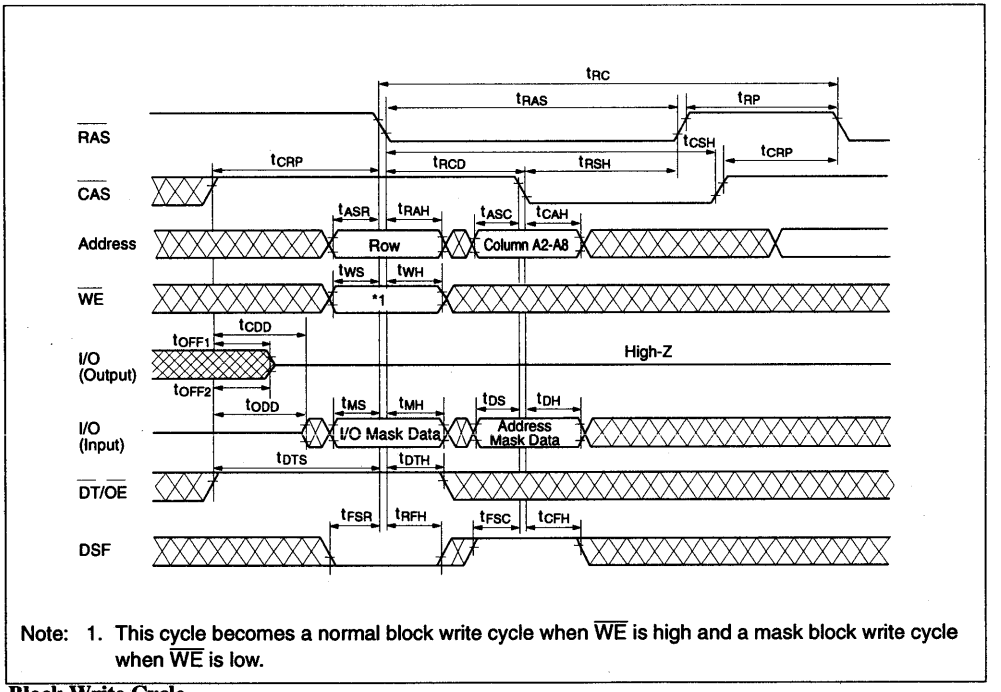
Color Register Set Cycle (Delayed Write)



Color Register Read Cycle

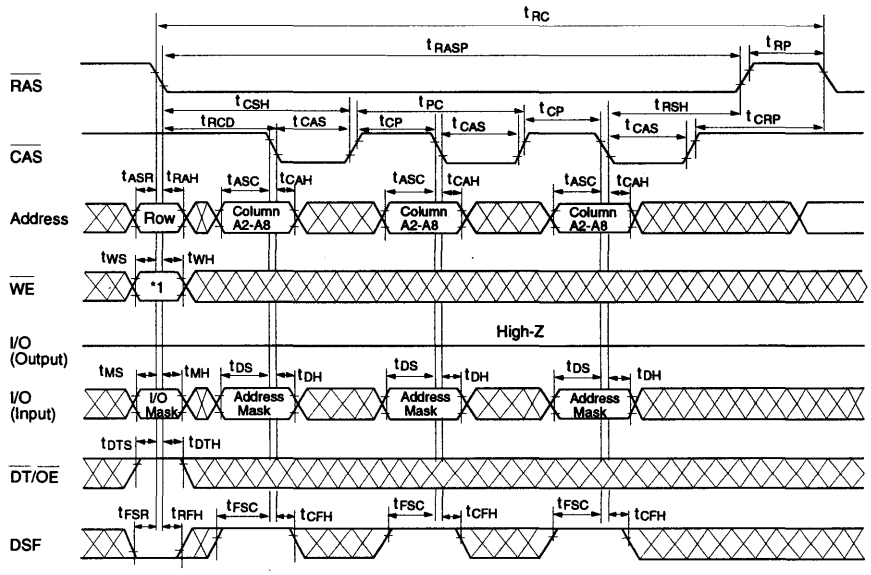


Flash Write Cycle



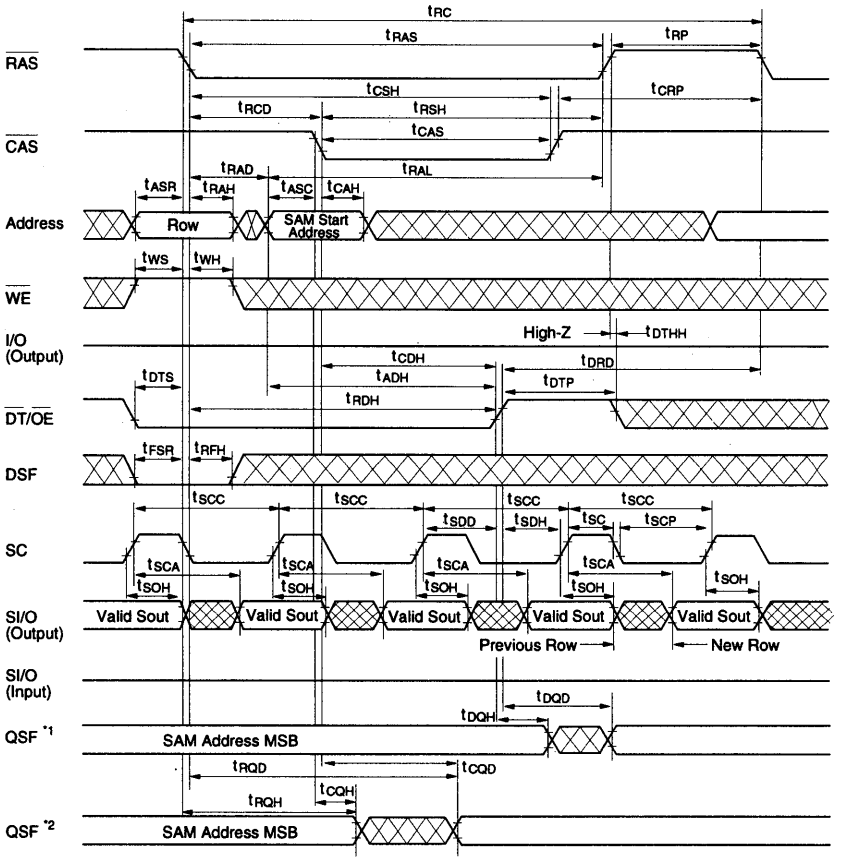
Note: 1. This cycle becomes a normal block write cycle when $\overline{WE}$ is high and a mask block write cycle when $\overline{WE}$ is low.

Block Write Cycle



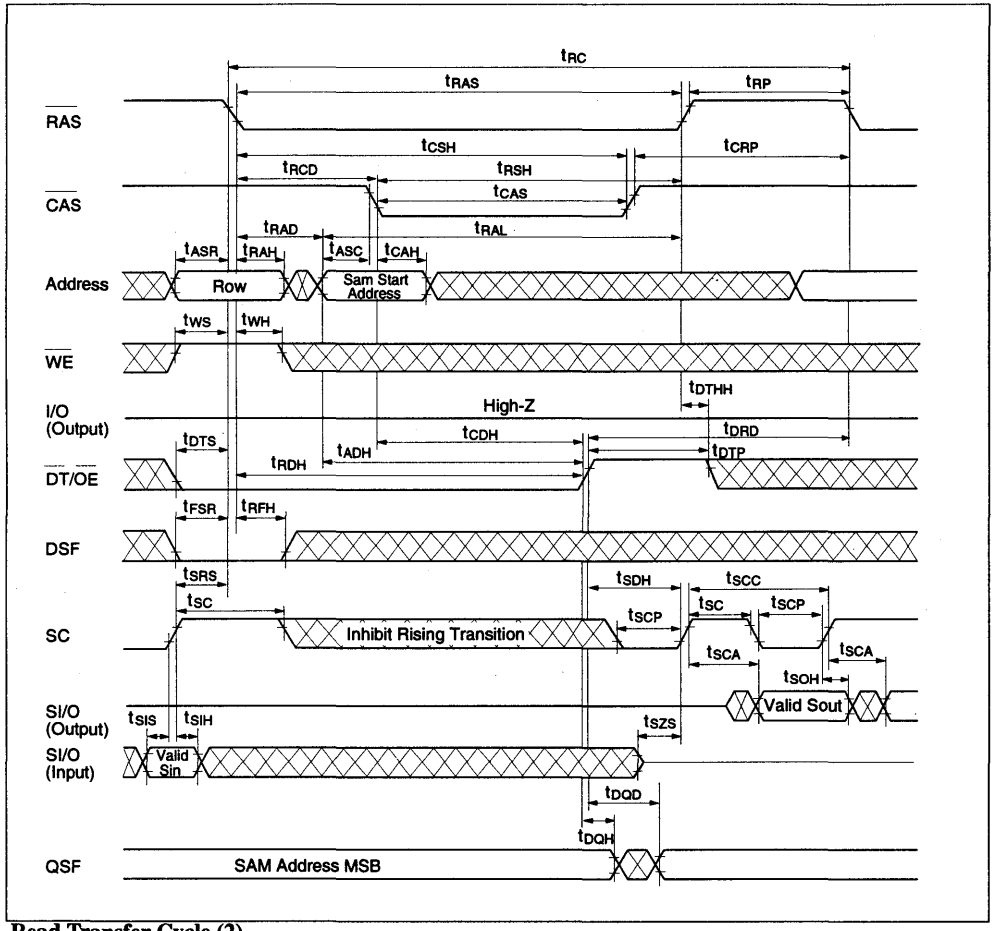
Note: 1. This cycle becomes a normal block write cycle when $\overline{WE}$ is high and a mask block write cycle when $\overline{WE}$ is low.

Page Mode Block Write Cycle

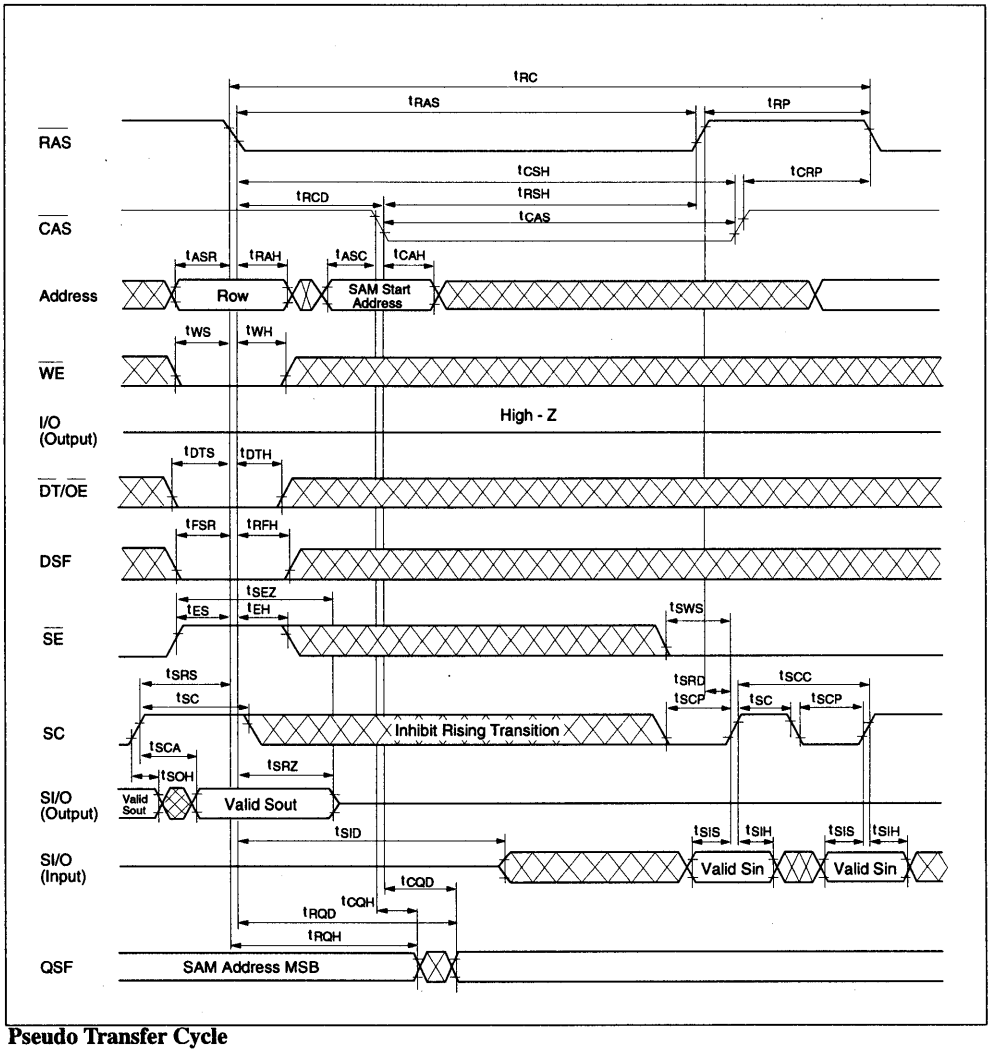


Note: 1. This QSF timing is referred when SC is risen once or more between the previous transfer cycle and $\overline{CAS}$ falling edge of this cycle (QSF is switched by $\overline{DT}$ rising).
2. This QSF timing is referred when SC isn't risen between the previous transfer cycle and $\overline{CAS}$ falling edge of this cycle (QSF is switched by $\overline{RAS}$ or $\overline{CAS}$ falling).

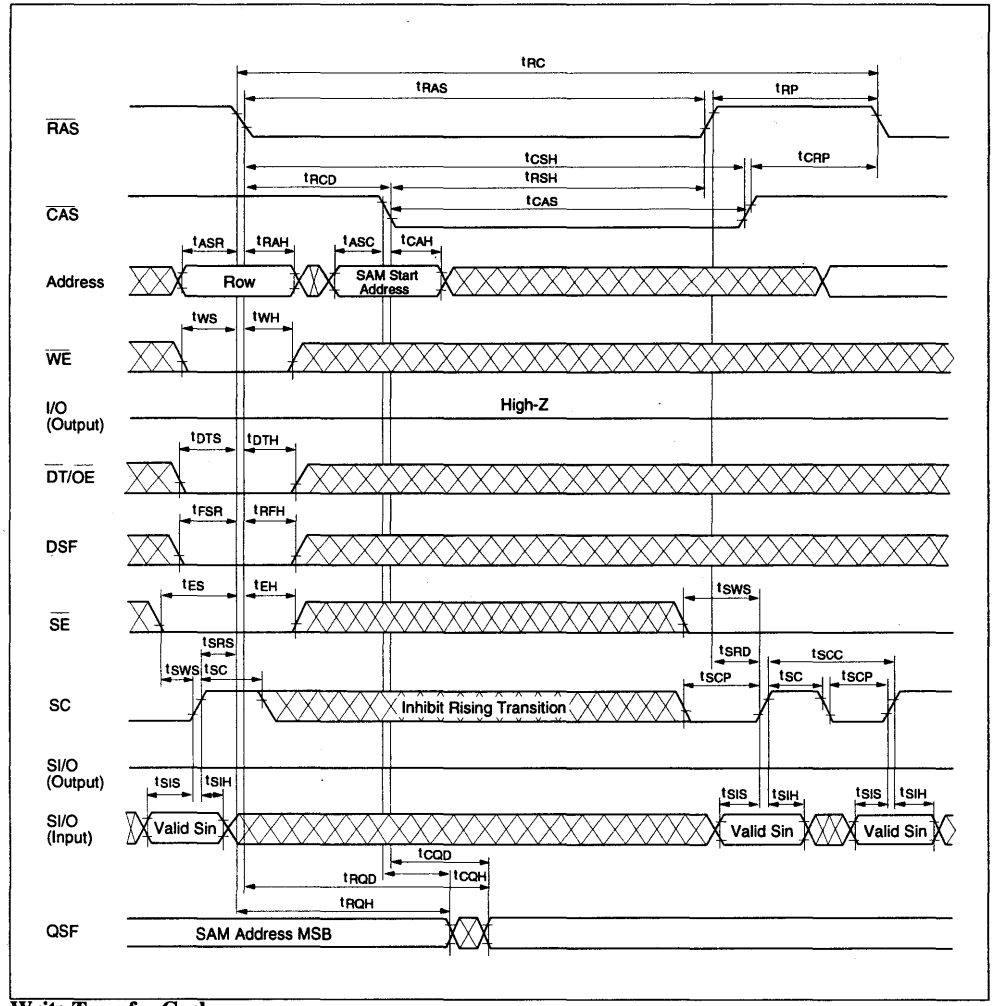
Read Transfer Cycle (1)



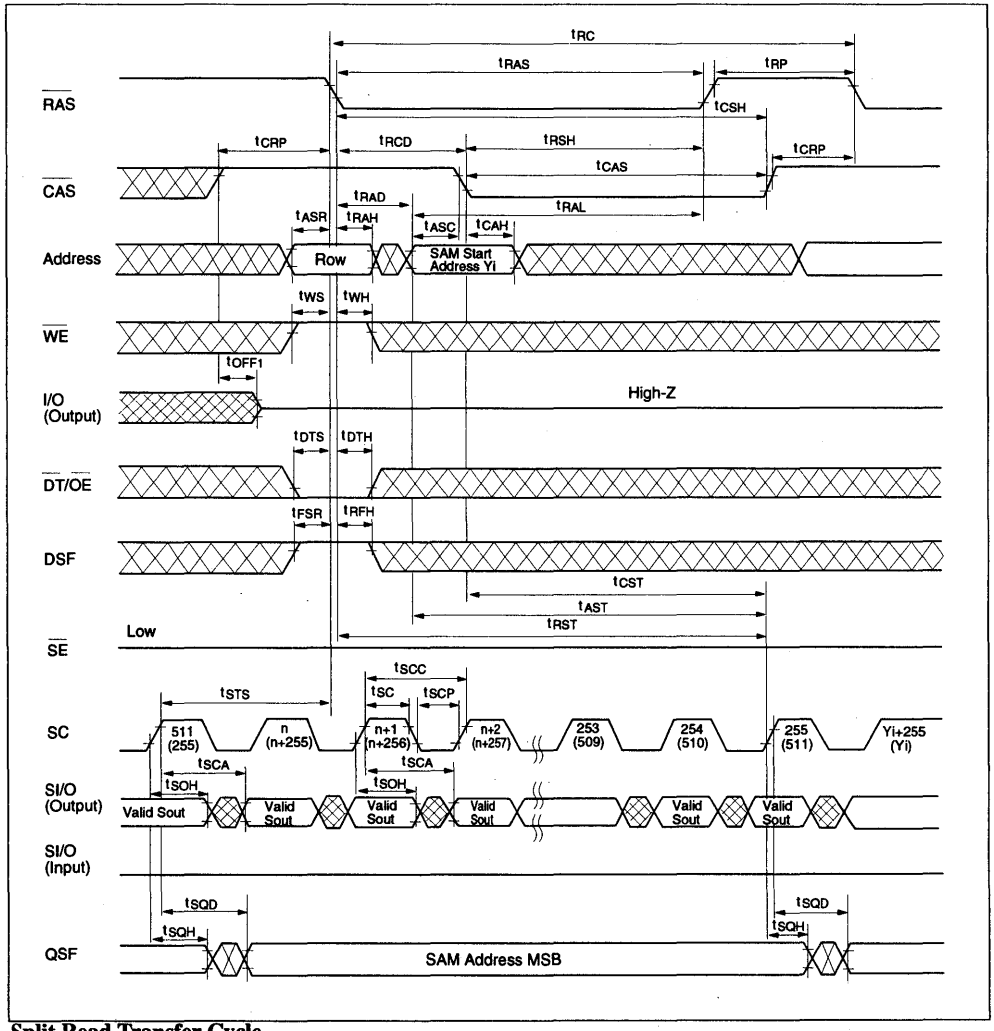
Read Transfer Cycle (2)



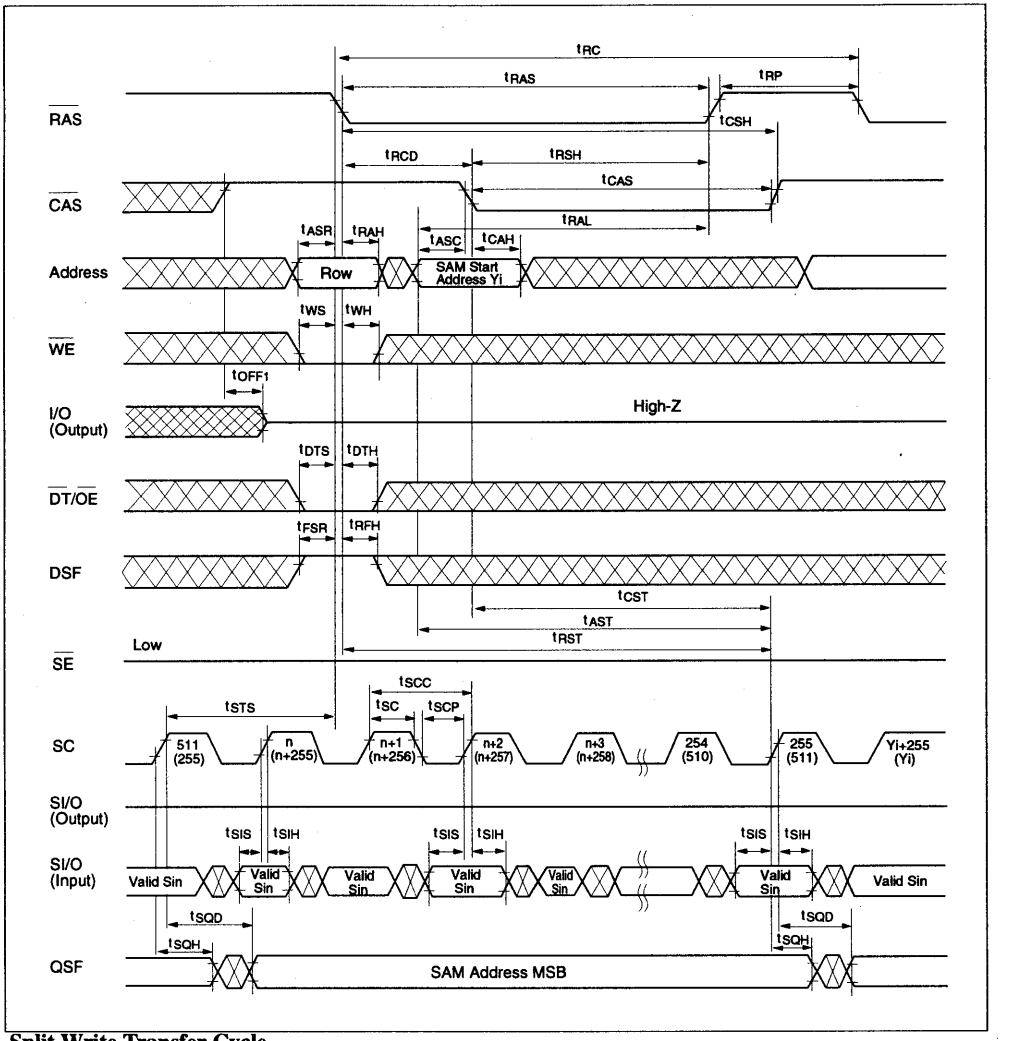
Pseudo Transfer Cycle



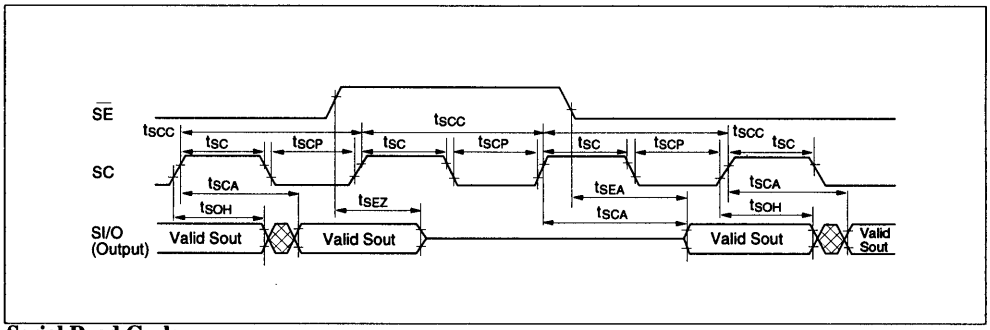
Write Transfer Cycle



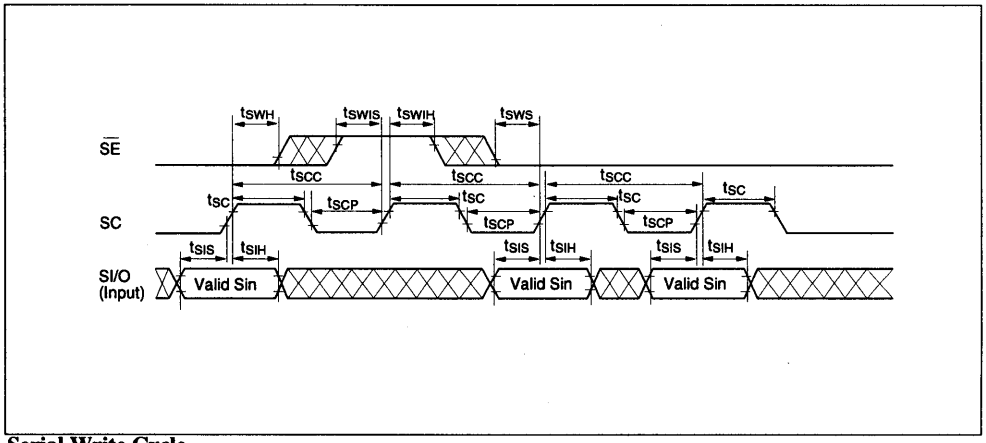
Split Read Transfer Cycle



Split Write Transfer Cycle



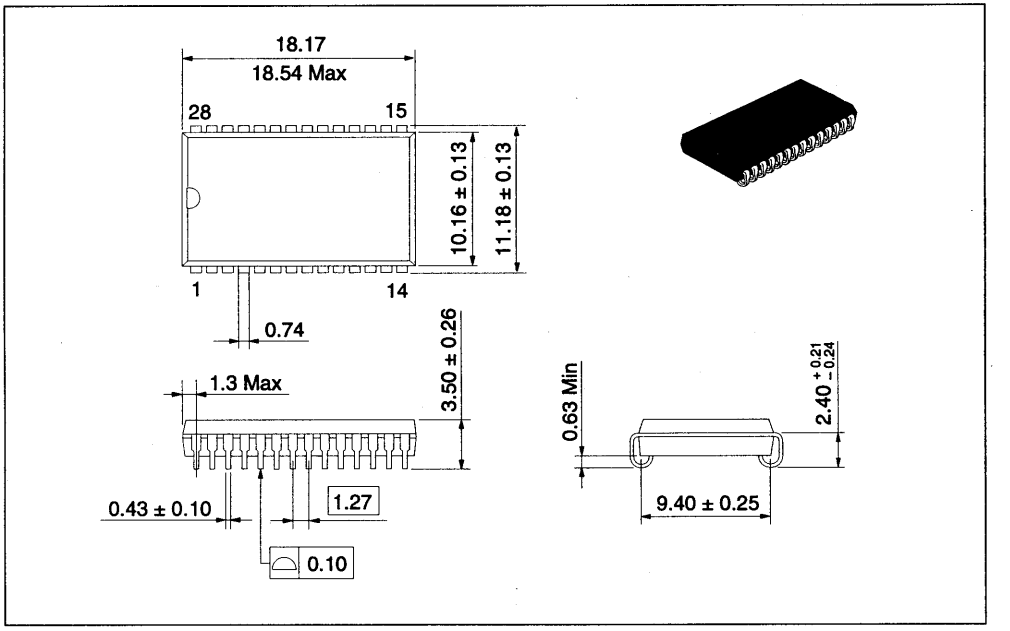
Serial Read Cycle



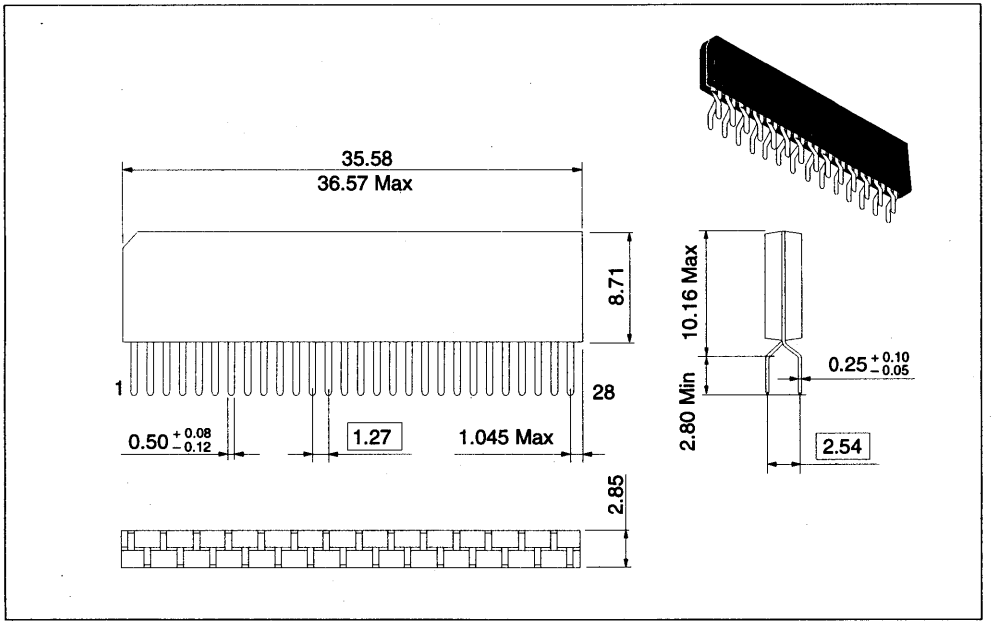
Serial Write Cycle

Package Dimensions

HM534253BJ Series (CP-28D) **Unit: mm**

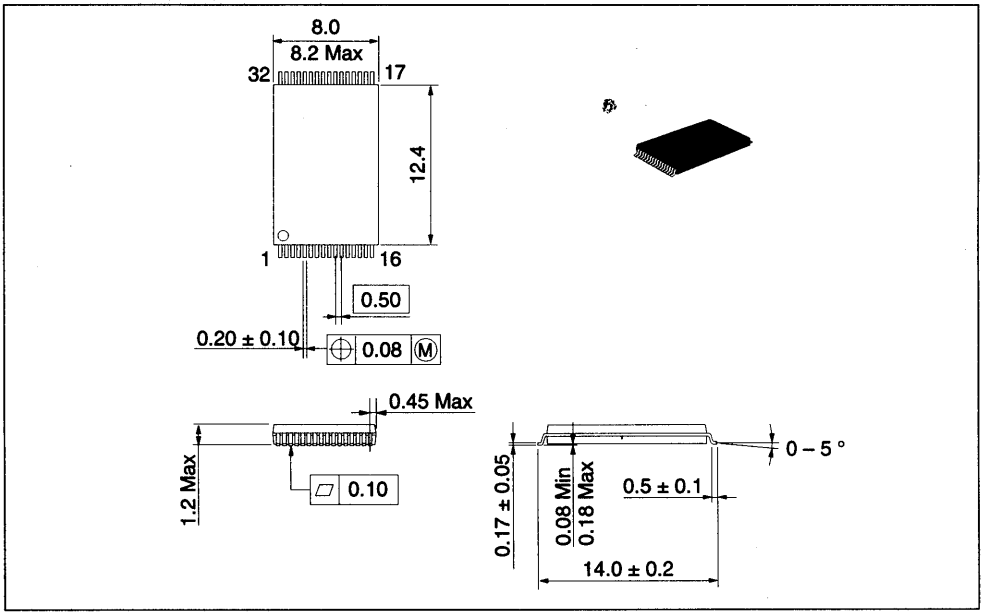


HM534253BZ Series (ZP-28) **Unit: mm**

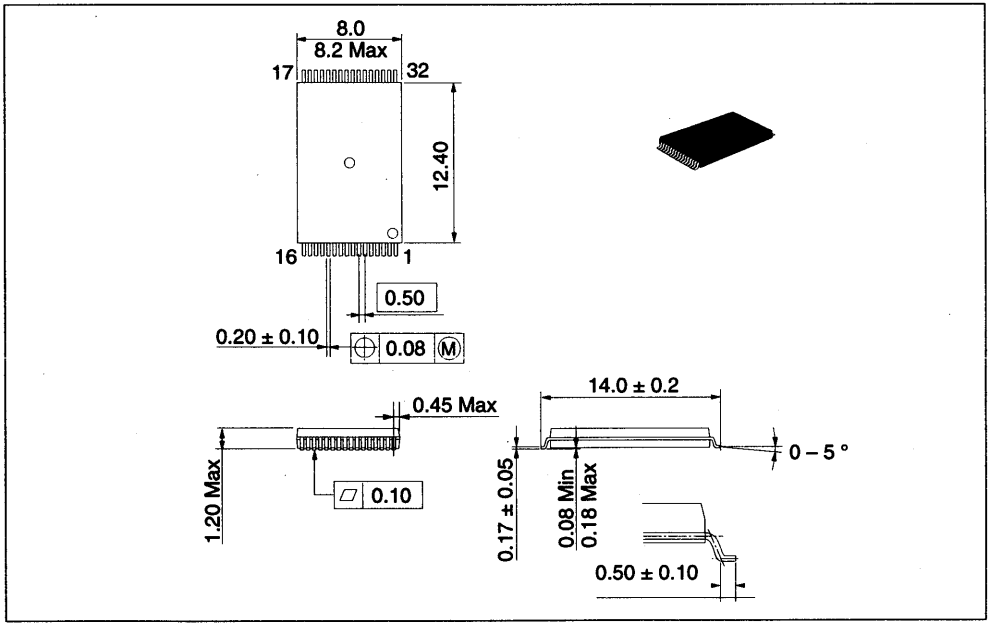


Package Dimensions (cont)

HM534253BT Series (TFP-32DA) **Unit: mm**



HM534253BR Series (TFP-32DAR) **Unit: mm**



HM538123B Series

131072-word x 8-bit Multiport CMOS Video RAM

HITACHI

Rev. 1
Mar. 18, 1994

The HM538123B is a 1-Mbit multiport video RAM equipped with a 128-kword x 8-bit dynamic RAM and a 256-word x 8-bit SAM (serial access memory). Its RAM and SAM operate independently and asynchronously. It can transfer data between RAM and SAM. In addition, it has two modes to realize fast writing in RAM. Block write and flash write modes clear the data of 4-word x 8-bit and the data of one row (256-word x 8-bit) respectively in one cycle of RAM. And the HM538123B makes split transfer cycle possible by dividing SAM into two split buffers equipped with 128-word x 8-bit each. This cycle can transfer data to SAM which is not active, and enables a continuous serial access.

Features

- Multiport organization
  - Asynchronous and simultaneous operation of RAM and SAM capability
    - RAM : 128 kword x 8 bit and
    - SAM : 256 word x 8 bit
- Access time
  - RAM : 60 ns/70 ns/80 ns/100 ns max
  - SAM : 20 ns/22 ns/25 ns/25 ns max
- Cycle time
  - RAM : 125 ns/135 ns/150 ns/180 ns min
  - SAM : 25 ns/25 ns/30 ns/30 ns min
- Low power
  - Active RAM : 413 mW max
  - SAM : 275 mW max
  - Standby 38.5 mW max
- High-speed page mode capability
- Mask write mode capability
- Bidirectional data transfer cycle between RAM and SAM capability
- Split transfer cycle capability
- Block write mode capability
- Flash write mode capability
- 3 variations of refresh (8 ms/512 cycles)
  - $\overline{\text{RAS}}$-only refresh
  - $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - Hidden refresh
- TTL compatible

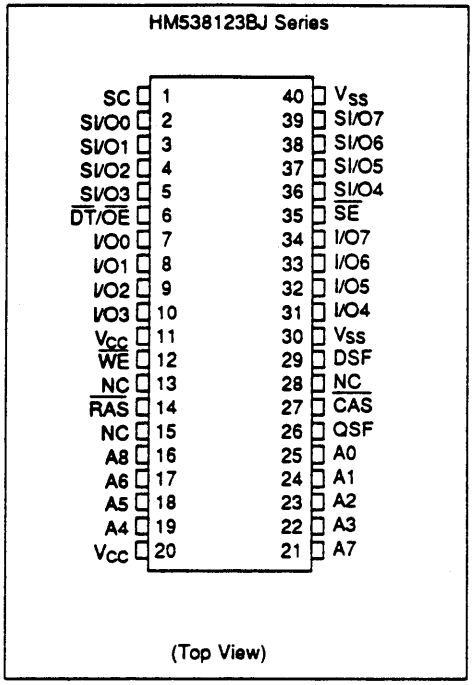
Ordering Information

Type No.	Access time	Package
HM538123BJ-6	60 ns	400-mil
HM538123BJ-7	70 ns	40-pin
HM538123BJ-8	80 ns	plastic SOJ
HM538123BJ-10	100 ns	(CP-40D)

Hitachi semiconductor

ADE-203-231A (Z)

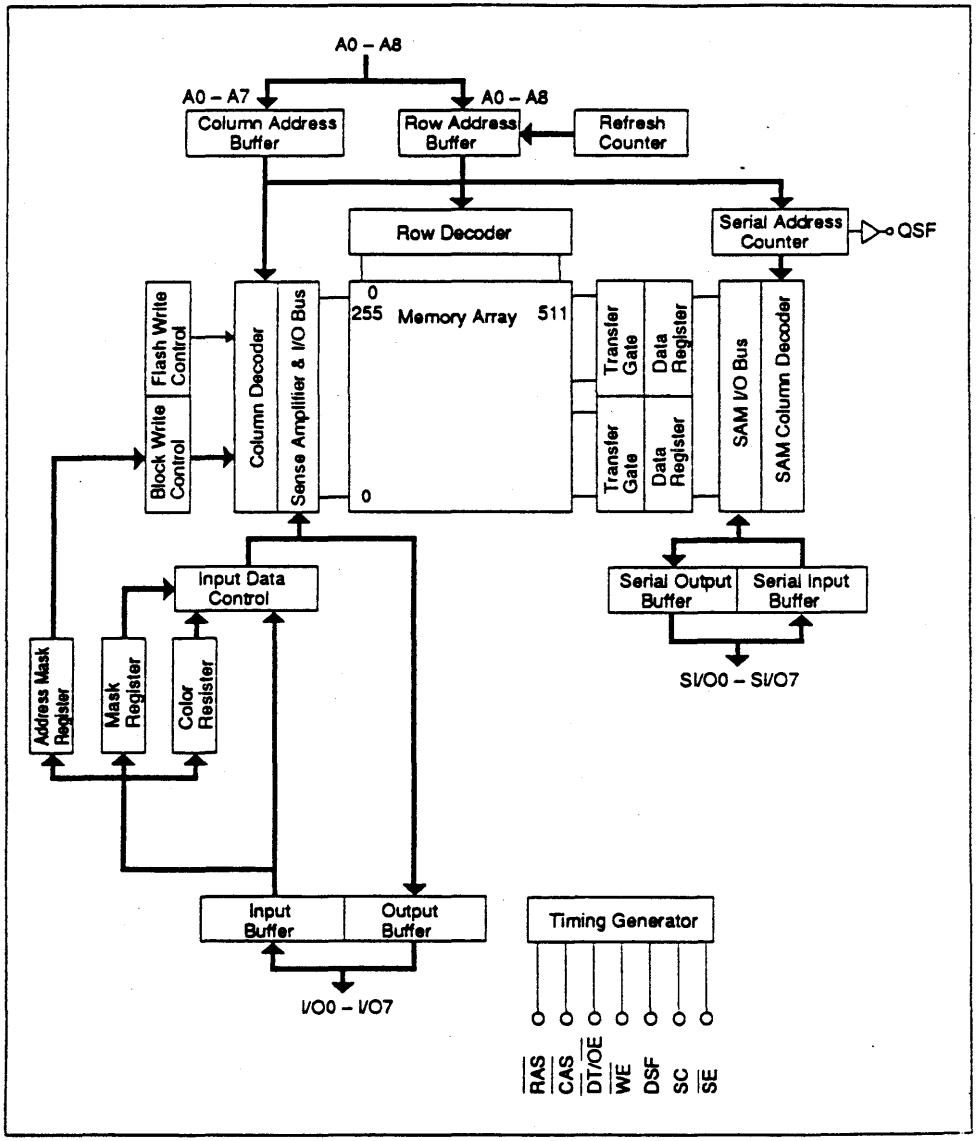
Pin Arrangement



Pin Description

Pin name	Function
A0-A8	Address inputs
I/O0-I/O7	RAM port data inputs/outputs
SI/O0-SI/O7	SAM port data inputs/outputs
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
$\overline{DT/OE}$	Data transfer/Output enable
SC	Serial clock
$\overline{SE}$	SAM port enable
DSF	Special function input flag
QSF	Special function output flag
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection

Block Diagram



Pin Functions

$\overline{RAS}$ (input pin): $\overline{RAS}$ is a basic RAM signal. It is active in low level and standby in high level. Row address and signals as shown in table 1 are input at the falling edge of $\overline{RAS}$. The input level of these signals determine the operation cycle of the HM538123B.

Table 1 Operation Cycles of the HM538123B

Input Level at the falling edge of $\overline{RAS}$						
$\overline{CAS}$	$\overline{DT}$/$\overline{OE}$	$\overline{WE}$	$\overline{SE}$	DSF	DSF at the falling edge of $\overline{CAS}$	Operation Mode
L	X	X	X	X	—	CBR refresh
H	L	L	L	L	X	Write transfer
H	L	L	H	L	X	Pseudo transfer
H	L	L	X	H	X	Split write transfer
H	L	H	X	L	X	Read transfer
H	L	H	X	H	X	Split read transfer
H	H	L	X	L	L	Read/mask write
H	H	L	X	L	H	Mask block write
H	H	L	X	H	X	Flash write
H	H	H	X	L	L	Read/write
H	H	H	X	L	H	Block write
H	H	H	X	H	X	Color register read/write

Note: X; Don't care.

$\overline{CAS}$ (input pin): Column address and DSF signal are fetched into chip at the falling edge of $\overline{CAS}$, which determines the operation mode of HM538123B. $\overline{CAS}$ controls output impedance of I/O in RAM.

A0-A8 (input pins): Row address (AX0-AX8) is determined by A0-A8 level at the falling edge of $\overline{RAS}$. Column address (AY0-AY7) is determined by A0-A7 level at the falling edge of $\overline{CAS}$. In transfer cycles, row address is the address on the word line which transfers data with SAM data register, and column address is the SAM start address after transfer.

$\overline{WE}$ (input pin): $\overline{WE}$ pin has two functions at the falling edge of $\overline{RAS}$ and after. When $\overline{WE}$ is low at the falling edge of $\overline{RAS}$, the HM538123B turns to mask write mode. According to the I/O level at the time, write on each I/O can be masked. ($\overline{WE}$ level at the falling edge of $\overline{RAS}$ is don't care in read cycle.) When $\overline{WE}$ is high at the falling edge of $\overline{RAS}$, a normal write cycle is executed. After that, $\overline{WE}$ switches read/write cycles as in a standard DRAM. In a transfer cycle, the direction of transfer is determined by $\overline{WE}$ level at the falling edge of $\overline{RAS}$. When $\overline{WE}$ is low, data is transferred from SAM to RAM (data is written into RAM), and when $\overline{WE}$ is high, data is transferred from RAM to SAM (data is read from RAM).

I/O0-I/O7 (input/output pins): I/O pins function as mask data at the falling edge of $\overline{RAS}$ (in mask write mode). Data is written only to high I/O pins. Data on low I/O pins are masked and internal data are retained. After that, they function as input/output pins as those of a standard DRAM. In block write cycle, they function as address mask data at the falling edge of $\overline{CAS}$.

$\overline{DT}/\overline{OE}$ (input pin): $\overline{DT}/\overline{OE}$ pin functions as $\overline{DT}$ (data transfer) pin at the falling edge of $\overline{RAS}$ and as $\overline{OE}$ (output enable) pin after that. When $\overline{DT}$ is low at the falling edge of $\overline{RAS}$, this cycle becomes a transfer cycle. When $\overline{DT}$ is high at the falling edge of $\overline{RAS}$, RAM and SAM operate independently.

SC (input pin): SC is a basic SAM clock. In a serial read cycle, data outputs from an SI/O pin synchronously with the rising edge of SC. In a serial write cycle, data on an SI/O pin at the rising edge of SC is fetched into the SAM data register.

$\overline{SE}$ (input pin): $\overline{SE}$ pin activates SAM. When $\overline{SE}$ is high, SI/O is in the high impedance state in serial read cycle and data on SI/O is not fetched into the SAM data register in serial write cycle. $\overline{SE}$ can be used as a mask for serial write because internal pointer is incremented at the rising edge of SC.

SI/O0-SI/O7 (input/output pins): SI/Os are input/output pins in SAM. Direction of input/output is determined by the previous transfer cycle. When it was a read transfer cycle, SI/O outputs data. When it was a pseudo transfer cycle or write transfer cycle, SI/O inputs data.

DSF (input pin): DSF is a special function data input flag pin. It is set to high at the falling edge of $\overline{RAS}$ when new functions such as color register read/write, split transfer, and flash write, are used. DSF is set to high at the falling edge of $\overline{CAS}$ when block write is executed.

QSF (output pin): QSF outputs data of address A7 in SAM. QSF is switched from low to high by accessing address 127 in SAM and from high to low by accessing 255 address in SAM.

Operation of HM538123B

RAM Read Cycle ($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high and DSF low at the falling edge of $\overline{RAS}$, DSF low at the falling edge of $\overline{CAS}$)

Row address is entered at the $\overline{RAS}$ falling edge and column address at the $\overline{CAS}$ falling edge to the device as in standard DRAM. Then, when $\overline{WE}$ is high and $\overline{DT}/\overline{OE}$ is low while $\overline{CAS}$ is low, the selected address data outputs through I/O pin. At the falling edge of $\overline{RAS}$, $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ become high to distinguish RAM read cycle from transfer cycle and CBR refresh cycle. Address access time (t_{AA}) and $\overline{RAS}$ to column address delay time (t_{RAD}) specifications are added to enable high-speed page mode.

RAM Write Cycle (Early Write, Delayed Write, Read-Modify-Write)
($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high and DSF low at the falling edge of $\overline{RAS}$, DSF low at the falling edge of $\overline{CAS}$)

- Normal Mode Write Cycle ($\overline{WE}$ high at the falling edge of $\overline{CAS}$)

When $\overline{CAS}$ and $\overline{WE}$ are set low after driving $\overline{RAS}$ low, a write cycle is executed and I/O data is written in the selected addresses. When all 8 I/Os are written, $\overline{WE}$ should be high at the falling edge of $\overline{RAS}$ to distinguish normal mode from mask write mode.

If $\overline{WE}$ is set low before the $\overline{CAS}$ falling edge, this cycle becomes an early write cycle and I/O becomes in high impedance. Data is entered at the $\overline{CAS}$ falling edge.
If $\overline{WE}$ is set low after the $\overline{CAS}$ falling edge, this cycle becomes a delayed write cycle. Data is input at the $\overline{WE}$ falling. I/O does not become high impedance in this cycle, so data should be entered with $\overline{OE}$ in high.
If $\overline{WE}$ is set low after t_{CWD} (min) and t_{AWD} (min) after the $\overline{CAS}$ falling edge, this cycle becomes a read-modify-write cycle and enables read/write at the same address in one cycle. In this cycle also, to avoid I/O contention, data should be input after reading data and driving $\overline{OE}$ high.

- Mask Write Mode ($\overline{WE}$ low at the falling edge of $\overline{RAS}$)

If $\overline{WE}$ is set low at the falling edge of $\overline{RAS}$, the cycle becomes a mask write mode which writes only to selected I/O. Whether or not an I/O is written depends on I/O level (mask data) at the falling edge of $\overline{RAS}$. Then the data is written in high I/O pins and masked in low ones and internal data is retained. This mask data is effective during the $\overline{RAS}$ cycle. So, in high-speed page mode, the mask data is retained during the page access.

High-Speed Page Mode Cycle ($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high and DSF low at the falling edge of $\overline{RAS}$)

High-speed page mode cycle reads/writes the data of the same row address at high speed by toggling $\overline{CAS}$ while $\overline{RAS}$ is low. Its cycle time is one third of the random read/write cycle. In this cycle, read, write, and block write cycles can be mixed. Note that address access time (t_{AA}), $\overline{RAS}$ to column address delay time (t_{RAD}), and access time from $\overline{CAS}$ precharge (t_{ACP}) are added. In one $\overline{RAS}$ cycle, 256-word memory cells of the same row address can be accessed. It is necessary to specify access frequency within t_{RASP} max (100 µs).

Color Register Set/Read Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ high, $\overline{WE}$ high and DSF high at the falling edge of $\overline{RAS}$)

In color register set cycle, color data is set to the internal color register used in flash write cycle or block write cycle. 8 bits of internal color register are provided at each I/O. This register is composed of static circuits, so once it is set, it retains the data until reset. Color register set cycle is just as same as the usual write cycle except that DSF is set high at the falling edge of $\overline{RAS}$, and read, early write and delayed write cycle can be executed. In this cycle, HM538123B refreshs the row address fetched at the falling edge of $\overline{RAS}$.

Flash Write Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ high, $\overline{WE}$ low and DSF high at the falling edge of $\overline{RAS}$)

In a flash write cycle, a row of data (256-word x 8-bit) is cleared to 0 or 1 at each I/O according to the data of color register mentioned before. It is also necessary to mask I/O in this cycle. When $\overline{CAS}$ and $\overline{DT}/\overline{OE}$ is set high, $\overline{WE}$ is low, and DSF is high at the falling edge of $\overline{RAS}$, this cycle starts. Then, the row address to clear is given to row address and mask data is given to I/O. Mask data is as same as that of a RAM write cycle. High I/O is cleared, low I/O is not cleared and the internal data is retained. Cycle time is the same as those of RAM read/write cycles, so all bits can be cleared in 1/256 of the usual cycle time. (See figure 1.)

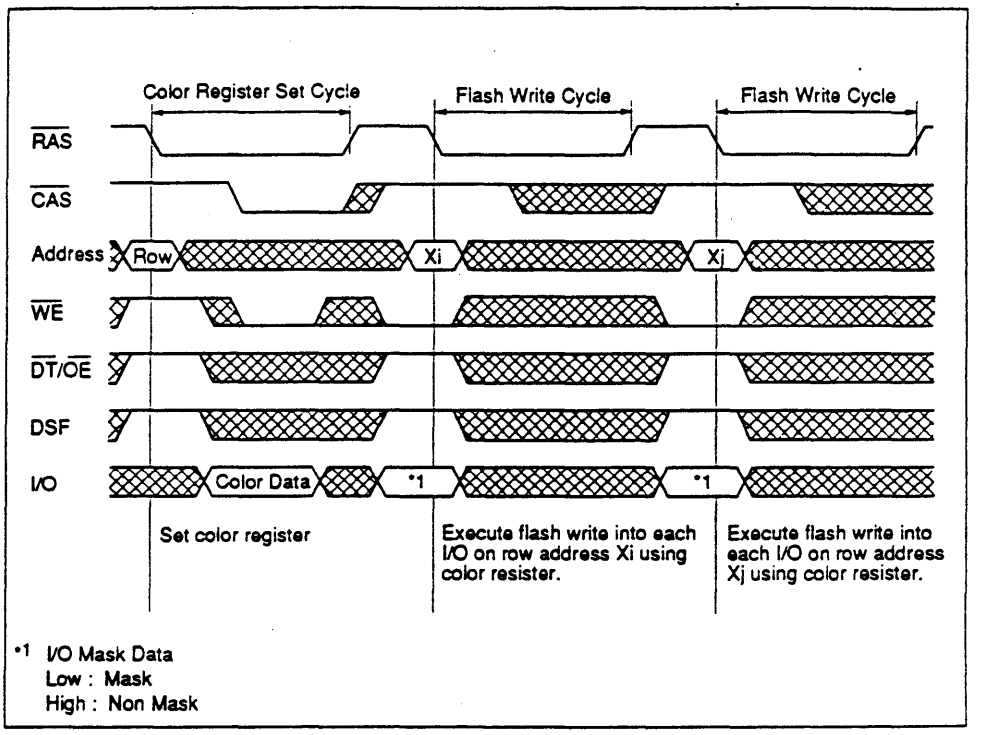


Figure 1 Use of Flash Write

Block Write Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ high and DSF low at the falling edge of $\overline{RAS}$, DSF high at the falling edge of $\overline{CAS}$)

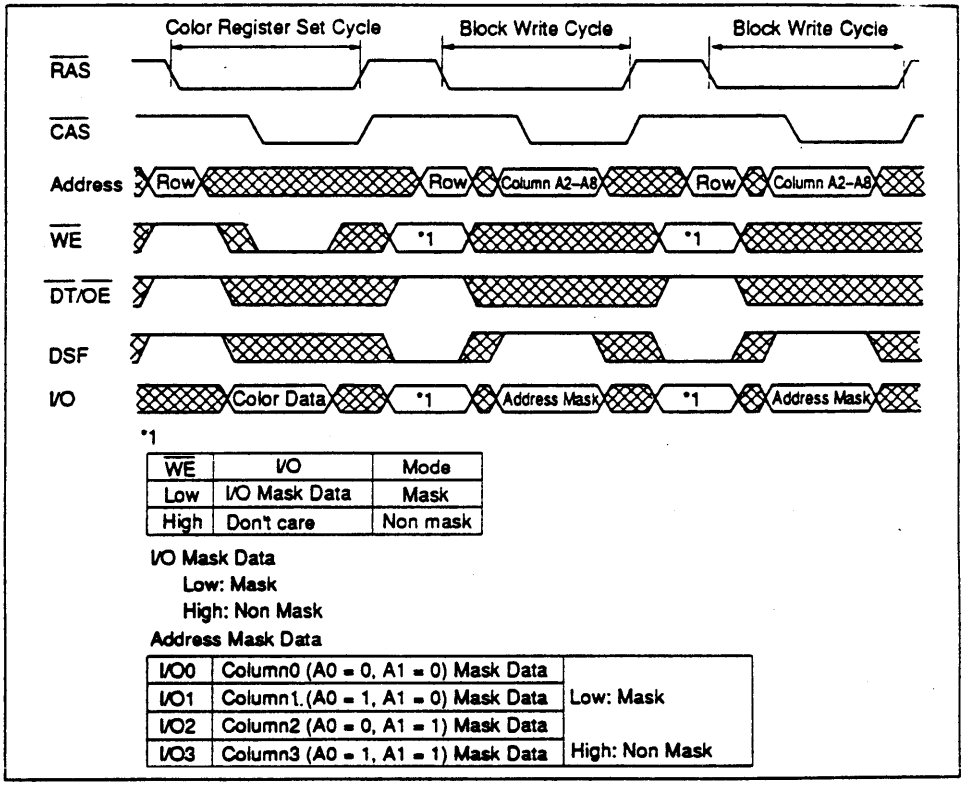
In a block write cycle, 4 columns of data (4-word x 8-bit) is cleared to 0 or 1 at each I/O according to the data of color register. Column addresses A0 and A1 are disregarded. The data on I/Os and addresses can be masked. I/O level at the falling edge of $\overline{CAS}$ determines the address to be cleared. (See figure 2.)

- Normal Mode Block Write Cycle ($\overline{WE}$ high at the falling edge of $\overline{RAS}$)

The data on 8 I/Os are all cleared when $\overline{WE}$ is high at the falling edge of $\overline{RAS}$.

- Mask Block Write Mode ($\overline{WE}$ low at the falling edge of $\overline{RAS}$)

When $\overline{WE}$ is low at the falling edge of $\overline{RAS}$, HM538123B starts mask block write mode to clear the data on an optional I/O. The mask data is the same as that of a RAM write cycle. High I/O is cleared, low I/O is not cleared and the internal data is retained. The mask data is available in the $\overline{RAS}$ cycle. In page mode block write cycle, the mask data is retained during the page access.



*1

WE	I/O	Mode
Low	I/O Mask Data	Mask
High	Don't care	Non mask

I/O Mask Data

Low: Mask

High: Non Mask

Address Mask Data

I/O0	Column0 (A0 = 0, A1 = 0) Mask Data	Low: Mask
I/O1	Column1 (A0 = 1, A1 = 0) Mask Data	
I/O2	Column2 (A0 = 0, A1 = 1) Mask Data	
I/O3	Column3 (A0 = 1, A1 = 1) Mask Data	High: Non Mask

Figure 2 Use of Block Write

Transfer Operation

The HM538123B provides the read transfer cycle, split read transfer cycle, pseudo transfer cycle, write transfer cycle and split write transfer cycle as data transfer cycles. These transfer cycles are set by driving $\overline{CAS}$ high and $\overline{DT/OE}$ low at the falling edge of $\overline{RAS}$. They have following functions:

(1) Transfer data between row address and SAM data register (except for pseudo transfer cycle)
Read transfer cycle and split read transfer cycle: RAM to SAM
Write transfer cycle and split write transfer cycle: SAM to RAM

(2) Determine SI/O state (except for split read transfer cycle and split write transfer cycle)
Read transfer cycle: SI/O output
Pseudo transfer cycle and write transfer cycle: SI/O input

(3) Determine first SAM address to access after transferring at column address (SAM start address).

SAM start address must be determined by read transfer cycle or pseudo transfer cycle (split transfer cycle isn't available) before SAM access, after power on, and determined for each transfer cycle.

Read Transfer Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ low, $\overline{WE}$ high and DSF low at the falling edge of $\overline{RAS}$)

This cycle becomes read transfer cycle by driving $\overline{DT/OE}$ low, $\overline{WE}$ high and DSF low at the falling edge of $\overline{RAS}$. The row address data (256 x 8-bit) determined by this cycle is transferred to SAM data register synchronously at the rising edge of $\overline{DT/OE}$. After the rising edge of $\overline{DT/OE}$, the new address data outputs from SAM start address determined by column address. In read transfer cycle, $\overline{DT/OE}$ must be risen to transfer data from RAM to SAM.

This cycle can access SAM even during transfer (real time read transfer). In this case, the timing t_{SDD} (min) specified between the last SAM access before transfer and $\overline{DT/OE}$ rising edge and t_{SDH} (min) specified between the first SAM access and $\overline{DT/OE}$ rising edge must be satisfied. (See figure 3.)

When read transfer cycle is executed, SI/O becomes output state by first SAM access. Input must be set high impedance before t_{SZS} (min) of the first SAM access to avoid data contention.

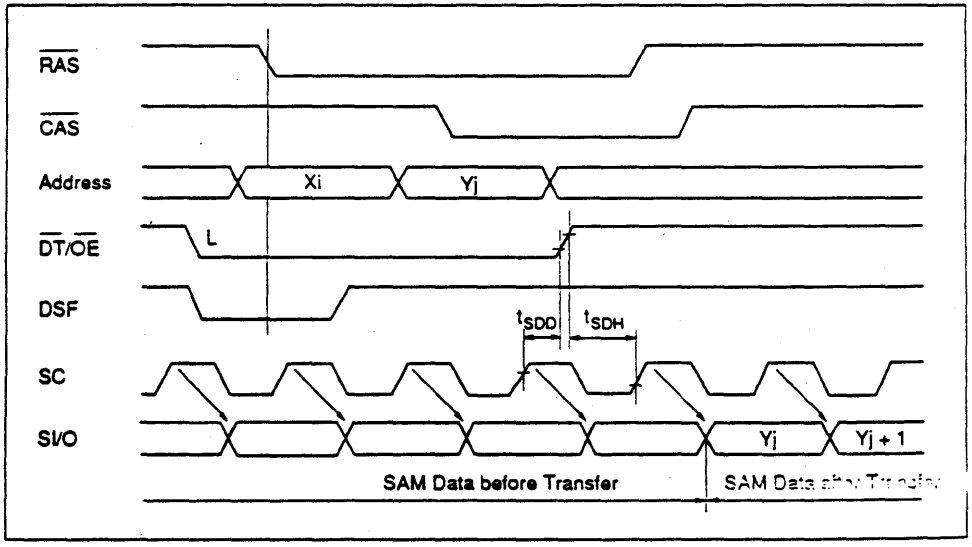


Figure 3 Real Time Read Transfer

Pseudo Transfer Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ low, $\overline{WE}$ low, $\overline{SE}$ high and DSF low at the falling edge of $\overline{RAS}$)

Pseudo transfer cycle switches SI/O to input state and set SAM start address without data transfer to RAM.
This cycle starts when $\overline{CAS}$ is high, $\overline{DT/OE}$ low, $\overline{WE}$ low, $\overline{SE}$ high and DSF low at the falling edge of $\overline{RAS}$. Data should be input to SI/O later than t_{SID} (min) after $\overline{RAS}$ becomes low to avoid data contention. SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. In this cycle, SAM access is inhibited during $\overline{RAS}$ low, therefore, SC must not be risen.

Write Transfer Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ low, $\overline{WE}$ low, $\overline{SE}$ low and DSF low at the falling edge of $\overline{RAS}$)

Write transfer cycle can transfer a row of data input by serial write cycle to RAM. The row address of data transferred into RAM is determined by the address at the falling edge of $\overline{RAS}$. The column address is specified as the first address for serial write after terminating this cycle. Also in this cycle, SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. SAM access is inhibited during $\overline{RAS}$ low. In this period, SC must not be risen. Data transferred to SAM by read transfer cycle or split read transfer cycle can be written to other addresses of RAM by write transfer cycle. However, the address to write data must be the same as that of the read transfer cycle or the split read transfer cycle (row address AX8).

Split Read Transfer Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ low, $\overline{WE}$ high and DSF high at the falling edge of $\overline{RAS}$)

To execute a continuous serial read by real time read transfer, HM538123B must satisfy SC and $\overline{DT/OE}$ timings and requires an external circuit to detect SAM last address. Split read transfer cycle makes it possible to execute a continuous serial read without the above timing limitation. Figure 4 shows the block diagram for a split transfer. SAM data register (DR) consists of 2 split buffers, whose organizations are 128-word x 8-bit each. Let us suppose that data is read from upper data register DR1 (The row address AX8 is 0 and SAM address A7 is 1.). When split read transfer is executed setting row address AX8 0 and SAM start addresses A0 to A6, 128-word x 8-bit data are transferred from RAM to the lower data register DR0 (SAM address A7 is 0) automatically. After data are read from data register DR1, data start to be read from SAM start addresses of data register DR0. If the next split read transfer isn't executed while data are read from data register DR0, data start to be read from SAM start address 0 of DR1 after data are read from data register DR0. If split read transfer is executed setting row address AX8 1 and SAM start addresses A0 to A6 while data are read from data register DR1, 128-word x 8-bit data are transferred to data register DR2. After data are read from data register DR1, data start to be read from SAM start addresses of data register DR2. If the next split read transfer isn't executed while data is read from data register DR2, data start to be read from SAM start address 0 of data register DR3 after data are read from data register DR2. In this time, SAM data is the one transferred to data register DR3 finally while row address AX8 is 1. In split read data transfer, the SAM start address A7 is automatically set in the data register which isn't used.
The data on SAM address A7, which will be accessed next, outputs to QSF, QSF is switched from low to high by accessing SAM last address 127 and from high to low by accessing address 255.
Split read transfer cycle is set when $\overline{CAS}$ is high, $\overline{DT/OE}$ is low, $\overline{WE}$ is high and DSF is high at the falling edge of $\overline{RAS}$. The cycle can be executed asyncronously with SC. However, HM538123B must be satisfied t_{STS} (min) timing specified between SC rising and $\overline{RAS}$ falling. SAM start address must be accessed, satisfying t_{RST} (min), t_{CST} (min) and t_{AST} (min) timings specified between $\overline{RAS}$ or $\overline{CAS}$ falling and column address. (See figure 5.)
In split read transfer, SI/O isn't switched to output state. Therefore, read transfer must be executed to switch SI/O to output state when the previous transfer cycle is pseudo transfer or write transfer cycle.

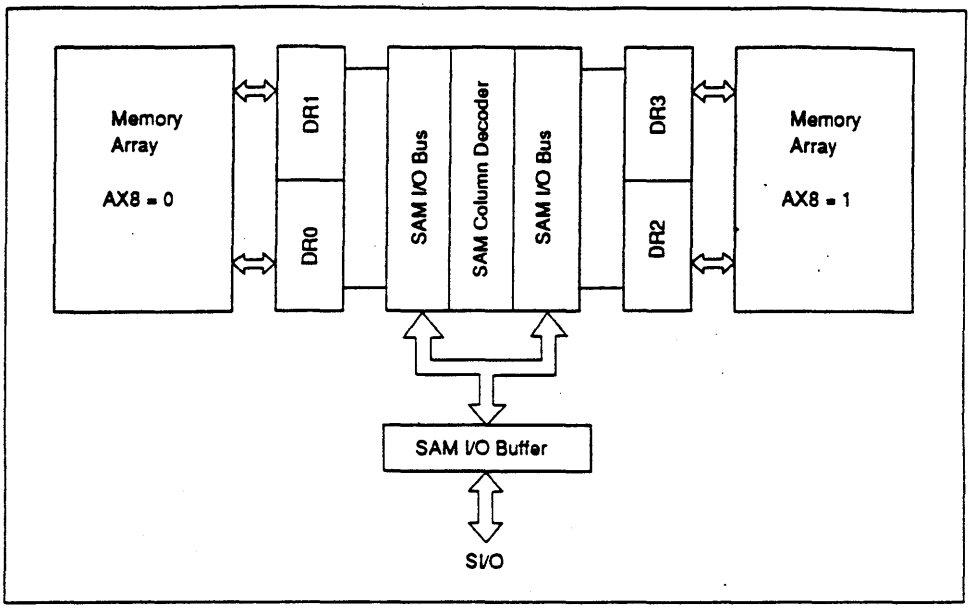


Figure 4 Block Diagram for Split Transfer

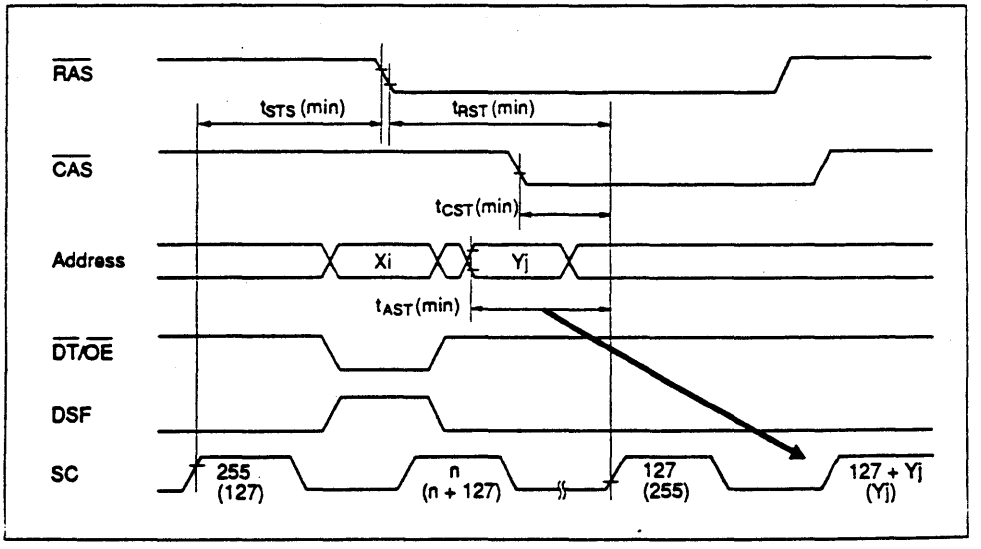


Figure 5 Limitation in Split Transfer

Split Write Transfer Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ low, $\overline{WE}$ low and DSF high at the falling edge of $\overline{RAS}$)

A continuous serial write cannot be executed because accessing SAM is inhibited during $\overline{RAS}$ low in write transfer. Split write transfer cycle makes it possible. In this cycle, t_{STS} (min), t_{RST} (min), t_{CST} (min) and t_{AST} (min) timings must be satisfied like split read transfer cycle. And it is impossible to switch SI/O to input state in this cycle. If SI/O is in output state, pseudo transfer cycle should be executed to switch SI/O into input state. Data transferred to SAM by read transfer cycle or split read transfer cycle can be written to other addresses of RAM by split write transfer cycle. However, pseudo transfer cycle must be executed before split write transfer cycle. And the MSB of row address (AX8) to write data must be the same as that of the read transfer cycle or the split read transfer cycle.

SAM Port Operation

Serial Read Cycle

SAM port is in read mode when the previous data transfer cycle is read transfer cycle. Access is synchronized with SC rising, and SAM data is output from SI/O. When $\overline{SE}$ is set high, SI/O becomes high impedance, and the internal pointer is incremented by the SC rising. After indicating the last address (address 255), the internal pointer indicates address 0 at the next access.

Serial Write Cycle

If previous data transfer cycle is pseudo transfer cycle or write transfer cycle, SAM port goes into write mode. In this cycle, SI/O data is fetched into data register at the SC rising edge like in the serial read cycle. If $\overline{SE}$ is high, SI/O data isn't fetched into data register. Internal pointer is incremented by the SC rising, so $\overline{SE}$ high can be used as mask data for SAM. After indicating the last address (address 255), the internal pointer indicates address 0 at the next access.

Refresh

RAM Refresh

RAM, which is composed of dynamic circuits, requires refresh to retain data. Refresh is executed by accessing all 512 row addresses within 8 ms. There are three refresh cycles: (1) $\overline{RAS}$-only refresh cycle, (2) $\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh cycle, and (3) Hidden refresh cycle. Besides them, the cycles which activate $\overline{RAS}$ such as read/write cycles or transfer cycles can refresh the row address. Therefore, no refresh cycle is required when all row addresses are accessed within 8 ms.

(1) $\overline{RAS}$-Only Refresh Cycle: $\overline{RAS}$-only refresh cycle is executed by activating only $\overline{RAS}$ cycle with $\overline{CAS}$ fixed to high after inputting the row address (=refresh address) from external circuits. To distinguish this cycle from data transfer cycle, $\overline{DT/OE}$ must be high at the falling edge of $\overline{RAS}$.

(2) CBR Refresh Cycle: CBR refresh cycle is set by activating $\overline{CAS}$ before $\overline{RAS}$. In this cycle, refresh address need not to be input through external circuits because it is input through an internal refresh counter. In this cycle, output is in high impedance and power dissipation is lowered because $\overline{CAS}$ circuits don't operate.

(3) Hidden Refresh Cycle: Hidden refresh cycle executes CBR refresh with the data output by reactivating $\overline{RAS}$ when $\overline{DT/OE}$ and $\overline{CAS}$ keep low in normal RAM read cycles.

SAM Refresh

SAM parts (data register, shift register and selector), organized as fully static circuitry, require no refresh.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal voltage*1	V_T	−1.0 to +7.0	V
Power supply voltage*1	V_{CC}	−0.5 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C

Note: 1. Relative to V_{SS}.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage*1	V_{CC}	4.5	5.0	5.5	V
Input high voltage*1	V_{IH}	2.4	—	6.5	V
Input low voltage*1	V_{IL}	−0.5*2	—	0.8	V

Notes: 1. All voltages referenced to V_{SS}
2. −3.0 V for pulse width ≤ 10 ns

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

		HM538123B										
		-6		-7		-8		-10		Unit	Test Conditions	
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		RAM port	SAM port
Operating current	I_{CC1}	—	75	—	70	—	60	—	55	mA	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC7}	—	125	—	120	—	100	—	95	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = Min
Standby current	I_{CC2}	—	7	—	7	—	7	—	7	mA	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC8}	—	50	—	50	—	40	—	40	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = Min
$\overline{RAS}$-only refresh current	I_{CC3}	—	75	—	70	—	60	—	55	mA	$\overline{RAS}$ cycling $\overline{CAS}$ = V_{IH} t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC9}	—	125	—	120	—	100	—	95	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = Min
Page mode current	I_{CC4}	—	80	—	80	—	70	—	65	mA	$\overline{CAS}$ cycling $\overline{RAS}$ = V_{IL} t_{PC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC10}	—	130	—	130	—	110	—	105	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = Min
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC5}	—	50	—	45	—	40	—	35	mA	$\overline{RAS}$ cycling t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC11}	—	100	—	95	—	80	—	75	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = Min
Data transfer current	I_{CC6}	—	80	—	75	—	65	—	60	mA	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC12}	—	130	—	125	—	105	—	100	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = Min
Input leakage current	I_{LI}	-10	10	-10	10	-10	10	-10	10	µA		
Output leakage current	I_{LO}	-10	10	-10	10	-10	10	-10	10	µA		
Output high voltage	V_{OH}	2.4	—	2.4	—	2.4	—	2.4	—	V	I_{OH} = -2 mA	
Output low voltage	V_{OL}	—	0.4	—	0.4	—	0.4	—	0.4	V	I_{OL} = 4.2 mA	

Note: 1. I_{CC} depends on output loading condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed once while $\overline{RAS}$ is low and $\overline{CAS}$ is high.

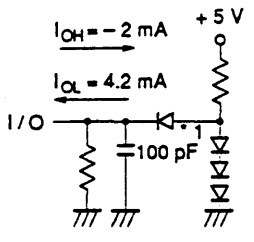
Capacitance (Ta = 25°C, V_{CC} = 5 V, f = 1 MHz, Bias: Clock, I/O = V_{CC}, address = V_{SS})

Item	Symbol	Min	Typ	Max	Unit
Address	C_{I1}	—	—	5	pF
Clock	C_{I2}	—	—	5	pF
I/O, SI/O, QSF	$C_{I/O}$	—	—	7	pF

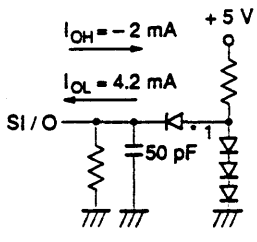
AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)*1,*16

Test Conditions

Input rise and fall time : 5 ns
Output load : See figures
Input pulse levels: V_{SS} to 3.0 V
Input timing reference levels : 0.8 V, 2.4 V
Output timing reference levels : 0.8 V, 2.0 V



Output Load (A)



Output Load (B)

Note: 1. Including scope & jig

Common Parameter

Item	Symbol	HM538123B -6 Min	-6 Max	-7 Min	-7 Max	-8 Min	-8 Max	-10 Min	-10 Max	Unit	Note
Random read or write cycle time	t_{RC}	125	—	135	—	150	—	180	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	55	—	55	—	60	—	70	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	—	20	—	20	—	25	—	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	15	—	15	—	15	—	15	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	20	60	20	75	ns	2
$\overline{RAS}$ hold time referenced to $\overline{CAS}$	t_{RSH}	20	—	20	—	20	—	25	—	ns	
$\overline{CAS}$ hold time referenced to $\overline{RAS}$	t_{CSH}	60	—	70	—	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	10	—	10	—	ns	
Transition time (rise to fall)	t_T	3	50	3	50	3	50	3	50	ns	3
Refresh period	t_{REF}	—	8	—	8	—	8	—	8	ms	
$\overline{DT}$ to $\overline{RAS}$ setup time	t_{DTS}	0	—	0	—	0	—	0	—	ns	
$\overline{DT}$ to $\overline{RAS}$ hold time	t_{DTH}	10	—	10	—	10	—	10	—	ns	
DSF to $\overline{RAS}$ setup time	t_{FSR}	0	—	0	—	0	—	0	—	ns	
DSF to $\overline{RAS}$ hold time	t_{RFH}	10	—	10	—	10	—	10	—	ns	
DSF to $\overline{CAS}$ setup time	t_{FSC}	0	—	0	—	0	—	0	—	ns	
DSF to $\overline{CAS}$ hold time	t_{CFH}	15	—	15	—	15	—	15	—	ns	
Data-in to $\overline{CAS}$ delay time	t_{DZC}	0	—	0	—	0	—	0	—	ns	4
Data-in to $\overline{OE}$ delay time	t_{DZO}	0	—	0	—	0	—	0	—	ns	4
Output buffer turn-off delay referenced to $\overline{CAS}$	t_{OFF1}	—	20	—	20	—	20	—	20	ns	5
Output buffer turn-off delay referenced to $\overline{OE}$	t_{OFF2}	—	20	—	20	—	20	—	20	ns	5

Read Cycle (RAM), Page Mode Read Cycle

		HM538123B									
		-6		-7		-8		-10			
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Note
Access time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	ns	6, 7
Access time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	20	—	25	ns	7, 8
Access time from $\overline{OE}$	t_{OAC}	—	20	—	20	—	20	—	25	ns	7
Address access time	t_{AA}	—	35	—	35	—	40	—	45	ns	7, 9
Read command setup time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	0	—	0	—	ns	10
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	10	—	ns	10
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	35	15	40	15	55	ns	2
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	—	35	—	40	—	45	—	ns	
Column address to $\overline{CAS}$ lead time	t_{CAL}	35	—	35	—	40	—	45	—	ns	
Page mode cycle time	t_{PC}	45	—	45	—	50	—	55	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	—	10	—	10	—	10	—	ns	
Access time from $\overline{CAS}$ precharge	t_{ACP}	—	40	—	40	—	45	—	50	ns	
Page mode $\overline{RAS}$ pulse width	t_{RASP}	60	100000	70	100000	80	100000	100	100000	ns	

Write Cycle (RAM), Page Mode Write Cycle, Color Register Set Cycle

		HM538123B									
		-6		-7		-8		-10			
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Note
Write command setup time	t_{WCS}	0	—	0	—	0	—	0	—	ns	11
Write command hold time	t_{WCH}	15	—	15	—	15	—	15	—	ns	
Write command pulse width	t_{WP}	15	—	15	—	15	—	15	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	—	20	—	20	—	20	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	—	20	—	20	—	20	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	0	—	ns	12
Data-in hold time	t_{DH}	15	—	15	—	15	—	15	—	ns	12
$\overline{WE}$ to $\overline{RAS}$ setup time	t_{WS}	0	—	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ hold time	t_{WH}	10	—	10	—	10	—	10	—	ns	
Mask data to $\overline{RAS}$ setup time	t_{MS}	0	—	0	—	0	—	0	—	ns	
Mask data to $\overline{RAS}$ hold time	t_{MH}	10	—	10	—	10	—	10	—	ns	
$\overline{OE}$ hold time referenced to $\overline{WE}$	t_{OEH}	20	—	20	—	20	—	20	—	ns	
Page mode cycle time	t_{PC}	45	—	45	—	50	—	55	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ to data-in delay time	t_{CDD}	20	—	20	—	20	—	20	—	ns	13
Page mode $\overline{RAS}$ pulse width	t_{RASP}	60	100000	70	100000	80	100000	100	100000	ns	

Read-Modify-Write Cycle

		HM538123B									
		-6		-7		-8		-10			
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Note
Read-modify-write cycle time	t_{RWC}	175	—	185	—	200	—	230	—	ns	
$\overline{RAS}$ pulse width (read-modify-write cycle)	t_{RWS}	110	10000	120	10000	130	10000	150	10000	ns	
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	45	—	45	—	45	—	50	—	ns	14
Column address to $\overline{WE}$ delay time	t_{AWD}	60	—	60	—	65	—	70	—	ns	14
$\overline{OE}$ to data-in delay time	t_{ODD}	20	—	20	—	20	—	20	—	ns	12
Access time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	ns	6, 7
Access time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	20	—	25	ns	7, 8
Access time from $\overline{OE}$	t_{OAC}	—	20	—	20	—	20	—	25	ns	7
Address access time	t_{AA}	—	35	—	35	—	40	—	45	ns	7, 9
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	35	15	40	15	55	ns	
Read command setup time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	—	20	—	20	—	20	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	—	20	—	20	—	20	—	ns	
Write command pulse width	t_{WP}	15	—	15	—	15	—	15	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	0	—	ns	12
Data-in hold time	t_{DH}	15	—	15	—	15	—	15	—	ns	12
$\overline{OE}$ hold time referenced to $\overline{WE}$	t_{OEH}	20	—	20	—	20	—	20	—	ns	

Refresh Cycle

Item	Symbol	HM538123B -6 Min	-6 Max	-7 Min	-7 Max	-8 Min	-8 Max	-10 Min	-10 Max	Unit	Note
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10	—	10	—	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	—	10	—	10	—	10	—	ns	

Flash Write Cycle, Block Write Cycle

Item	Symbol	HM538123B -6 Min	-6 Max	-7 Min	-7 Max	-8 Min	-8 Max	-10 Min	-10 Max	Unit	Note
$\overline{CAS}$ to data-in delay time	t_{CDD}	20	—	20	—	20	—	20	—	ns	13
$\overline{OE}$ to data-in delay time	t_{ODD}	20	—	20	—	20	—	20	—	ns	13

Read Transfer Cycle

Item	Symbol	HM538123B -6- Min	-6- Max	7 Min	7 Max	-8 Min	-8 Max	-10 Min	-10 Max	Unit	Note
$\overline{DT}$ hold time referenced to $\overline{RAS}$	t_{RDH}	50	10000	60	10000	65	10000	80	10000	ns	
$\overline{DT}$ hold time referenced to $\overline{CAS}$	t_{CDH}	20	—	20	—	20	—	25	—	ns	
$\overline{DT}$ hold time referenced to column address	t_{ADH}	25	—	25	—	30	—	30	—	ns	
$\overline{DT}$ precharge time	t_{DTP}	20	—	20	—	20	—	30	—	ns	
$\overline{DT}$ to $\overline{RAS}$ delay time	t_{DRD}	65	—	65	—	70	—	80	—	ns	
SC to $\overline{RAS}$ setup time	t_{SRS}	25	—	25	—	30	—	30	—	ns	
1st SC to $\overline{RAS}$ hold time	t_{SRH}	60	—	70	—	80	—	100	—	ns	
1st SC to $\overline{CAS}$ hold time	t_{SCH}	25	—	25	—	25	—	25	—	ns	

Read Transfer Cycle (cont)

Item	Symbol	HM538123B -6- Min	-6- Max	7 Min	7 Max	-8 Min	-8 Max	-10 Min	-10 Max	Unit	Note
1st SC to column address hold time	t_{SAH}	40	—	40	—	45	—	50	—	ns	
Last SC to $\overline{DT}$ delay time	t_{SDD}	5	—	5	—	5	—	5	—	ns	
1st SC to $\overline{DT}$ hold time	t_{SDH}	10	—	10	—	15	—	15	—	ns	
$\overline{RAS}$ to QSF delay time	t_{RQD}	—	65	—	70	—	75	—	85	ns	15
$\overline{CAS}$ to QSF delay time	t_{CQD}	—	35	—	35	—	40	—	40	ns	15
$\overline{DT}$ to QSF delay time	t_{DQD}	—	35	—	35	—	35	—	35	ns	15
QSF hold time referenced to $\overline{RAS}$	t_{RQH}	20	—	20	—	20	—	25	—	ns	
QSF hold time referenced to $\overline{CAS}$	t_{CQH}	5	—	5	—	5	—	5	—	ns	
QSF hold time referenced to $\overline{DT}$	t_{DQH}	5	—	5	—	5	—	5	—	ns	
Serial data-in to 1st SC delay time	t_{SZS}	0	—	0	—	0	—	0	—	ns	
Serial clock cycle time	t_{SCC}	25	—	25	—	30	—	30	—	ns	
SC pulse width	t_{SC}	5	—	5	—	10	—	10	—	ns	
SC precharge time	t_{SCP}	10	—	10	—	10	—	10	—	ns	
SC access time	t_{SCA}	—	20	—	22	—	25	—	25	ns	15
Serial data-out hold time	t_{SOH}	5	—	5	—	5	—	5	—	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	15	—	15	—	15	—	ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	35	15	40	15	55	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	—	35	—	40	—	45	—	ns	
$\overline{RAS}$ precharge to $\overline{DT}$ high hold time	t_{DTHH}	10	—	10	—	10	—	10	—	ns	

Pseudo Transfer Cycle, Write Transfer Cycle

Item	Symbol	HM538123B -6- Min	-6- Max	-7 Min	-7 Max	-8 Min	-8 Max	-10 Min	-10 Max	Unit	Note
$\overline{SE}$ setup time referenced to $\overline{RAS}$	t_{ES}	0	—	0	—	0	—	0	—	ns	
$\overline{SE}$ hold time referenced to $\overline{RAS}$	t_{EH}	10	—	10	—	10	—	10	—	ns	
SC setup time referenced to $\overline{RAS}$	t_{SRS}	25	—	25	—	30	—	30	—	ns	
$\overline{RAS}$ to SC delay time	t_{SRD}	20	—	20	—	25	—	25	—	ns	
Serial output buffer turn-off time referenced to $\overline{RAS}$	t_{SRZ}	10	40	10	40	10	45	10	50	ns	
$\overline{RAS}$ to serial data-in delay time	t_{SID}	40	—	40	—	45	—	50	—	ns	
$\overline{RAS}$ to QSF delay time	t_{RQD}	—	65	—	70	—	75	—	85	ns	15
$\overline{CAS}$ to QSF delay time	t_{CQD}	—	35	—	35	—	40	—	40	ns	15
QSF hold time referenced to $\overline{RAS}$	t_{RQH}	20	—	20	—	20	—	25	—	ns	
QSF hold time referenced to $\overline{CAS}$	t_{CQH}	5	—	5	—	5	—	5	—	ns	
Serial clock cycle time	t_{SCC}	25	—	25	—	30	—	30	—	ns	
SC pulse width	t_{SC}	5	—	5	—	10	—	10	—	ns	
SC precharge time	t_{SCP}	10	—	10	—	10	—	10	—	ns	
SC access time	t_{SCA}	—	20	—	22	—	25	—	25	ns	15
$\overline{SE}$ access time	t_{SEA}	—	20	—	22	—	25	—	25	ns	15
Serial data-out hold time	t_{SOH}	5	—	5	—	5	—	5	—	ns	
Serial write enable setup time	t_{SWS}	5	—	5	—	5	—	5	—	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	15	—	15	—	15	—	ns	

Split Read Transfer Cycle, Split Write Transfer Cycle

		HM538123B									
		-6-		7		-8		-10			
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Note
Split transfer setup time	t_{STS}	20	—	20	—	20	—	25	—	ns	
Split transfer hold time referenced to $\overline{RAS}$	t_{RST}	60	—	70	—	80	—	100	—	ns	
Split transfer hold time referenced to $\overline{CAS}$	t_{CST}	20	—	20	—	20	—	25	—	ns	
Split transfer hold time referenced to column address	t_{AST}	35	—	35	—	40	—	45	—	ns	
SC to QSF delay time	t_{SQD}	—	30	—	30	—	30	—	30	ns	15
QSF hold time referenced to SC	t_{SQH}	5	—	5	—	5	—	5	—	ns	
Serial clock cycle time	t_{SCC}	25	—	25	—	30	—	30	—	ns	
SC pulse width	t_{SC}	5	—	5	—	10	—	10	—	ns	
SC precharge time	t_{SCP}	10	—	10	—	10	—	10	—	ns	
SC access time	t_{SCA}	—	20	—	22	—	25	—	25	ns	15
Serial data-out hold time	t_{SOH}	5	—	5	—	5	—	5	—	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	15	—	15	—	15	—	ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	35	15	40	15	55	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	—	35	—	40	—	45	—	ns	

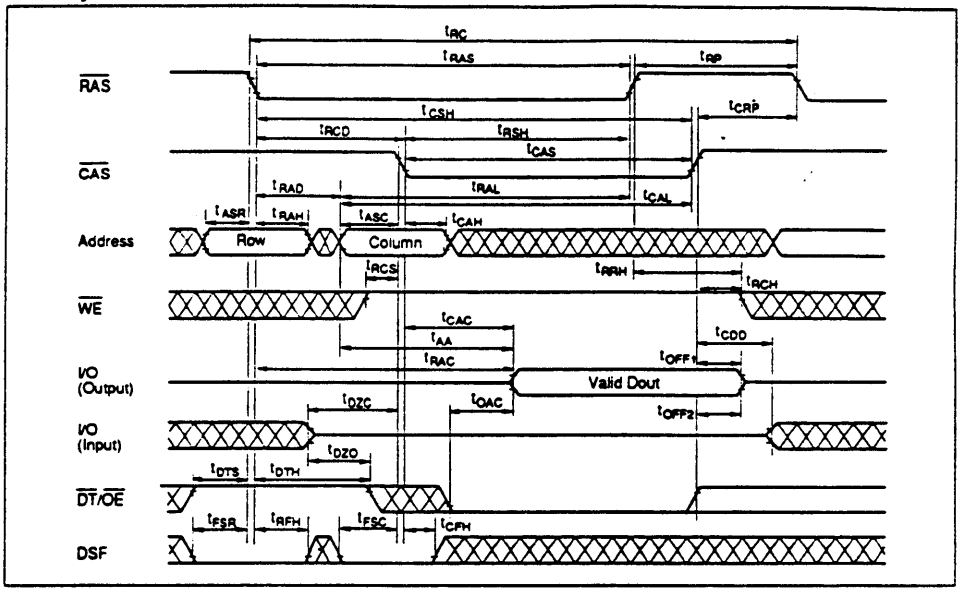
Serial Read Cycle, Serial Write Cycle

		HM538123B									
		-6-		7		-8		-10			
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Note
Serial clock cycle time	t_{SCC}	25	—	25	—	30	—	30	—	ns	
SC pulse width	t_{SC}	5	—	5	—	10	—	10	—	ns	
SC precharge width	t_{SCP}	10	—	10	—	10	—	10	—	ns	
Access time from SC	t_{SCA}	—	20	—	22	—	25	—	25	ns	15
Access time from $\overline{SE}$	t_{SEA}	—	20	—	22	—	25	—	25	ns	15
Serial data-out hold time	t_{SOH}	5	—	5	—	5	—	5	—	ns	
Serial output buffer turn-off time referenced to $\overline{SE}$	t_{SEZ}	—	20	—	20	—	20	—	20	ns	5
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	15	—	15	—	15	—	ns	
Serial write enable setup time	t_{SWS}	5	—	5	—	5	—	5	—	ns	
Serial write enable hold time	t_{SWH}	15	—	15	—	15	—	15	—	ns	
Serial write disable setup time	t_{SWIS}	5	—	5	—	5	—	5	—	ns	
Serial write disable hold time	t_{SWIH}	15	—	15	—	15	—	15	—	ns	

Notes:
1. AC measurements assume t_T = 5 ns.
2. When $t_{RCD} > t_{RCD}$ (max) or $t_{RAD} > t_{RAD}$ (max), access time is specified by t_{CAC} or t_{AA}.
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition time t_T is measured between V_{IH} and V_{IL}.
4. Data input must be floating before output buffer is turned on. In read cycle, read-modify-write cycle and delayed write cycle, either t_{DZC} (min) or t_{DZO} (min) must be satisfied.
5. t_{OFF1} (max), t_{OFF2} (max) and t_{SEZ} (max) are defined as the time at which the output achieves the open circuit condition (V_{OH} – 100 mV, V_{OL} + 100 mV).
6. Assume that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
7. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
8. When $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max), access time is specified by t_{CAC}.
9. When $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max), access time is specified by t_{AA}.
10. If either t_{RCH} of t_{RRH} is satisfied, operation is guaranteed.
11. When $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle, and I/O pins remain in an open circuit (high impedance) condition.
12. These parameters are specified by the later falling edge of $\overline{CAS}$ or $\overline{WE}$.
13. Either t_{CDD} (min) or t_{ODD} (min) must be satisfied because output buffer must be turned off by $\overline{CAS}$ or $\overline{OE}$ prior to applying data to the device when output buffer is on.
14. When $t_{AWD} \geq t_{AWD}$ (min) and $t_{CWD} \geq t_{CWD}$ (min) in read-modify-write cycle, the data of the selected address outputs to an I/O pin and input data is written into the selected address. t_{ODD} (min) must be satisfied because output buffer must be turned off by $\overline{OE}$ prior to applying data to the device.
15. Measured with a load circuit equivalent to 2 TTL loads and 50 pF.
16. After power-up, pause for 100 µs or more and execute at least 8 initialization cycle (normal memory cycle or refresh cycle), then start operation.

Timing Waveforms *17

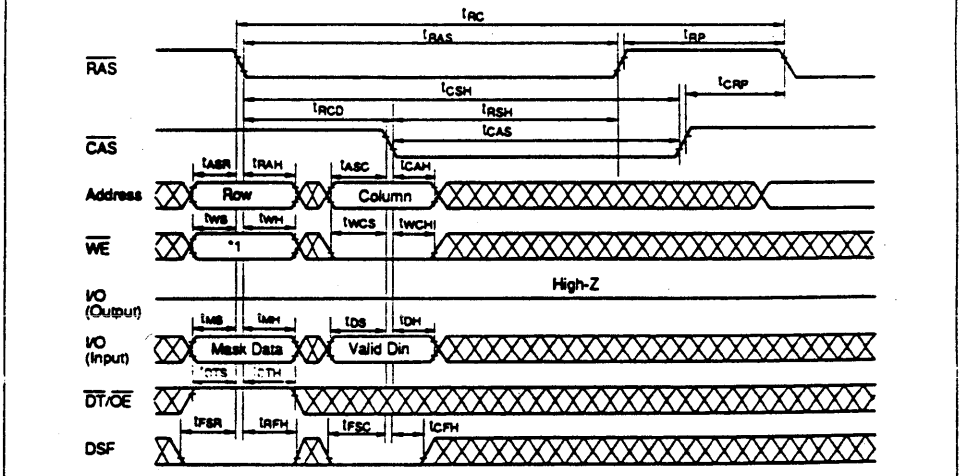
Read Cycle



Note17: H or L (H: V_{IH} (min) ≤ V_{IN} ≤ V_{IH} (max), L: V_{IL} (min) ≤ V_{IN} ≤ V_{IL} (max))

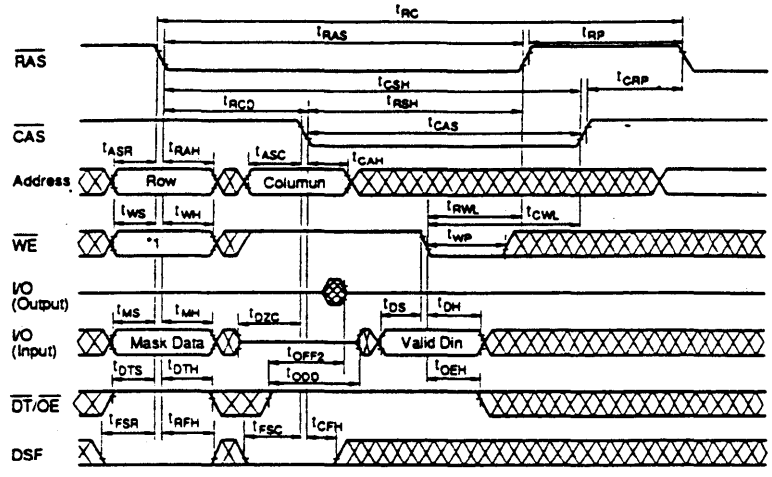
Invalid Dout

Early Write Cycle



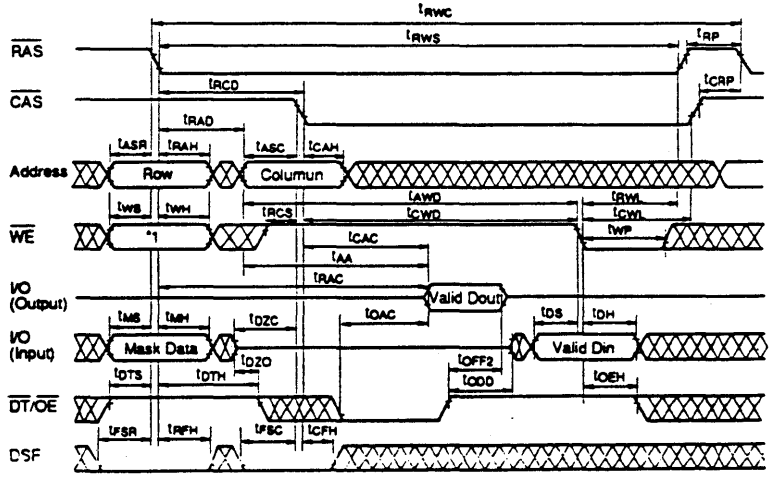
Note: 1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

Delayed Write Cycle



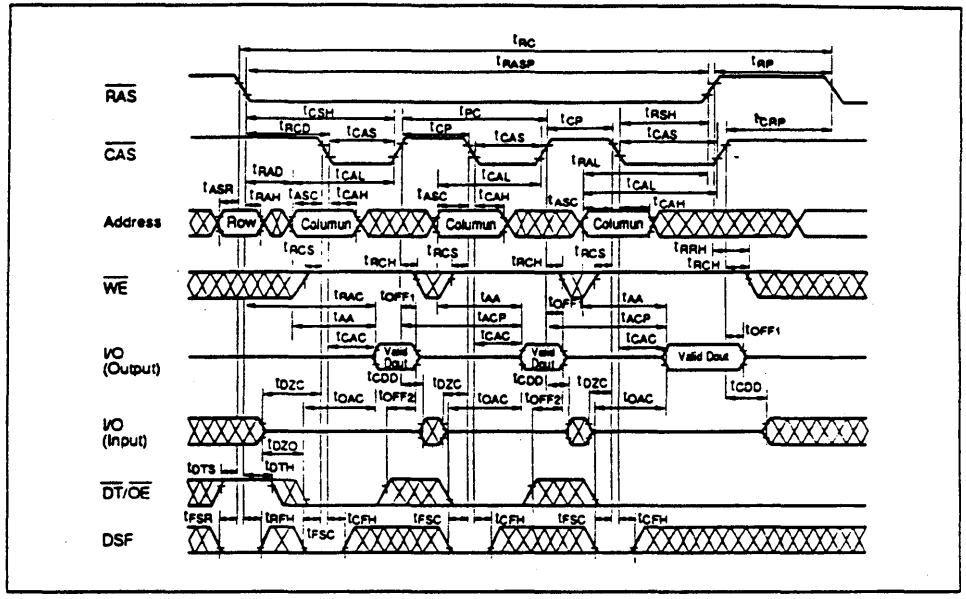
Note: 1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

Read-Modify-Write Cycle

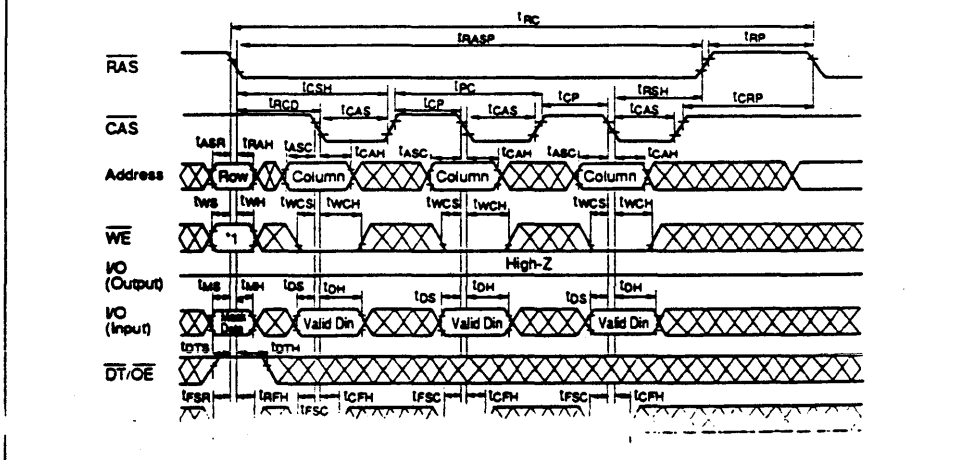


Note: 1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

Page Mode Read Cycle

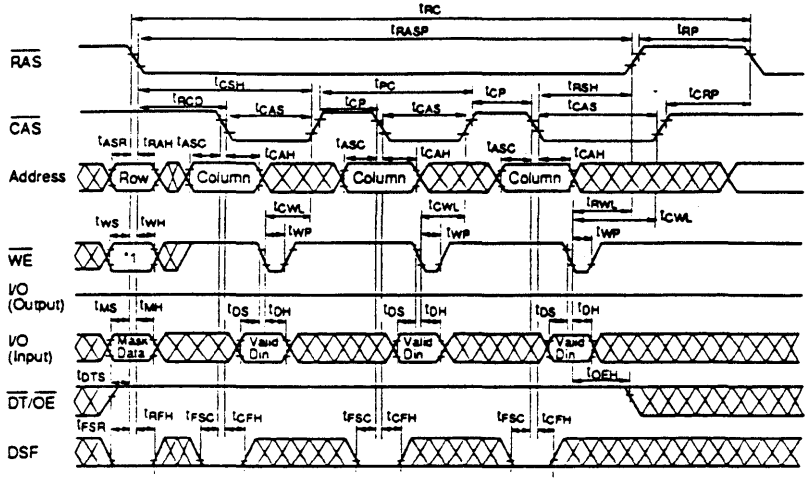


Page Mode Write Cycle (Early Write)



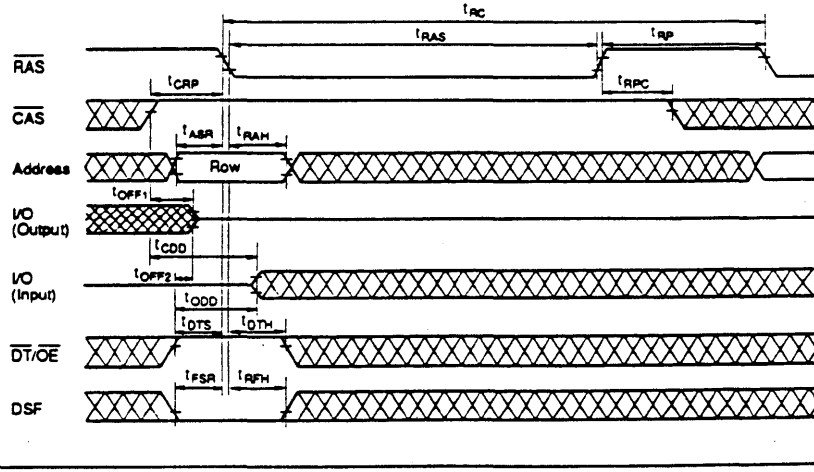
Note: 1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

Page Mode Write Cycle (Delayed Write)

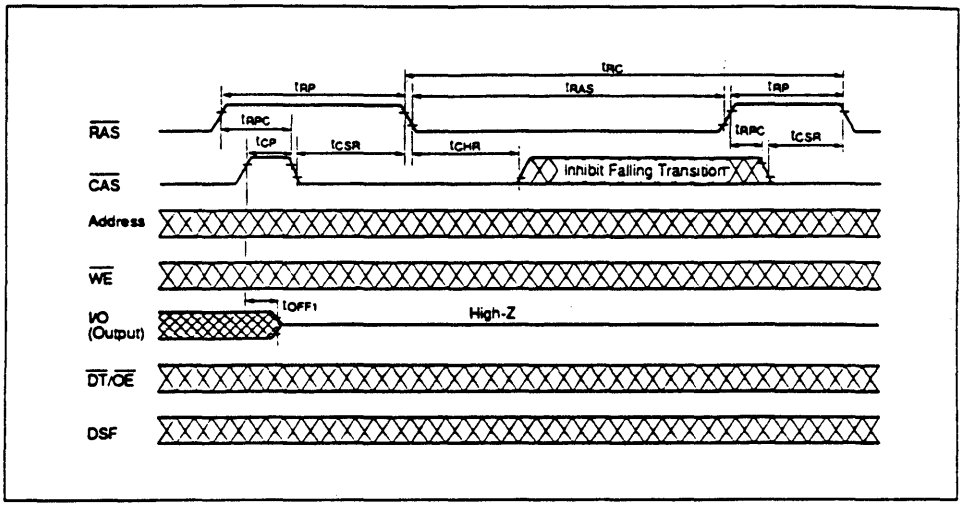


Note: 1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

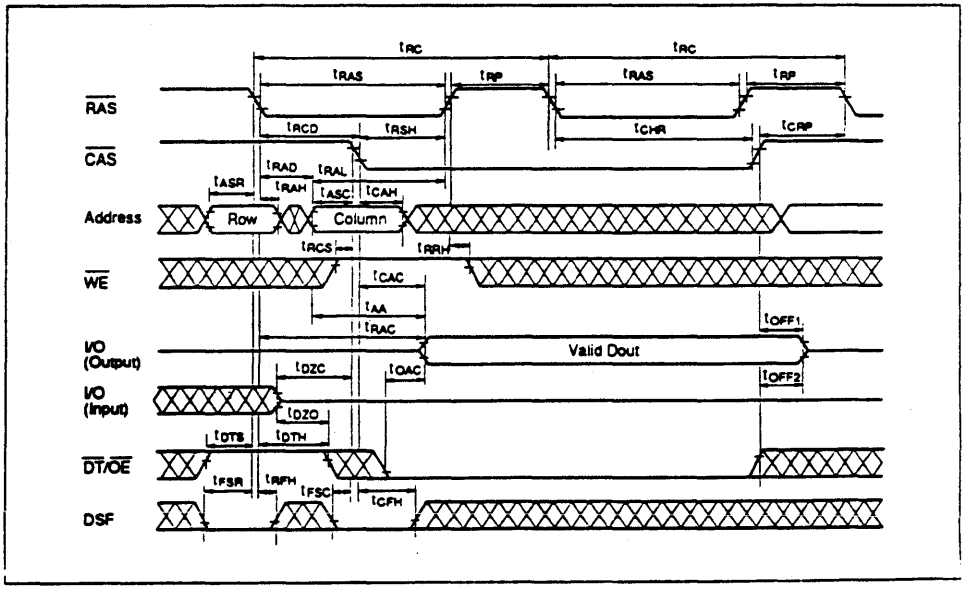
$\overline{RAS}$-Only Refresh Cycle



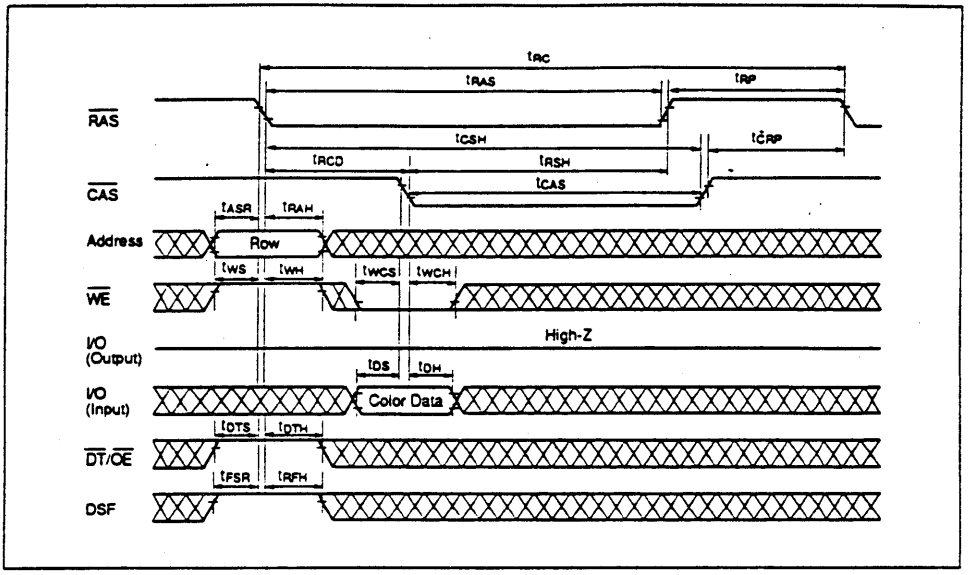
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle



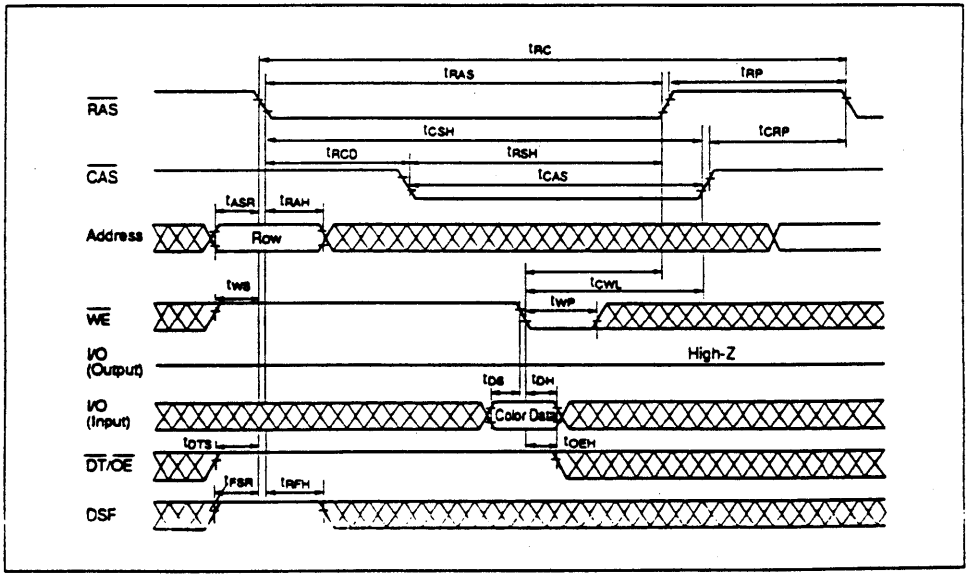
Hidden Refresh Cycle



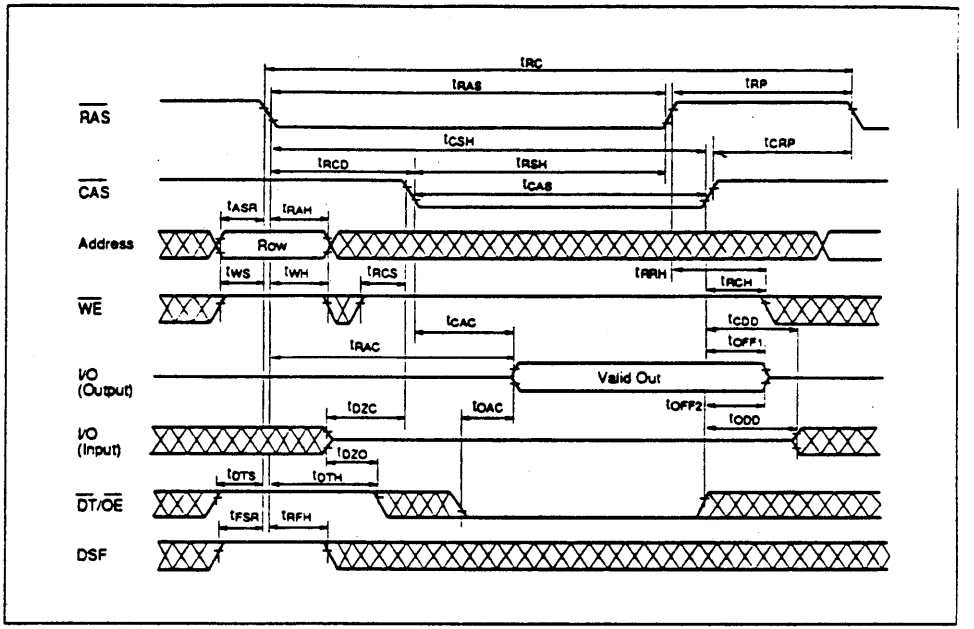
Color Register Set Cycle (Early Write)



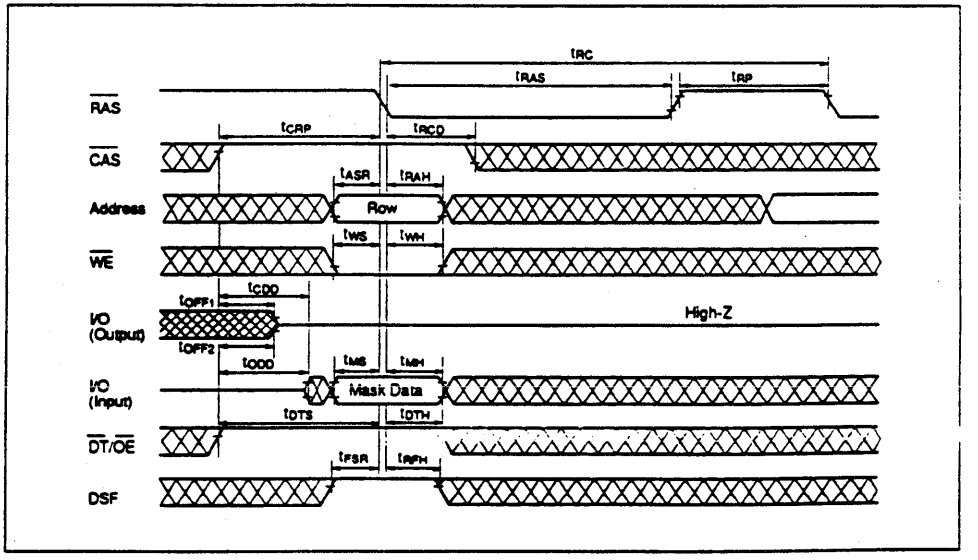
Color Register Set Cycle (Delayed Write)



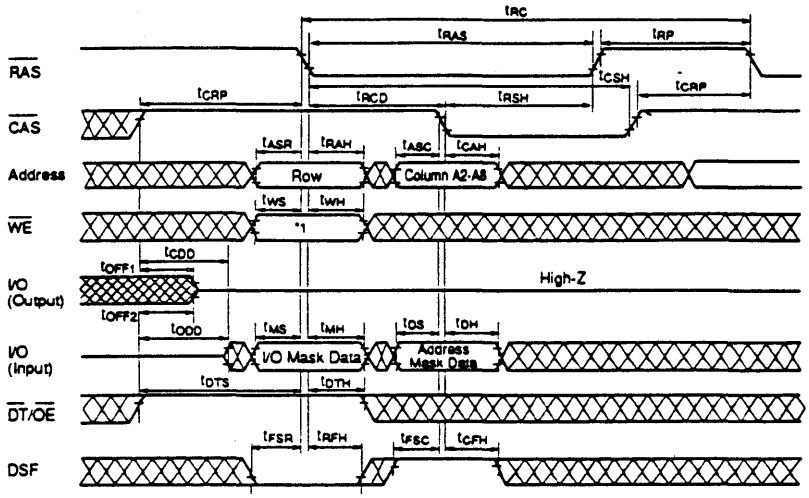
Color Register Read Cycle



Flash Write Cycle

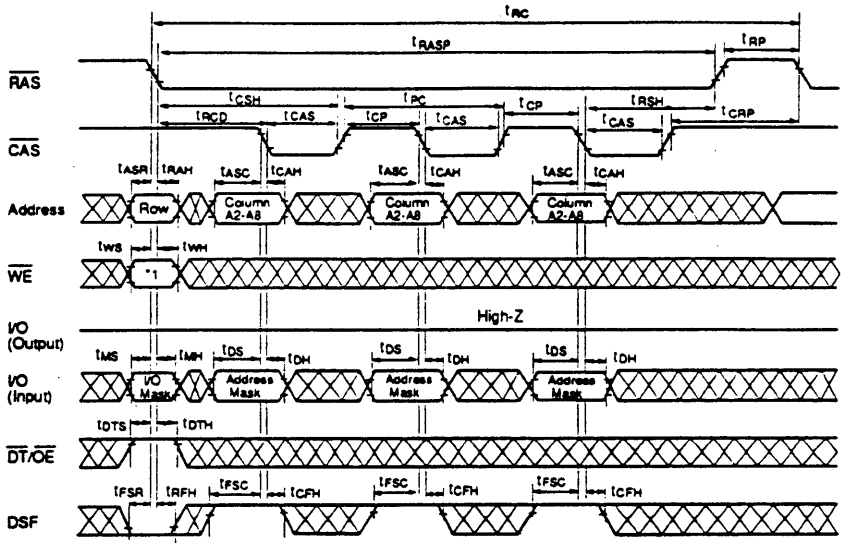


Block Write Cycle



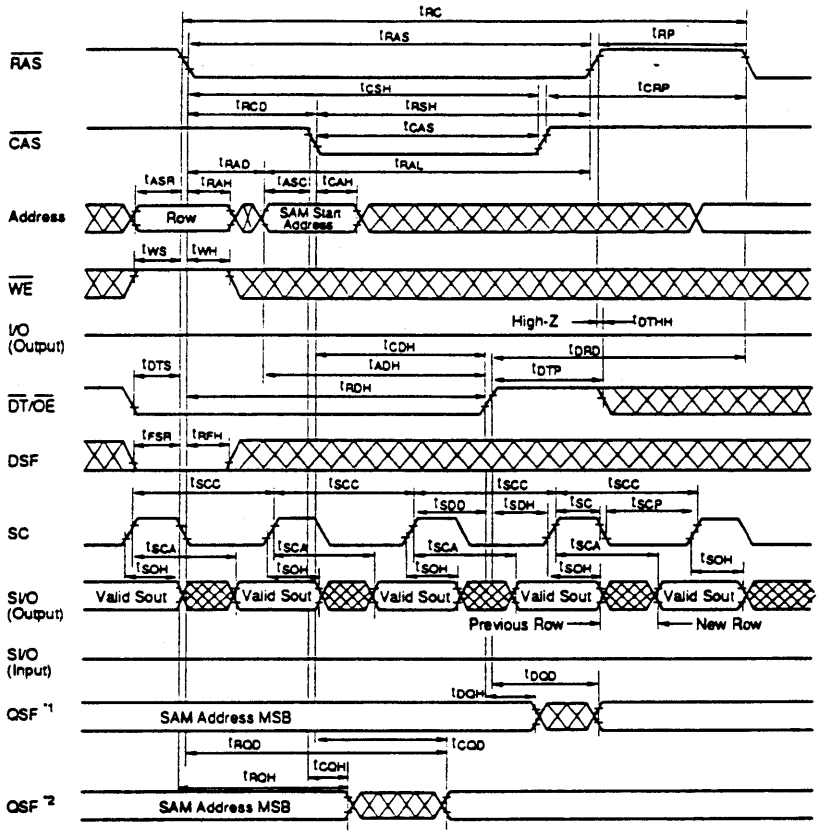
Note: 1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

Page Mode Block Write Cycle



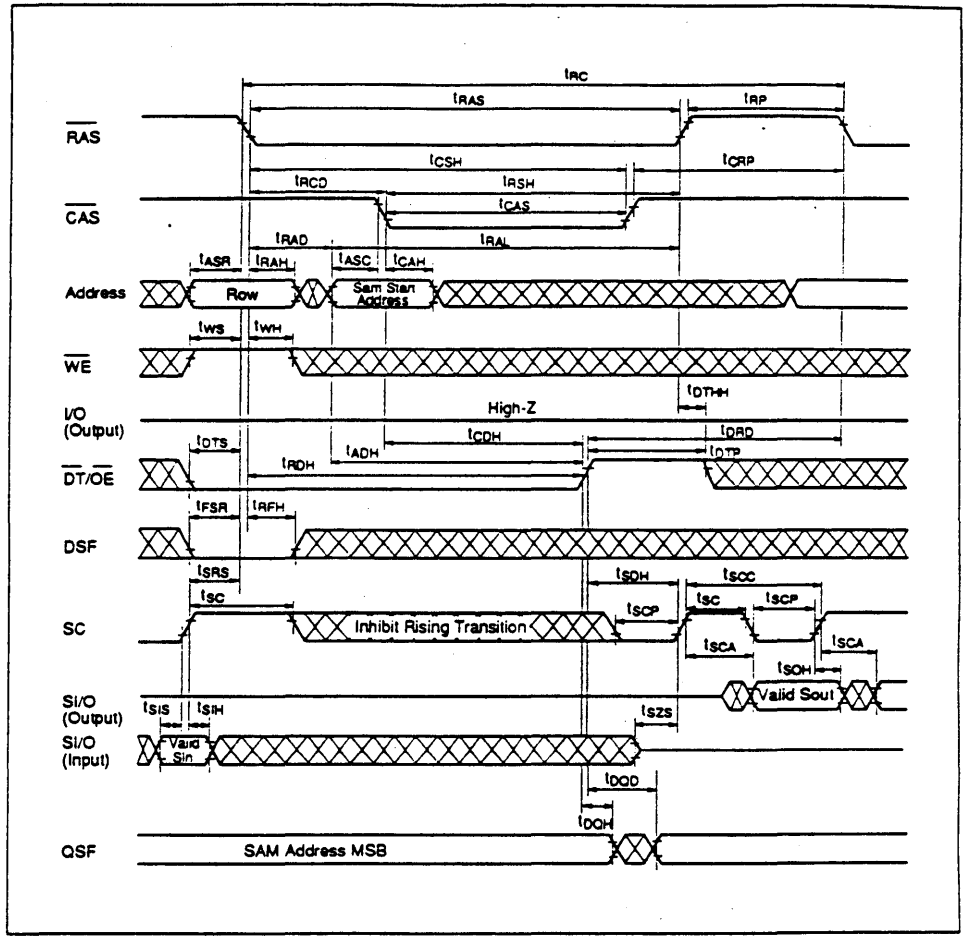
Note: 1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

Read Transfer Cycle (1)

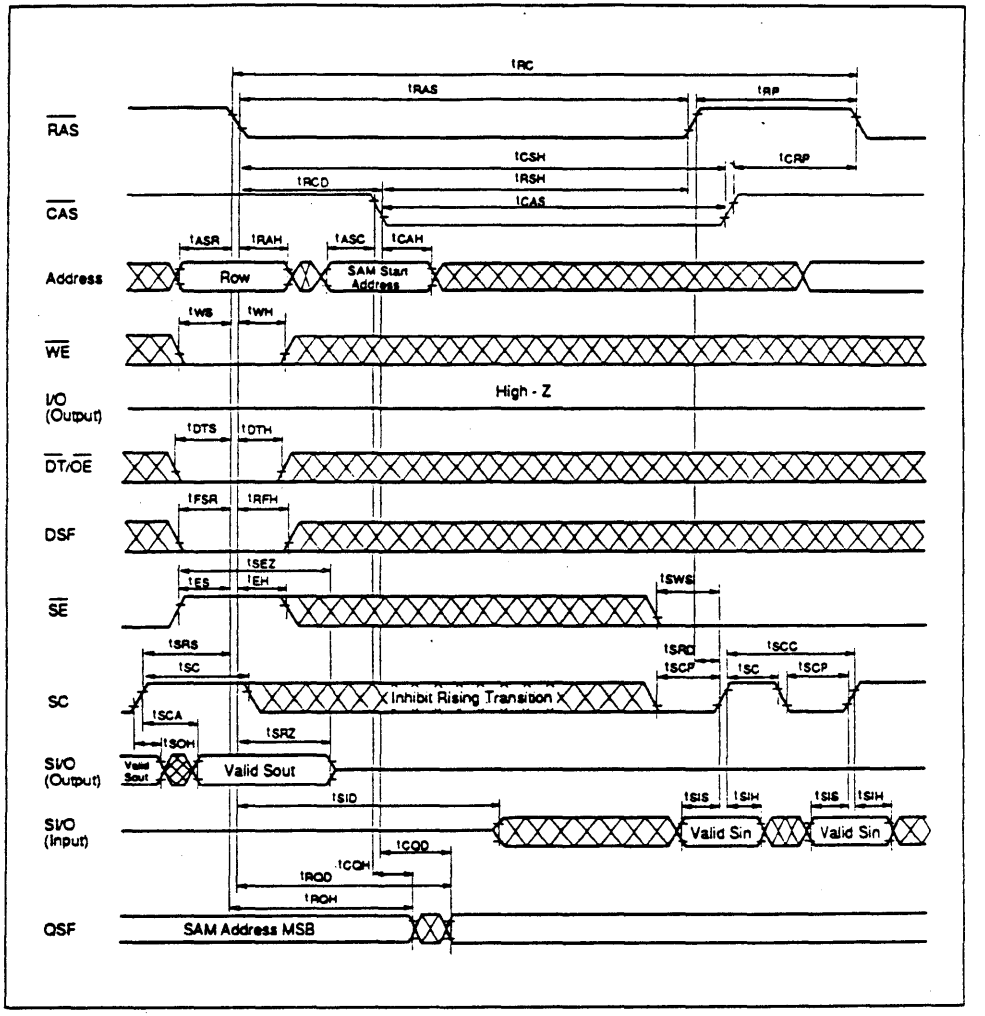


Note: 1. This QSF timing is referred when SC is risen once or more between the previous transfer cycle and $\overline{CAS}$ falling edge of this cycle (QSF is switched by $\overline{DT}$ rising).
2. This QSF timing is referred when SC isn't risen between the previous transfer cycle and $\overline{CAS}$ falling edge of this cycle (QSF is switched by $\overline{RAS}$ or $\overline{CAS}$ falling).

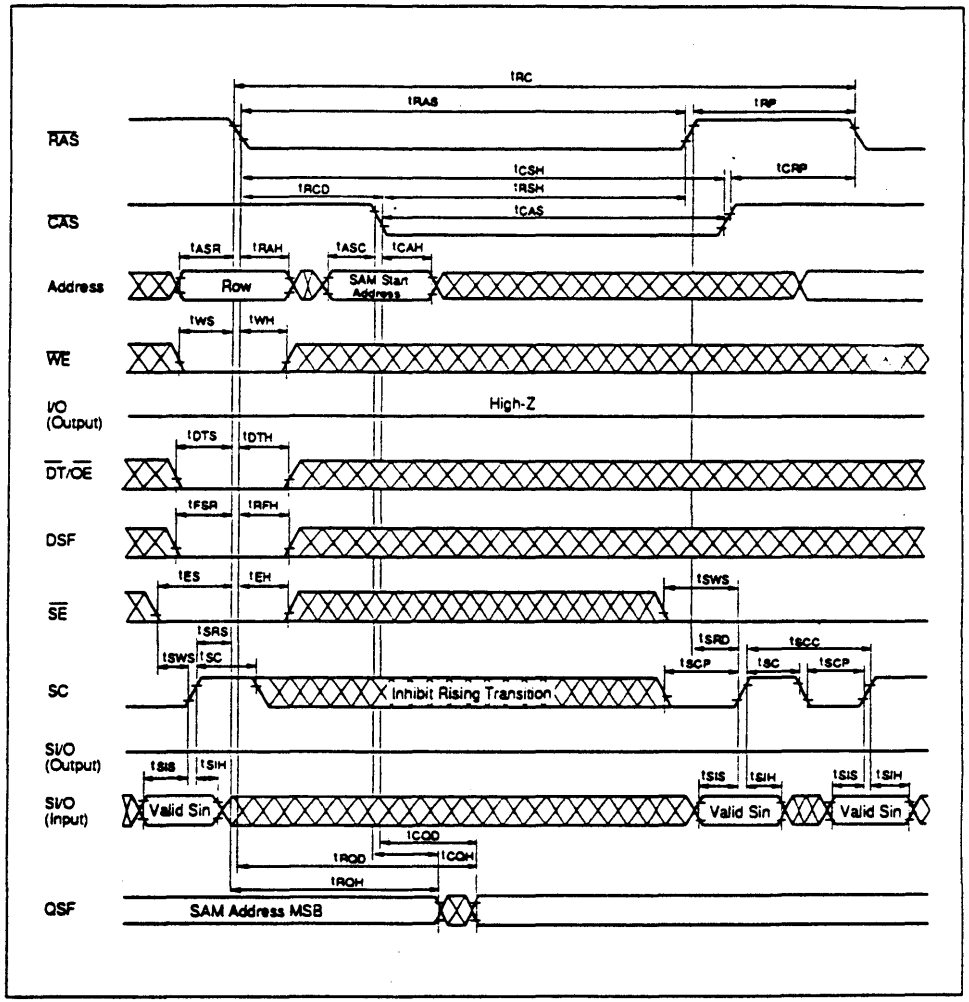
Read Transfer Cycle (2)



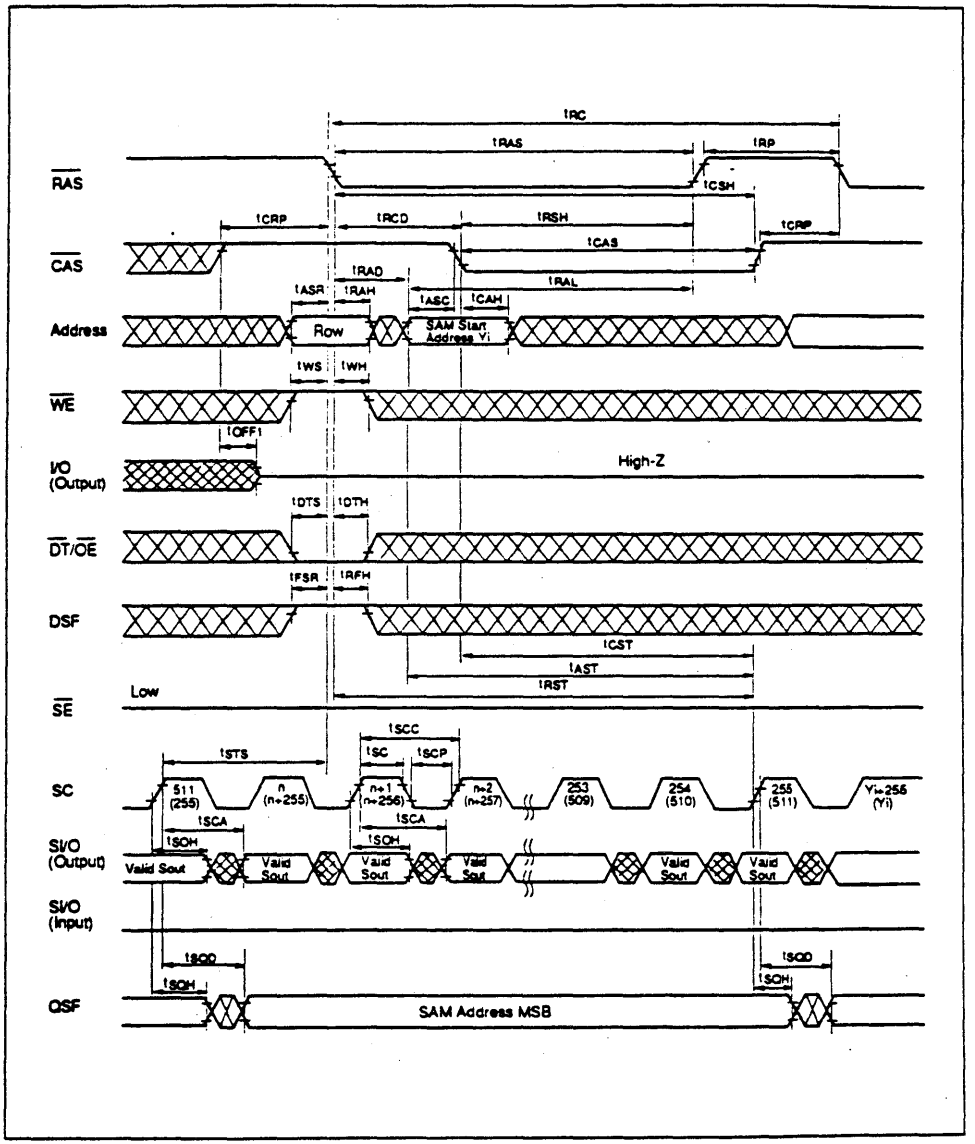
Pseudo Transfer Cycle



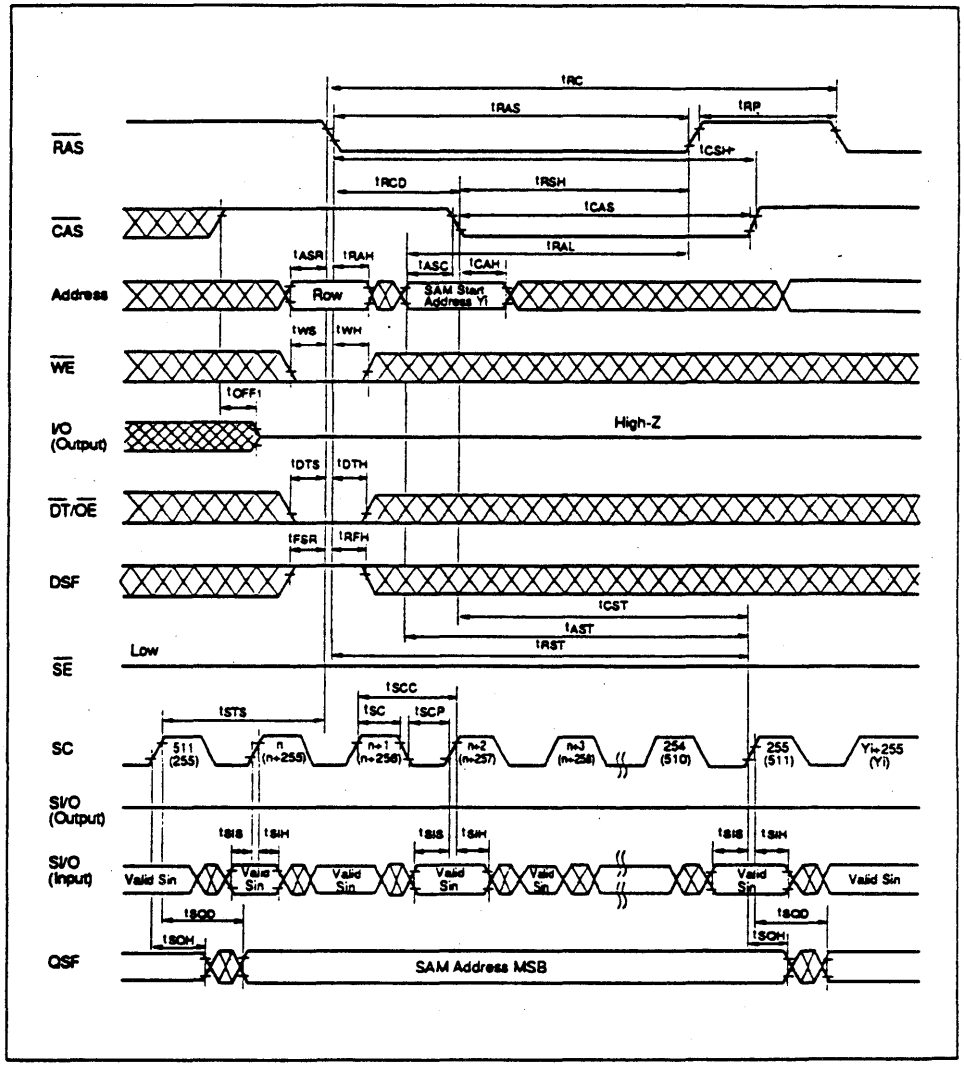
Write Transfer Cycle



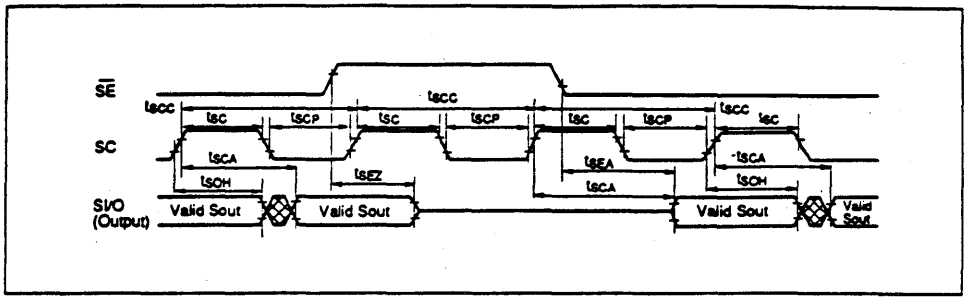
Split Read Transfer Cycle



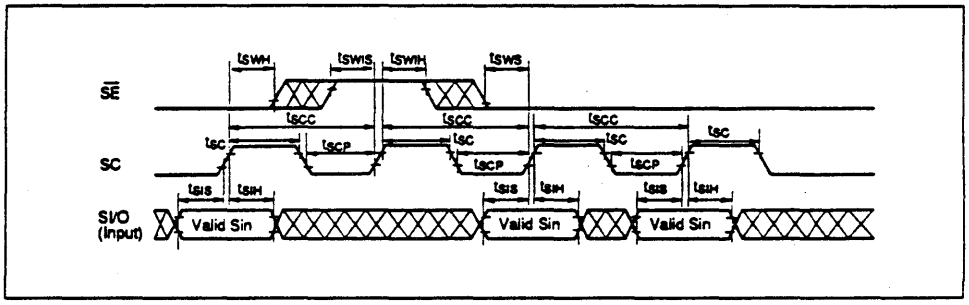
Split Write Transfer Cycle



Serial Read Cycle



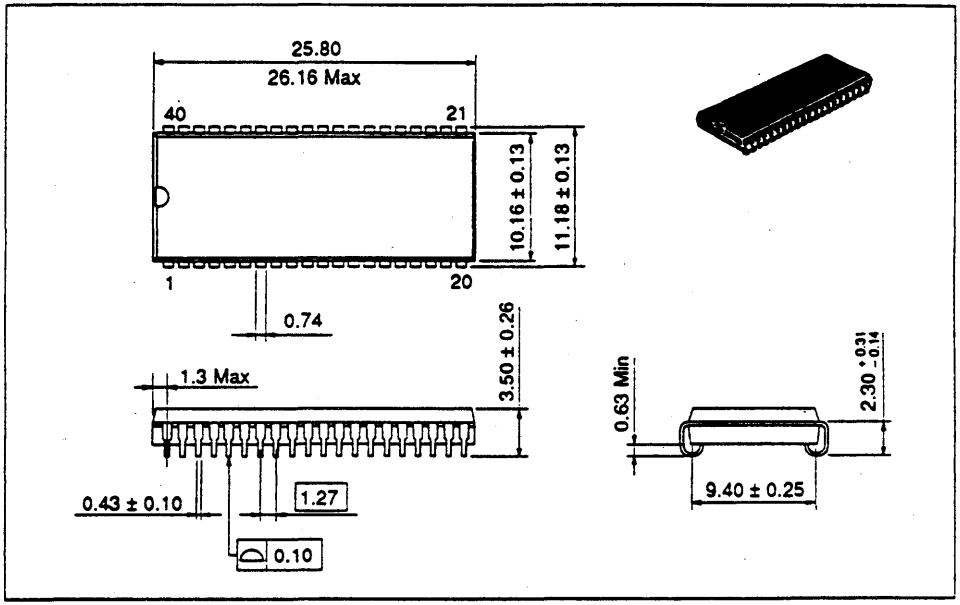
Serial Write Cycle



Package Dimensions

Unit: mm

HM538123BJ Series (CP-40D)



HM538253 Series

262,144-Word x 8-Bit Multiport CMOS Video RAM

HITACHI

Rev. 5
Jul. 20, 1993

The HM538253 is a 2-Mbit multiport video RAM equipped with a 256-kword x 8-bit dynamic RAM and a 512-word x 8-bit SAM (full-sized SAM). Its RAM and SAM operate independently and asynchronously. The HM538253 has basically upward-compatibility with the HM534253A / HM538123A except that pseudo-write-transfer cycle is replaced with masked-write-transfer cycle, which has been approved by JEDEC. Furthermore, several new features are added to the HM538253 without conflict with the conventional features. Stopping column feature realizes much flexibility to the length of split SAM register. Persistent mask is also installed according to the TMS34020 features.

Features

- Multiport organization
  - Asynchronous and simultaneous operation of RAM and SAM capability
  - RAM: 256 kword x 8 bit
  - SAM: 512 word x 8 bit
- Access time
  - RAM: 70 ns/80 ns/100 ns (max)
  - SAM: 20 ns/23 ns/25 ns (max)
- Cycle time
  - RAM: 130 ns/150 ns/180 ns (min)
  - SAM: 25 ns/28 ns/30 ns (min)
- Low power
  - Active RAM: 605 mW/550 mW/495mW
  - SAM: 358 mW/330 mW/303 mW
  - Standby 38.5 mW (max)
- Masked-write-transfer cycle capability
- Stopping column feature capability
- Persistent mask capability
- Fast page mode capability
  - Cycle time: 45 ns/50 ns/55 ns
  - Power RAM: 605 mW/578 mW/550 mW
- Mask write mode capability
- Bidirectional data transfer cycle between RAM and SAM capability
- Split transfer cycle capability
- Block write mode capability
- Flash write mode capability
- 3 variations of refresh (8 ms/512 cycles)
  - $\overline{\text{RAS}}$-only refresh
  - $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - Hidden refresh
- TTL compatible

Ordering Information

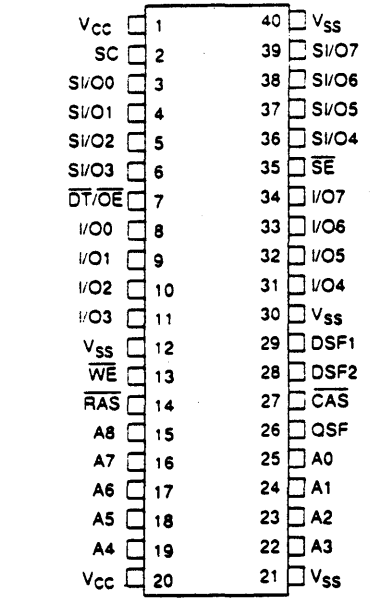
Type No.	Access time	Package
HM538253J-7	70 ns	400 mil 40-pin plastic SOJ (CP-40D)
HM538253J-8	80 ns	
HM538253J-10	100 ns	
HM538253TT-7	70 ns	44-pin thin small outline package (TTP-40DA)
HM538253TT-8	80 ns	
HM538253TT-10	100 ns	
HM538253RR-7	70 ns	44-pin thin small outline package (TTP-40DAR)
HM538253RR-8	80 ns	
HM538253RR-10	100 ns	

Hitachi semiconductor

93.09.02
ADE-203-113E(Z)

Pin Arrangement

HM538253J Series

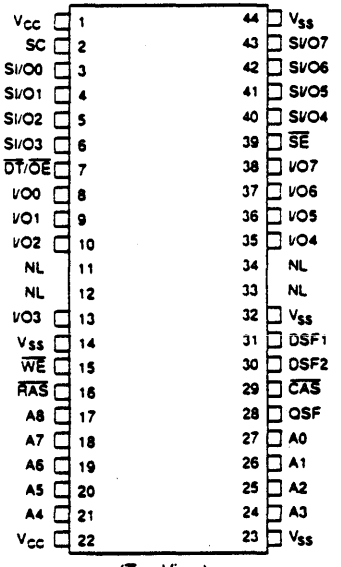


(Top View)

Pin Description

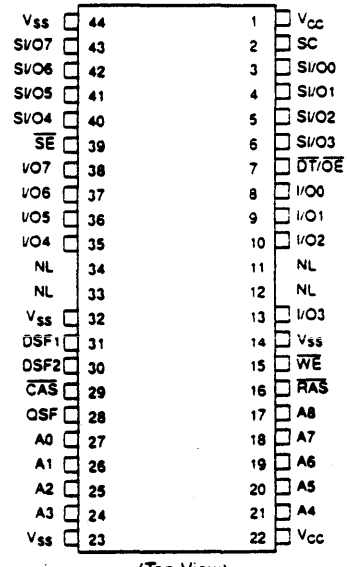
Pin name	Function
A0 – A8	Address inputs
I/O0 – I/O7	RAM port data inputs/outputs
SI/O0 – SI/O7	SAM port data inputs/outputs
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
$\overline{DT/OE}$	Data transfer/output enable
SC	Serial clock
$\overline{SE}$	SAM port enable
DSF1, DSF2	Special function input flag
QSF	Special function output flag
V_{CC}	Power supply
V_{SS}	Ground
NL	No lead

HM538253TT Series



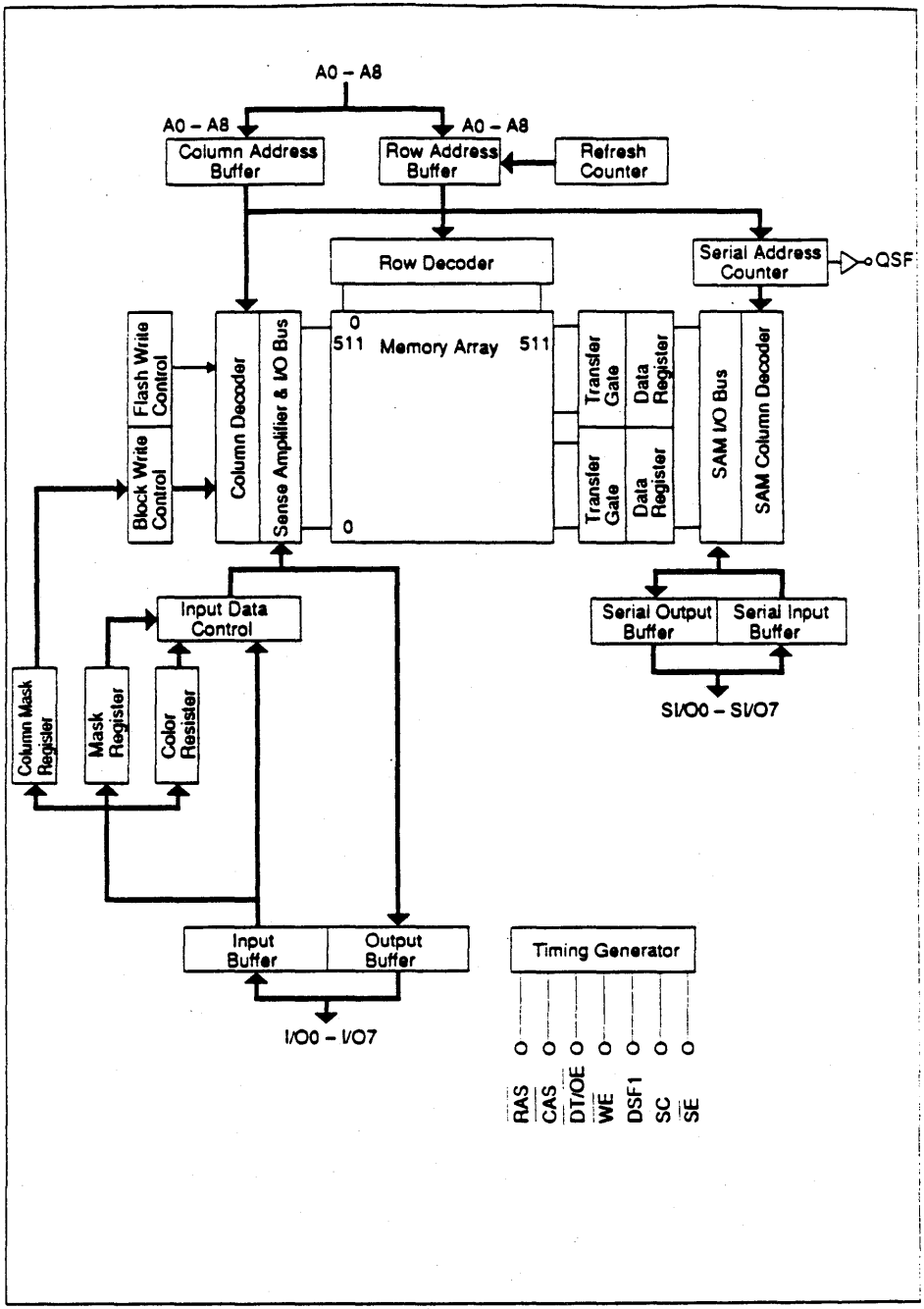
(Top View)

HM538253RR Series



(Top View)

Block Diagram



Pin Functions

$\overline{RAS}$ (input pin): $\overline{RAS}$ is a basic RAM signal. It is active in low level and standby in high level. Row address and signals as shown in table 1 are input at the falling edge of $\overline{RAS}$. The input level of these signals determine the operation cycle of the HM538253.

Table 1. Operation Cycles of the HM538253

Mnemonic Code	$\overline{RAS}$					$\overline{CAS}$		Address		I/On Input	
	$\overline{CAS}$	DT/$\overline{OE}$	$\overline{WE}$	DSF1	DSF2	DSF1	DSF2	$\overline{RAS}$	$\overline{CAS}$	$\overline{RAS}$	$\overline{CAS}$/$\overline{WE}$
CBRS	0	–	0	1	0	–	0	Stop	–	–	–
CBRR	0	–	1	0	0	–	0	–	–	–	–
CBRN	0	–	1	1	0	–	0	–	–	–	–
MWT	1	0	0	0	0	–	0	Row	TAP	WM	–
MSWT	1	0	0	1	0	–	0	Row	TAP	WM	–
RT	1	0	1	0	0	–	0	Row	TAP	–	–
SRT	1	0	1	1	0	–	0	Row	TAP	–	–
RWM	1	1	0	0	0	0	0	Row	Column	WM	Input data

Mnemonic Code	Write Mask	Pers W.M.	Register		No.of Bndry	Function
			WM	Color		
CBRS	–	–	–	–	Set	CBR refresh with stop resister set
CBRR	–	Reset	Reset	–	Reset	CBR refresh with register reset
CBRN	–	–	–	–	–	CBR refresh (no reset)
MWT	Yes	No Yes	Load/use Use	–	–	Masked write transfer (new/old mask)
MSWT	Yes	No Yes	Load/use Use	–	Use	Masked split write transfer (new/old mask)
RT	–	–	–	–	–	Read transfer
SRT	–	–	–	–	Use	Split read transfer
RWM	Yes	No Yes	Load/use Use	–	–	Read/write (new/old mask)

Table 1. Operation Cycles of the HM538253 (cont)

Mnemonic	$\overline{RAS}$					$\overline{CAS}$		Address		I/On Input	
Code	$\overline{CAS}$	DT/$\overline{OE}$	$\overline{WE}$	DSF1	DSF2	DSF1	DSF2	$\overline{RAS}$	$\overline{CAS}$	$\overline{RAS}$	$\overline{CAS}$/$\overline{WE}$
BWM	1	1	0	0	0	1	0	Row	Column	WM	Column Mask
RW (No)	1	1	1	0	0	0	0	Row	Column	–	Input Data
BW (No)	1	1	1	0	0	1	0	Row	Column	–	Column Mask
FWM	1	1	0	1	0	–	0	Row	–	WM	–
LMR and Old Mask Set	1	1	1	1	0	0	0	(Row)	–	–	Mask Data
LCR	1	1	1	1	0	1	0	(Row)	–	–	Color
Option	0	0	0	0	0	–	0	Mode	–	Data	–

Mnemonic Code	Write Mask	Pers W.M.	Register WM	Register Color	No.of Bndry	Function
BWM	Yes	No Yes	Load/use Use	Use	–	Block write (new/old mask)
RW (No)	No	No	–	–	–	Read/write (no mask)
BW (No)	No	No	–	Use	–	Block write (no mask)
FWM	Yes	No Yes	Load/use Use	Use	–	Masked flash write (new/old mask)
LMR and Old Mask Set	–	Set	Load	–	–	Load mask register and old mask set
LCR	–	–	–	Load	–	Load color resister set
Option	–	–	–	–	–	–

Notes: 1. With CBRS, all SAM operations use stop register.
2. After LMR, RWM, BWM, FWM, MWT, and MSWT, use old mask which can be reset by CBRR.
3. DSF2 is fixed low in all operation. (for the addition of operation mode in future)

$\overline{CAS}$ (input pin): Column address and DSF1 signals are fetched into chip at the falling edge of $\overline{CAS}$, which determines the operation mode of the HM538253. $\overline{CAS}$ controls output impedance of I/O in RAM.

A0 – A8 (input pins): Row address (AX0 – AX8) is determined by A0 – A8 level at the falling edge of $\overline{RAS}$. Column address (AY0 – AY8) is determined by A0 – A8 level at the falling edge of $\overline{CAS}$. In transfer cycles, row address is the address on the word line which transfers data with SAM data register, and column address is the SAM start address after transfer.

$\overline{WE}$ (input pin): $\overline{WE}$ pin has two functions at the falling edge of $\overline{RAS}$ and after. When $\overline{WE}$ is low at the falling edge of $\overline{RAS}$, the HM538253 turns to mask write mode. According to the I/O level at the time, write on each I/O can be masked. ($\overline{WE}$ level at the falling edge of $\overline{RAS}$ is don't care in read cycle.) When $\overline{WE}$ is high at the falling edge of $\overline{RAS}$, a no mask write cycle is executed. After that, $\overline{WE}$ switches read/write cycles. In a transfer cycle, the direction of transfer is determined by $\overline{WE}$ level at the falling edge of $\overline{RAS}$. When $\overline{WE}$ is low, data is transferred from SAM to RAM (data is written into RAM), and when $\overline{WE}$ is high, data is transferred from RAM to SAM (data is read from RAM).

I/O0 – I/O7 (input/output pins): I/O pins function as mask data at the falling edge of $\overline{RAS}$ (in mask write mode). Data is written only to high I/O pins. Data on low I/O pins are masked and internal data are retained. After that, they function as inut/output pins as those of a standard DRAM. In block write cycle, they function as column mask data at the falling edges of $\overline{CAS}$ and $\overline{WE}$.

$\overline{DT}/\overline{OE}$ (input pin): $\overline{DT}/\overline{OE}$ pin functions as $\overline{DT}$ (data transfer) pin at the falling edge of $\overline{RAS}$ and as $\overline{OE}$ (output enable) pin after that. When $\overline{DT}$ is low at the falling edge of $\overline{RAS}$, this cycle becomes a transfer cycle. When $\overline{DT}$ is high at the falling edge of $\overline{RAS}$, RAM and SAM operate independently.

SC (input pin): SC is a basic SAM clock. In a serial read cycle, data outputs from an SI/O pin synchronously with the rising edge of SC. In a serial write cycle, data on an SI/O pin at the rising edge of SC is fetched into the SAM data register.

$\overline{SE}$ (input pin): $\overline{SE}$ pin activates SAM. When $\overline{SE}$ is high, SI/O is in the high impedance state in serial read cycle and data on SI/O is not fetched into the SAM data register in serial write cycle. $\overline{SE}$ can be used as a mask for serial write because the internal pointer is incremented at the rising edge of SC.

SI/O0 – SI/O7 (input/output pins): SI/Os are input/output pins in SAM. Direction of input/output is determined by the previous transfer cycle. When it was a read transfer cycle, SI/O outputs data. When it was a masked write transfer cycle, SI/O inputs data.

DSF1 (input pin): DSF1 is a special function data input flag pin. It is set to high at the falling edge of $\overline{RAS}$ when new functions such as color register and mask register read/write, split transfer, and flash write, are used.

DSF2 (input pin): DSF2 is also a special function data input flag pin. This pin is fixed to low level in all operations of the HM538253.

QSF (output pin): QSF outputs data of address A8 in SAM. QSF is switched from low to high by accessing address 255 in SAM and from high to low by accessing address 511 address in SAM.

Operation of HM538253

RAM Port Operation

RAM Read Cycle ($\overline{DT/OE}$ high, $\overline{CAS}$ high and DSF1 low at the falling edge of $\overline{RAS}$, DSF1 low at the falling edge of $\overline{CAS}$)

Row address is entered at the $\overline{RAS}$ falling edge and column address at the $\overline{CAS}$ falling edge to the device as in standard DRAM. Then, when $\overline{WE}$ is high and $\overline{DT/OE}$ is low while $\overline{CAS}$ is low, the selected address data outputs through I/O pin. At the falling edge of $\overline{RAS}$, $\overline{DT/OE}$ and $\overline{CAS}$ become high to distinguish RAM read cycle from transfer cycle and CBR refresh cycle. Address access time (t_{AA}) and $\overline{RAS}$ to column address delay time (t_{RAD}) specifications are added to enable fast page mode.

RAM Write Cycle (Eraly Write, Delayed Write, Read-Modify-Write)
($\overline{DT/OE}$ high, $\overline{CAS}$ high and DSF1 low at the falling edge of $\overline{RAS}$, DSF1 low at the falling edge of $\overline{CAS}$)

- No Mask Write Cycle ($\overline{WE}$ high at the falling edge of $\overline{RAS}$)

When $\overline{CAS}$ is set low and $\overline{WE}$ is set low after $\overline{RAS}$ low, a write cycle is executed.
If $\overline{WE}$ is set low before the $\overline{CAS}$ falling edge, this cycle becomes an early write cycle and all I/O become in high impedance.
If $\overline{WE}$ is set low after the $\overline{CAS}$ falling edge, this cycle becomes a delayed write cycle. I/O does not become high impedance in this cycle, so data should be entered with $\overline{OE}$ in high.
If $\overline{WE}$ is set low after t_{CWD} (min) and t_{AWD} (min) after the $\overline{CAS}$ falling edge, this cycle becomes a read-modify-write cycle and enables read/write at the same address in one cycle. In this cycle also, to avoid I/O contention, data should be input after reading data and driving $\overline{OE}$ high.

- Mask Write Mode ($\overline{WE}$ low at the falling edge of $\overline{RAS}$)

If $\overline{WE}$ is set low at the falling edge of $\overline{RAS}$, two modes of mask write cycle are capable.
1. In new mask mode, mask data is loaded from I/O pin and used. Whether or not an I/O is written depends on I/O level at the falling edge of $\overline{RAS}$. The data is written in high level I/Os, and the data is masked and retained in low level I/Os. This mask data is effective during the $\overline{RAS}$ cycle. So, in page mode cycles the mask data is retained during the page access.
2. If a load mask register cycle (LMR) has been performed, the mask data is not loaded from I/O pins and the mask data stored in mask registers persistently are used. This operation is known as persistent write mask, set by LMR cycle and reset by CBRR cycle.

Fast Page Mode Cycle ($\overline{DT/OE}$ high, $\overline{CAS}$ high and DSF1 low at the falling edge of $\overline{RAS}$)

Fast page mode cycle reads/writes the data of the same row address at high speed by toggling $\overline{CAS}$ while $\overline{RAS}$ is low. Its cycle time is one third of the random read/write cycle. In this cycle, read, write, and block write cycles can be mixed. Note that address access time (t_{AA}), $\overline{RAS}$ to column address delay time (t_{RAD}), and access time from $\overline{CAS}$ precharge (t_{ACP}) are added. In one $\overline{RAS}$ cycle, 512-word memory cells of the same row address can be accessed. It is necessary to specify access frequency within t_{RASP} max (100 μs).

Color Register Set/Read Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ high, $\overline{WE}$ high and DSF1 high at the falling edge of $\overline{RAS}$)

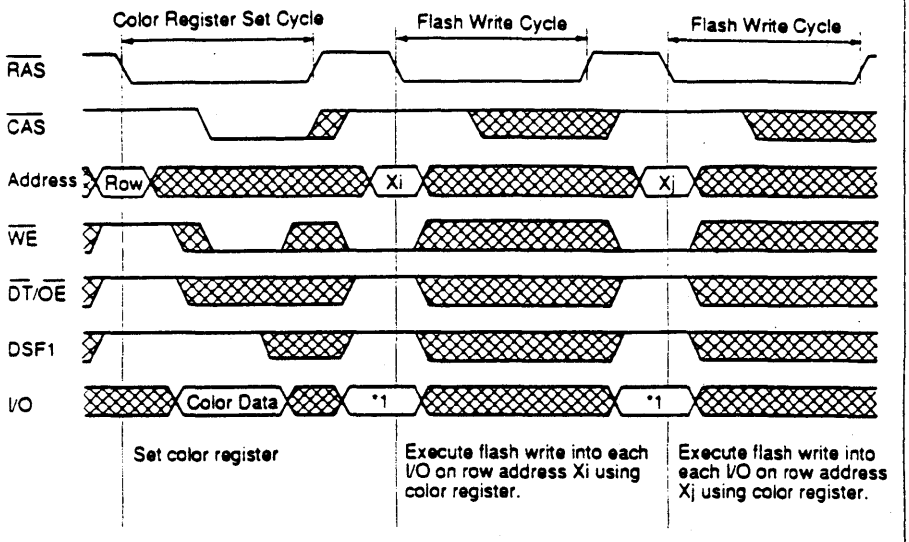
In color register set cycle, color data is set to the internal color register used in flash write cycle or block write cycle. 8 bits of internal color register are provided at each I/O. This register is composed of static circuits, so once it is set, it retains the data until reset. Since color register set cycle is just as same as the usual read and write cycle, so read, early write and delayed write cycle can be executed. In this cycle, the HM538253 refreshes the row address fetched at the falling edge of $\overline{RAS}$.

Mask Register Set/Read Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ high, $\overline{WE}$ high, and DSF1 high at the falling edge of $\overline{RAS}$)

In mask register set cycle, mask data is set to the internal mask register used in mask write cycle, block write cycle, flash write cycle, masked write transfer, and masked split write transfer. 8 bits of internal mask register are provided at each I/O. This mask register is composed of static circuits, so once it is set, it retains the data until next mask register set or reset (CBRR). Since mask register set cycle is just as same as the usual read and write cycle, so read, early write and delayed write cycle can be executed.

Flash Write Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ high, $\overline{WE}$ low, and DSF1 high at the falling edge of $\overline{RAS}$)

In a flash write cycle, a row of data (512 word x 8 bit) is cleared to 0 or 1 at each I/O according to the data of color register mentioned before. It is also necessary to mask I/O in this cycle. When $\overline{CAS}$ and $\overline{DT/OE}$ is set high, $\overline{WE}$ is low, and DSF1 is high at the falling edge of $\overline{RAS}$, this cycle starts. Then, the row address to clear is given to row address. Mask data is as same as that of a RAM write cycle. Cycle time is the same as those of RAM read/write cycles, so all bits can be cleared in 1/512 of the usual cycle time. (See figure 1.)



*1 I/O Mask Data (In new mask mode)
Low: Mask
High: Non Mask
In persistent mask mode, I/O don't care

Figure 1 Use of Flash Write

Block Write Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ high and DSF1 low at the falling edge of $\overline{RAS}$, DSF1 high and $\overline{WE}$ low at the falling edge of $\overline{CAS}$)

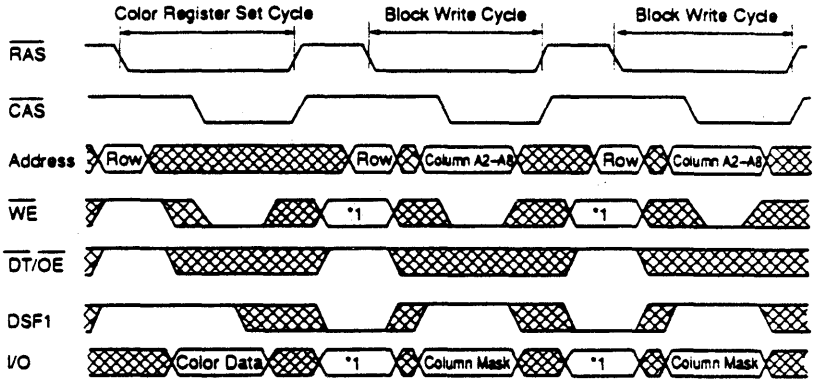
In a block write cycle, 4 columns of data (4 column x 8 bit) are cleared to 0 or 1 at each I/O according to the data of color register. Column addresses A0 and A1 are disregarded. The mask data on I/Os and the mask data on column address can be determined independently. I/O level at the falling edge of $\overline{CAS}$ determines the address to be cleared. (See Figure 2.) The block write cycle is as the same as the usual write cycle, so early and delayed write, read-modify-write, and page mode write cycle can be executed.

- No mask Mode Block Write Cycle ($\overline{WE}$ high at the falling edge of $\overline{RAS}$)

The data on 8 I/Os are all cleared when $\overline{WE}$ is high at the falling edge of $\overline{RAS}$.

- Mask Block Write Cycle ($\overline{WE}$ low at the falling edge of $\overline{RAS}$)

When $\overline{WE}$ is low at the falling edge of $\overline{RAS}$, the HM538253 starts mask block write cycle to clear the data on an optional I/O. The mask data is the same as that of a RAM write cycle. High I/O is cleared, low I/O is not cleared and the internal data is retained. In new mask mode, the mask data is available in the $\overline{RAS}$ cycle. In persistent mask mode, I/O don't care about mask mode.



*1

$\overline{WE}$	Mode	I/O data/$\overline{RAS}$
Low	New Mask Mode	Mask
	Persistent Mask Mode	Don't care (mask register used)
High	No mask	Don't care

I/O Mask Data (In new mask mode)
Low: Mask
High: Non Mask
In persistent mask mode, I/O don't care

Column Mask Data

I/O0	Column0 (A0 = 0, A1 = 0) Mask Data	Low: Mask
I/O1	Column1 (A0 = 1, A1 = 0) Mask Data	
I/O2	Column2 (A0 = 0, A1 = 1) Mask Data	
I/O3	Column3 (A0 = 1, A1 = 1) Mask Data	High: Non Mask

Figure 2 Use of Block Write

Transfer Operation

The HM538253 provides the read transfer cycle, split read transfer cycle, masked write transfer cycle and masked split write transfer cycle as data transfer cycles. Theses transfer cycles are set by driving $\overline{CAS}$ high and $\overline{DT/OE}$ low at the falling edge of $\overline{RAS}$. They have following functions:
(1) Transfer data between row address and SAM data register
Read transfer cycle and split read transfer cycle: RAM to SAM
Masked write transfer cycle and masked split write transfer cycle: SAM to RAM
(2) Determine SI/O state (except for split read transfer cycle and masked split write transfer cycle)
Read transfer cycle: SI/O output
Masked write transfer cycle: SI/O input
(3) Determine first SAM address to access after transferring at column address (SAM start address).
SAM start address must be determined by read transfer cycle or masked write transfer cycle (split transfer cycle isn't available)before SAM access, after power on, and determined for each transfer cycle.
(4) Use the stopping columns (boundaries) in the serail shift register. If the stopping columns have been set, split transfer cycles use the stopping columns, but any boundaries cannot be set as the start address.
(5) Load/use mask data in masked write transfer cycle and masked split write transfer cycle.

Read Transfer Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ low, $\overline{WE}$ high and DSF1 low at the falling edge of $\overline{RAS}$)

This cycle becomes read transfer cycle by driving $\overline{DT/OE}$ low, $\overline{WE}$ high and DSF1 low at the falling edge of $\overline{RAS}$. The row address data (512 x 8 bits) determined by this cycle is transferred to SAM data register synchronously at the rising edge of $\overline{DT/OE}$. After the rising edge of $\overline{DT/OE}$, the new address data outputs from SAM start address determined by column address. In read transfer cycle, $\overline{DT/OE}$ must be risen to transfer data from RAM to SAM.
This cycle can access SAM even during transfer (real time read transfer). In this case, the timing t_{SDD} (min) specified between the last SAM access before transfer and $\overline{DT/OE}$ rising edge and t_{SDH} (min) specified between the first SAM access and $\overline{DT/OE}$ rising edge must be satisfied. (See figure 3.)
When read transfer cycle is executed, SI/O becomes output state by first SAM access. Input must be set high impedance before t_{SZS} (min) of the first SAM access to avoid data contention.

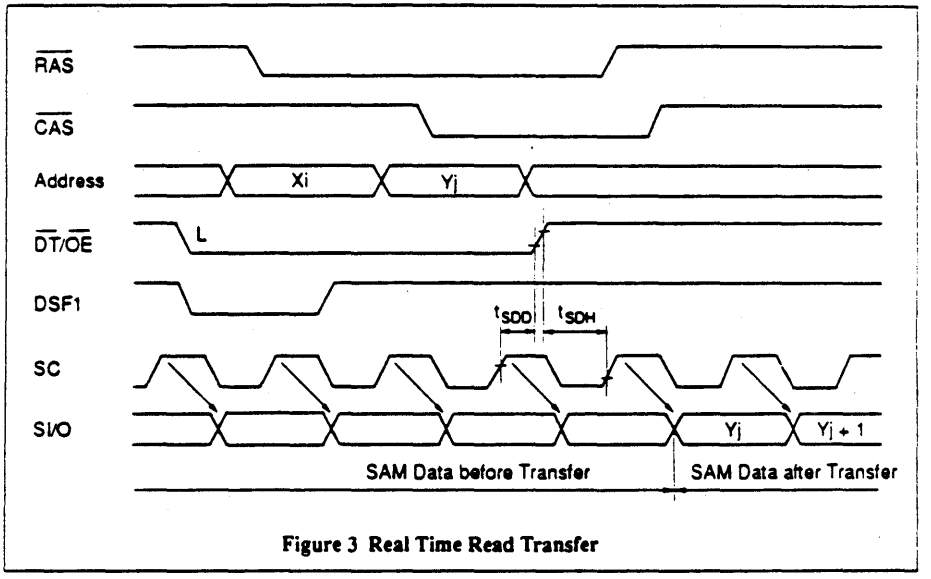


Figure 3 Real Time Read Transfer

Masked Write Transfer cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ low, $\overline{WE}$ low, and DSF1 low at the falling edge of $\overline{RAS}$)

Masked write transfer cycle can transfer only selected I/O data in a row of data input by serial write cycle to RAM. Whether SAM data is transferred or not depends on the corresponding I/O level (mask data) at the falling edge of $\overline{RAS}$. This mask transfer operation is the same as a mask write operation in RAM cycles, so the persistent mode can be supported. The row address of data transferred into RAM is determined by the address at the falling edge of $\overline{RAS}$. The column address is specified as the first address for serial write after terminating this cycle. Also in this cycle, SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. SAM access is inhibited during $\overline{RAS}$ low. In this period, SC must bot be risen. Data transferred to SAM by read transfer cycle or split read transfer cycle can be written to other addreses of RAM by write transfer cycle. However, the adddress to write data must be the same as that of the read transfer cycle or the split read transfer cycle (row address AX8)

Split Read Transfer Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ low, $\overline{WE}$ high and DSF1 high at the falling edge of $\overline{RAS}$)

To execute a continuous serial read by real time read transfer, the HM538253 must satisfy SC and $\overline{DT/OE}$ timings and requires an external circuit to detect SAM last address. Split read transfer cycle makes it possible to execute a continuous serial read without the above timing limitation.
The HM538253 supports two types of split register operation. One is the normal split register operation to split the data register into two halves. The other is the boundary split register operation using stopping columns described later.
Figure 4 shows the block diagram for the normal split register operation. SAM data register (DR) consists of 2 split buffers, whose organizations are 256-word x 8-bit each. Let us suppose that data is read from upper data reagister DR1 (The row address AX8 is 0 and SAM address A8 is 1.). When split read transfer is executed setting row address AX8 0 and SAM start addresses A0 to A7, 256-word x 8-bit data are transferred from RAM to the lower data register DR0 (SAM address A8 is 0) automatically. After data are read from data register DR1, data start to be read from SAM start addresses of data register DR0. If the next split read transfer isn't executed while data are read from data register DR0, data start to be read from SAM start address 0 of DR1 after data are read from data register DR0. If split read transfer is executed setting row address AX8 1 and SAM start addresses A0 to A7 while data are read from data register DR1, 256-word x 8-bit data are transferred to data register DR2. After data are read from data register DR1, data start to be read from SAM start addresses of data register DR2. If the next split read transfer isn't executed while data is read from data register DR2, data start to be read from SAM start address 0 of data register DR1 after data are read from data register DR2. In split read data transfer, the SAM start address A8 is automatically set in the data register, which isn't used.
The data on SAM address A8, which will be accessed next, outputs to QSF, QSF is switched from low to high by accessing SAM last address 255 and from high to low by accessing address 511.
Split read transfer cycle is set when $\overline{CAS}$ is high, $\overline{DT/OE}$ is low, $\overline{WE}$ is high and DSF1 is high at the falling edge of $\overline{RAS}$. The cycle can be executed asyncronously with SC. However, HM538253 must be satisfied tSTS (min) timing specified between SC rising (Boundary address) and $\overline{RAS}$ falling. In split transfer cycle, the HM538253 must satisfy t_{RST} (min), t_{CST} (min) and t_{AST} (min) timings specified between $\overline{RAS}$ or $\overline{CAS}$ falling and column address. (See figure 5.)
In split read transfer, SI/O isn't switched to output state. Therefore, read transfer must be executed to switch SI/O to output state when the previous transfer cycle is masked write transfer cycle or masked split write transfer cycle, or power on. SAM start address must be set in every split read transfer cycle.

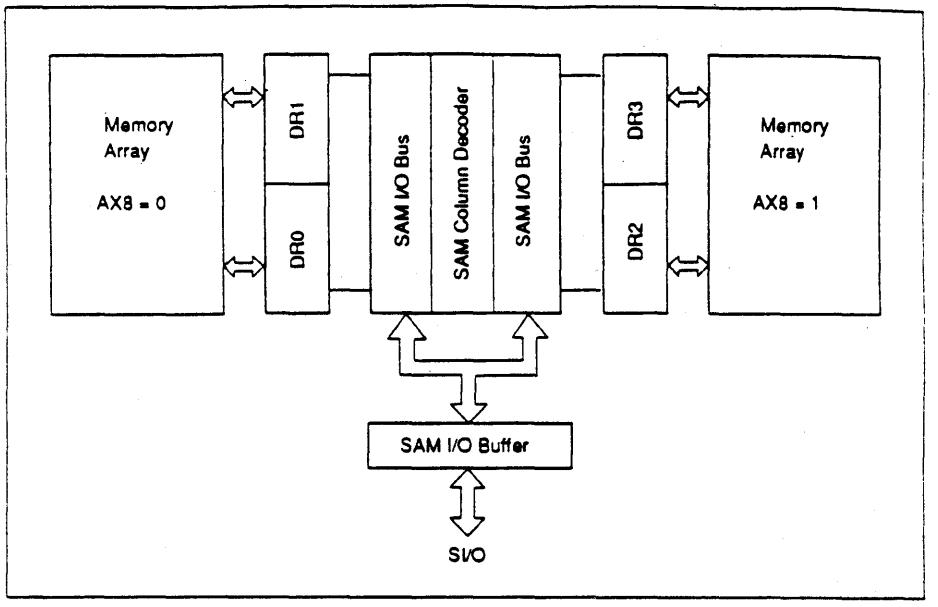


Figure 4 Block Diagram for Split Transfer

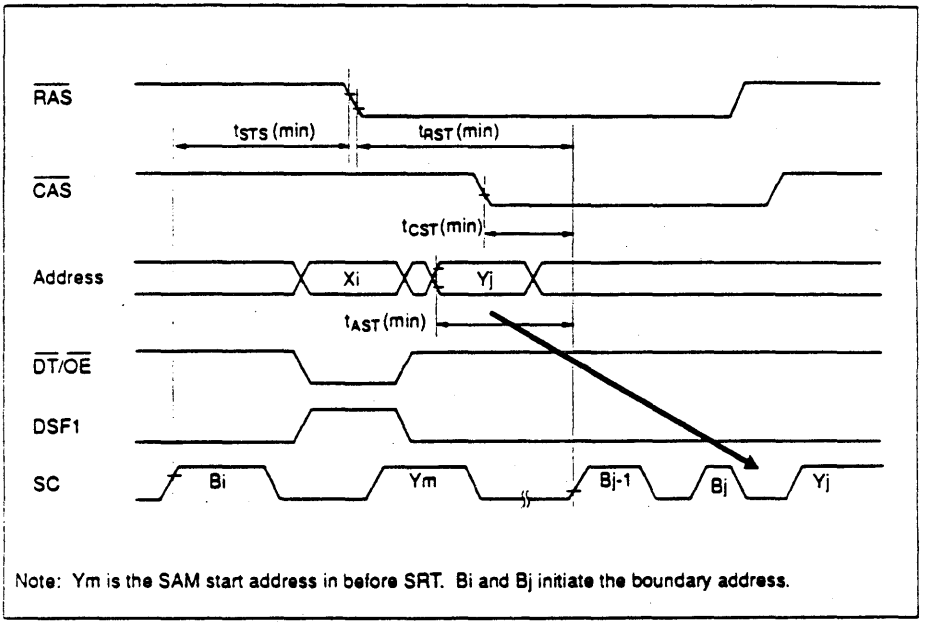


Figure 5 Limitation in Split Transfer

Masked Split Write Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low and DSF1 high at the falling edge of $\overline{RAS}$)

A continuous serial write cannot be executed because accessing SAM is inhibited during $\overline{RAS}$ low in write transfer. Masked split write transfer cycle makes it possible. In this cycle, t_{STS} (min), t_{RST} (min), t_{CST} (min) and t_{AST} (min) timings must be satisfied like split read transfer cycle. And it is impossible to switch SI/O to input state in this cycle. If SI/O is in output state, masked write transfer cycle should be executed to switch SI/O into input state. Data transferred to SAM by read transfer cycle or split read transfer cycle can be written to other addresses of RAM by masked split write transfer cycle. However masked write transfer cycle must be executed before masked split write transfer cycle. And in this masked split write transfer cycle, the MSB of row address (AX8) to write data must be the same as that of the read transfer cycle or the split read transfer cycle. In this cycle, the boundary split register operation using stopping columns is capable like split read transfer cycle.

Stopping Column in Split Transfer Cycle

The HM538253 has the boundary split register operation using stopping columns. If a CBRS cycle has been performed, split transfer cycle performs the boundary operation. Figure 6 shows an example of boundary split register. (Boundary code is B7.)
First of all a read transfer cycle is executed, and SAM start addresses A0 to A8 are set. The RAM data are transferred to the SAM, and SAM serial read starts from the start address (Y1) on the lower SAM. After that, a split read transfer cycle is executed, and the next start address (Y2) is set. The RAM data are transferred to the upper SAM. When the serial read arrive at the first boundary after the split read transfer cycle, the next read jumps to the start address (Y2) on the upper SAM (jump 1) and continues. Then the second split read transfer cycle is executed, and another start address (Y3) is set. The RAM data are transferred to the lower SAM. When the serial read arrive at the other boundary again, the next read jumps to the start address (Y3) on the lower SAM. In stopping column, split transfer is needed for jump operation between lower SAM and upper SAM.

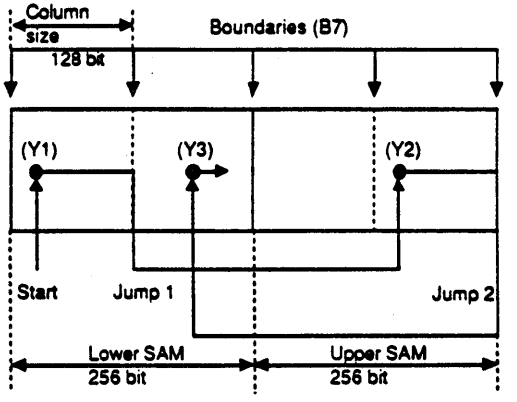


Figure 6 Example of Boundary Split Register

Stopping Column Set Cycle (CBRS)

This cycle becomes stopping column set cycle by driving $\overline{CAS}$ low, $\overline{WE}$ low, DSF1 high at the falling edge of $\overline{RAS}$. Stopping column data (boundaries) are latched from address inputs on the falling edge of $\overline{RAS}$. To determine the boundary, A2 to A7 can be used and don't care A0, A1, and A8. In the HM538253, 7 types of boundary (B2 to B8) can be set including the default case. (See stopping column boundary table.) If A2 to A6 are set to high and A7 is set to low, the boundaries (B7) are selected. Figure 6 shows the example. The stop address that is set by the CBRS is used from next split transfer cycle. Once a CBRS is executed, the stopping column operation mode continues until CBRR.

Stopping Column Boundary Table

		Stop Address					
Boundary code	Column size	A2	A3	A4	A5	A6	A7
B2	4	0	•	•	•	•	•
B3	8	1	0	•	•	•	•
B4	16	1	1	0	•	•	•
B5	32	1	1	1	0	•	•
B6	64	1	1	1	1	0	•
B7	128	1	1	1	1	1	0
B8	256	1	1	1	1	1	1

Notes: 1.A0, A1, and A8: don't care
2.•: don't care

Register Reset Cycle (CBRR)

This cycle becomes register reset cycle (CBRR) by driving $\overline{CAS}$ low, $\overline{WE}$ high, and DSF1 low at the falling edge of $\overline{RAS}$. A CBRR can reset the persistent mask operation and stopping column operation, so the HM538253 becomes the new mask operation and boundary code B8. When a CBRR is executed for stopping column operation reset and split transfer operation, it needs to satisfy t_{STS} (min) and t_{RST} (min) between $\overline{RAS}$ falling and SC rising for correct SAM read/write operation.

No Reset CBR Cycle (CBRN)

This cycle becomes no reset CBR cycle (CBRN) by driving $\overline{CAS}$ low, $\overline{WE}$ high and DSF1 high at the falling edge of $\overline{RAS}$. The CBRN can only execute the refresh operation.

SAM Port Operation

Serial Read Cycle

SAM port is in read mode when the previous data transfer cycle is a read transfer cycle. Access is synchronized with SC rising, and SAM data is output from SI/O. When $\overline{SE}$ is set high, SI/O becomes high impedance, and the internal pointer is incremented by the SC rising. After indicating the last address (address 511), the internal pointer indicates address 0 at the next access.

Serial Write Cycle

If previous data transfer cycle is masked write transfer cycle, SAM port goes into write mode. In this cycle, SI/O data is fetched into data register at the SC rising edge like in the serial read cycle. If $\overline{SE}$ is high, SI/O data isn't fetched into data register. The internal pointer is incremented by the SC rising, so $\overline{SE}$ high can be used as mask data for SAM. After indicating the last address (address 511), the internal pointer indicates address 0 at the next access.

Refresh

RAM Refresh

RAM, which is composed of dynamic circuits, requires refresh cycle to retain data. Refresh is executed by accessing all 512 row addresses within 8 ms. There are three refresh cycles: (1) $\overline{RAS}$-only refresh cycle, (2) $\overline{CAS}$-before-$\overline{RAS}$ (CBRN, CBRS, and CBRR) refresh cycle, and (3) Hidden refresh cycle. Besides them, the cycles which activate $\overline{RAS}$, such as read/write cycles or transfer cycles, can also refresh the row address. Therefore, no refresh cycle is required when all row addresses are accessed within 8 ms.

(1) $\overline{RAS}$-Only Refresh Cycle: $\overline{RAS}$-only refresh cycle is executed by activating only the $\overline{RAS}$ cycle with $\overline{CAS}$ fixed to high after inputting the row address (= refresh address) from external circuits. To distinguish this cycle from a data transfer cycle, $\overline{DT}/\overline{OE}$ must be high at the falling edge of $\overline{RAS}$.

(2) CBR Refresh Cycle: CBR refresh cycle (CBRN, CBRS and CBRR) are set by activating $\overline{CAS}$ before $\overline{RAS}$. In this cycle, the refresh address need not to be input through external circuits because it is input through an internal refresh counter. In this cycle, output is in high impedance and power dissipation is lowered because $\overline{CAS}$ circuits don't operate.

(3) Hidden Refresh Cycle: Hidden refresh cycle executes CBR refresh with the data output by reactivating $\overline{RAS}$ when $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ keep low in normal RAM read cycles. In the mask register read cycle and the color register read cycle, Dout data guaranteed while $\overline{RAS}$ and $\overline{CAS}$ are low, and so after the mask register read cycle or the color register read cycle is performed, in hidden refresh cycle Dout data is not guaranteed.

SAM Refresh

SAM parts (data register, shift resister and selector), organized as fully static circuitry, require no refresh.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	−0.5 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{CC}	4.5	5.0	5.5	V	1
Input high voltage	V_{IH}	2.4	—	6.5	V	1
Input low voltage	V_{IL}	−0.5*2	—	0.8	V	1

Notes: 1. All voltage referenced to V_{SS}
2 −3.0 V for pulse width ≤ 10 ns.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Parameter	Symbol	HM538253-7 Min	HM538253-7 Max	HM538253-8 Min	HM538253-8 Max	HM538253-10 Min	HM538253-10 Max	Unit	Test conditions
Operating current	I_{CC1}	—	110	—	100	—	90	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min; SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC7}	—	165	—	150	—	140	mA	$\overline{SE}$ = V_{IL}, SC cycling, t_{SCC} = min
Block write current	I_{CC1BW}	—	115	—	105	—	90	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min; SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC7BW}	—	170	—	155	—	140	mA	$\overline{SE}$ = V_{IL}, SC cycling, t_{SCC} = min
Standby current	I_{CC2}	—	7	—	7	—	7	mA	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}; SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC8}	—	65	—	60	—	55	mA	$\overline{SE}$ = V_{IL}, SC cycling, t_{SCC} = min
$\overline{RAS}$-only refresh current	I_{CC3}	—	110	—	100	—	90	mA	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = min; SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC9}	—	165	—	150	—	135	mA	$\overline{SE}$ = V_{IL}, SC cycling, t_{SCC} = min
Fast page mode current *3	I_{CC4}	—	110	—	105	—	100	mA	$\overline{CAS}$ cycling, $\overline{RAS}$ = V_{IL}; t_{PC} = min; SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC10}	—	160	—	155	—	150	mA	$\overline{SE}$ = V_{IL}, SC cycling, t_{SCC} = min
Fast page mode block wnte current *3	I_{CC4BW}	—	130	—	125	—	120	mA	$\overline{CAS}$ cycling, $\overline{RAS}$ = V_{IL}; t_{PC} = min; SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC10BW}	—	185	—	175	—	165	mA	$\overline{SE}$ = V_{IL}, SC cycling, t_{SCC} = min
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC5}	—	85	—	75	—	65	mA	$\overline{RAS}$ cycling, t_{RC} = min; SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC11}	—	140	—	130	—	120	mA	$\overline{SE}$ = V_{IL}, SC cycling, t_{SCC} = min
Data transfer current	I_{CC6}	—	130	—	115	—	100	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min; SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC12}	—	180	—	165	—	145	mA	$\overline{SE}$ = V_{IL}, SC cycling, t_{SCC} = min
Input leakage current	I_{LI}	−10	10	−10	10	−10	10	µA	0 V ≤ Vin ≤ 7 V
Output leakage current	I_{LO}	−10	10	−10	10	−10	10	µA	0 V ≤ Vout ≤ 7 V Dout, Sout = disable
Output high voltage	V_{OH}	2.4	—	2.4	—	2.4	—	V	I_{OH} = −1 mA
Output low voltage	V_{OL}	—	0.4	—	0.4	—	0.4	V	I_{OL} = 2.1 mA

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed once while $\overline{RAS}$ is low and $\overline{CAS}$ is high.
3. Address can be changed once in 1 page cycle (t_{PC}).

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 10%, f = 1 MHz, Bias: Clock, I/O = V_{CC}, address = V_{SS})

Parameter	Symbol	Typ	Max	Unit	Note
Input capacitance (Address)	C_{I1}	—	5	pF	1
Input capacitance (Clocks)	C_{I2}	—	5	pF	1
Output capacitance (I/O, SI/O, QSF)	$C_{I/O}$	—	7	pF	1

Notes: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V) *1, *16

Test Conditions

- Input rise and fall times: 5 ns
- Input pulse levels: V_{SS} to 3.0 V
- Input timing reference levels: 0.8 V, 2.4 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: RAM 1TTL + CL (50 pF)
  SAM, QSF 1TTL + CL (30 pF)
  (Including scope and jig)

Common Parameter

		HM538253-7		HM538253-8		HM538253-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Random read or write cycle time	t_{RC}	130	—	150	—	180	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	50	—	60	—	70	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10000	80	10000	100	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	—	20	—	25	—	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	12	—	15	—	15	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	20	75	ns	2
$\overline{RAS}$ hold time referenced to $\overline{CAS}$	t_{RSH}	20	—	20	—	25	—	ns	
$\overline{CAS}$ hold time referenced to $\overline{RAS}$	t_{CSH}	70	—	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	10	—	ns	

Common Parameter (cont)

Parameter	Symbol	HM538253-7 Min	HM538253-7 Max	HM538253-8 Min	HM538253-8 Max	HM538253-10 Min	HM538253-10 Max	Unit	Notes
Transition time (rise to fall)	t_T	3	50	3	50	3	50	ns	3
Refresh period	t_{REF}	—	8	—	8	—	8	ms	
$\overline{DT}$ to $\overline{RAS}$ setup time	t_{DTS}	0	—	0	—	0	—	ns	
$\overline{DT}$ to $\overline{RAS}$ hold time	t_{DTH}	10	—	10	—	10	—	ns	
DSF1 to $\overline{RAS}$ setup time	t_{FSR}	0	—	0	—	0	—	ns	
DSF1 to $\overline{RAS}$ hold time	t_{RFH}	10	—	10	—	10	—	ns	
DSF1 to $\overline{CAS}$ setup time	t_{FSC}	0	—	0	—	0	—	ns	
DSF1 to $\overline{CAS}$ hold time	t_{CFH}	12	—	15	—	15	—	ns	
Data-in to $\overline{CAS}$ delay time	t_{DZC}	0	—	0	—	0	—	ns	4
Data-in to $\overline{OE}$ delay time	t_{DZO}	0	—	0	—	0	—	ns	4
Output buffer turn-off delay referenced to $\overline{CAS}$	t_{OFF1}	—	15	—	20	—	20	ns	5
Output buffer turn-off delay referenced to $\overline{OE}$	t_{OFF2}	—	15	—	20	—	20	ns	5

Read Cycle (RAM), Page Mode Read Cycle

Parameter	Symbol	HM538253-7 Min	HM538253-7 Max	HM538253-8 Min	HM538253-8 Max	HM538253-10 Min	HM538253-10 Max	Unit	Notes
Access time from $\overline{RAS}$	t_{RAC}	—	70	—	80	—	100	ns	6, 7
Access time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	25	ns	7, 8
Access time from $\overline{OE}$	t_{OAC}	—	20	—	20	—	25	ns	7
Address access time	t_{AA}	—	35	—	40	—	45	ns	7, 9
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	0	—	ns	10
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0	—	5	—	10	—	ns	10
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	15	55	ns	2
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	—	40	—	45	—	ns	
Column address to $\overline{CAS}$ lead time	t_{CAL}	35	—	40	—	45	—	ns	
Page mode cycle time	t_{PC}	45	—	50	—	55	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	7	—	10	—	10	—	ns	
Access time from $\overline{CAS}$ precharge	t_{ACP}	—	40	—	45	—	50	ns	
Page mode $\overline{RAS}$ pulse width	t_{RASP}	70	100000	80	100000	100	100000	ns	

Write Cycle (RAM), Page Mode Write Cycle, Color Register Set Cycle

		HM538253-7		HM538253-8		HM538253-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	11
Write command hold time	t_{WCH}	12	—	15	—	15	—	ns	
Write command pulse width	t_{WP}	12	—	15	—	15	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	—	20	—	20	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	—	20	—	20	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	12
Data-in hold time	t_{DH}	12	—	15	—	15	—	ns	12
$\overline{WE}$ to $\overline{RAS}$ setup time	t_{WS}	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ hold time	t_{WH}	10	—	10	—	10	—	ns	
Mask data to $\overline{RAS}$ setup time	t_{MS}	0	—	0	—	0	—	ns	
Mask data to $\overline{RAS}$ hold time	t_{MH}	10	—	10	—	10	—	ns	
$\overline{OE}$ hold time referenced to $\overline{WE}$	t_{OEH}	15	—	20	—	20	—	ns	
Page mode cycle time	t_{PC}	45	—	50	—	55	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	7	—	10	—	10	—	ns	
$\overline{CAS}$ to data-in delay time	t_{CDD}	15	—	20	—	20	—	ns	13
Page mode $\overline{RAS}$ pulse width	t_{RASP}	70	100000	80	100000	100	100000	ns	

Read-Modify-Write Cycle

		HM538253-7		HM538253-8		HM538253-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Read-modify-write cycle time	t_{RWC}	180	—	200	—	230	—	ns	
$\overline{RAS}$ pulse width (read-modify-write cycle)	t_{RWS}	120	10000	130	10000	150	10000	ns	
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	40	—	45	—	50	—	ns	14
Column address to $\overline{WE}$ delay time	t_{AWD}	60	—	65	—	70	—	ns	14
$\overline{OE}$ to data-in delay time	t_{ODD}	15	—	20	—	20	—	ns	12
Access time from $\overline{RAS}$	t_{RAC}	—	70	—	80	—	100	ns	6, 7
Access time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	25	ns	7, 8
Access time from $\overline{OE}$	t_{OAC}	—	20	—	20	—	25	ns	7
Address access time	t_{AA}	—	35	—	40	—	45	ns	7, 9
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	15	55	ns	
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	—	20	—	20	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	—	20	—	20	—	ns	
Write command pulse width	t_{WP}	12	—	15	—	15	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	12
Data-in hold time	t_{DH}	12	—	15	—	15	—	ns	12
$\overline{OE}$ hold time referenced to $\overline{WE}$	t_{OEH}	15	—	20	—	20	—	ns	

Refresh Cycle

		HM538253-7		HM538253-8		HM538253-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10	—	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	—	10	—	10	—	ns	

Flash Write Cycle, Block Write Cycle, and Register Read Cycle

		HM538253-7		HM538253-8		HM538253-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{CAS}$ to data-in delay time	t_{CDD}	15	—	20	—	20	—	ns	13
$\overline{OE}$ to data-in delay time	t_{ODD}	15	—	20	—	20	—	ns	13

CBR Refresh with Register Reset

		HM538253-7		HM538253-8		HM538253-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Split transfer setup time	t_{STS}	20	—	20	—	25	—	ns	
Split transfer hold time referenced to $\overline{RAS}$	t_{RST}	70	—	80	—	100	—	ns	

Read Transfer Cycle

		HM538253-7		HM538253-8		HM538253-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{DT}$ hold time referenced to $\overline{RAS}$	t_{RDH}	60	10000	65	10000	80	10000	ns	
$\overline{DT}$ hold time referenced to $\overline{CAS}$	t_{CDH}	20	—	20	—	25	—	ns	
$\overline{DT}$ hold time referenced to column address	t_{ADH}	25	—	30	—	30	—	ns	
$\overline{DT}$ precharge time	t_{DTP}	20	—	20	—	30	—	ns	
$\overline{DT}$ to $\overline{RAS}$ delay time	t_{DRD}	60	—	70	—	80	—	ns	
SC to $\overline{RAS}$ setup time	t_{SRS}	15	—	20	—	30	—	ns	
1st SC to $\overline{RAS}$ hold time	t_{SRH}	70	—	80	—	100	—	ns	
1st SC to $\overline{CAS}$ hold time	t_{SCH}	25	—	25	—	25	—	ns	
1st SC to column address hold time	t_{SAH}	40	—	45	—	50	—	ns	
Last SC to $\overline{DT}$ delay time	t_{SDD}	5	—	5	—	5	—	ns	
1st SC to $\overline{DT}$ hold time	t_{SDH}	10	—	13	—	15	—	ns	
$\overline{DT}$ to QSF delay time	t_{DQD}	—	30	—	35	—	35	ns	15

Read Transfer Cycle (cont)

		HM538253-7		HM538253-8		HM538253-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
QSF hold time referenced to $\overline{DT}$	t_{DQH}	5	—	5	—	5	—	ns	
Serial data-in to 1st SC delay time	t_{SZS}	0	—	0	—	0	—	ns	
Serial clock cycle time	t_{SCC}	25	—	28	—	30	—	ns	
SC pulse width	t_{SC}	5	—	10	—	10	—	ns	
SC precharge time	t_{SCP}	10	—	10	—	10	—	ns	
SC access time	t_{SCA}	—	20	—	23	—	25	ns	15
Serial data-out hold time	t_{SOH}	5	—	5	—	5	—	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	15	—	15	—	ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	15	55	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	—	40	—	45	—	ns	
$\overline{RAS}$ to QSF delay time	t_{RQD}	—	70	—	75	—	85	ns	15
$\overline{CAS}$ to QSF delay time	t_{CQD}	—	35	—	35	—	35	ns	15
QSF hold time referenced to $\overline{RAS}$	t_{RQH}	20	—	20	—	25	—	ns	
QSF hold time referenced to $\overline{CAS}$	t_{CQH}	5	—	5	—	5	—	ns	

Masked Write Transfer Cycle

Parameter	Symbol	HM538253-7 Min	HM538253-7 Max	HM538253-8 Min	HM538253-8 Max	HM538253-10 Min	HM538253-10 Max	Unit	Notes
SC setup time referenced to $\overline{RAS}$	t_{SRS}	15	—	20	—	30	—	ns	
$\overline{RAS}$ to SC delay time	t_{SRD}	20	—	25	—	25	—	ns	
Serial output buffer turn-off time referenced to $\overline{RAS}$	t_{SRZ}	10	30	10	35	10	50	ns	
$\overline{RAS}$ to serial data-in delay time	t_{SID}	30	—	35	—	50	—	ns	
$\overline{RAS}$ to QSF delay time	t_{RQD}	—	70	—	75	—	85	ns	15
$\overline{CAS}$ to QSF delay time	t_{CQD}	—	35	—	35	—	35	ns	15
QSF hold time referenced to $\overline{RAS}$	t_{RQH}	20	—	20	—	25	—	ns	
QSF hold time referenced to $\overline{CAS}$	t_{CQH}	5	—	5	—	5	—	ns	
Serial clock cycle time	t_{SCC}	25	—	28	—	30	—	ns	
SC pulse width	t_{SC}	5	—	10	—	10	—	ns	
SC precharge time	t_{SCP}	10	—	10	—	10	—	ns	
SC access time	t_{SCA}	—	20	—	23	—	25	ns	15
Serial data-out hold time	t_{SOH}	5	—	5	—	5	—	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	15	—	15	—	ns	

Split Read Transfer Cycle, Masked Split Write Transfer Cycle

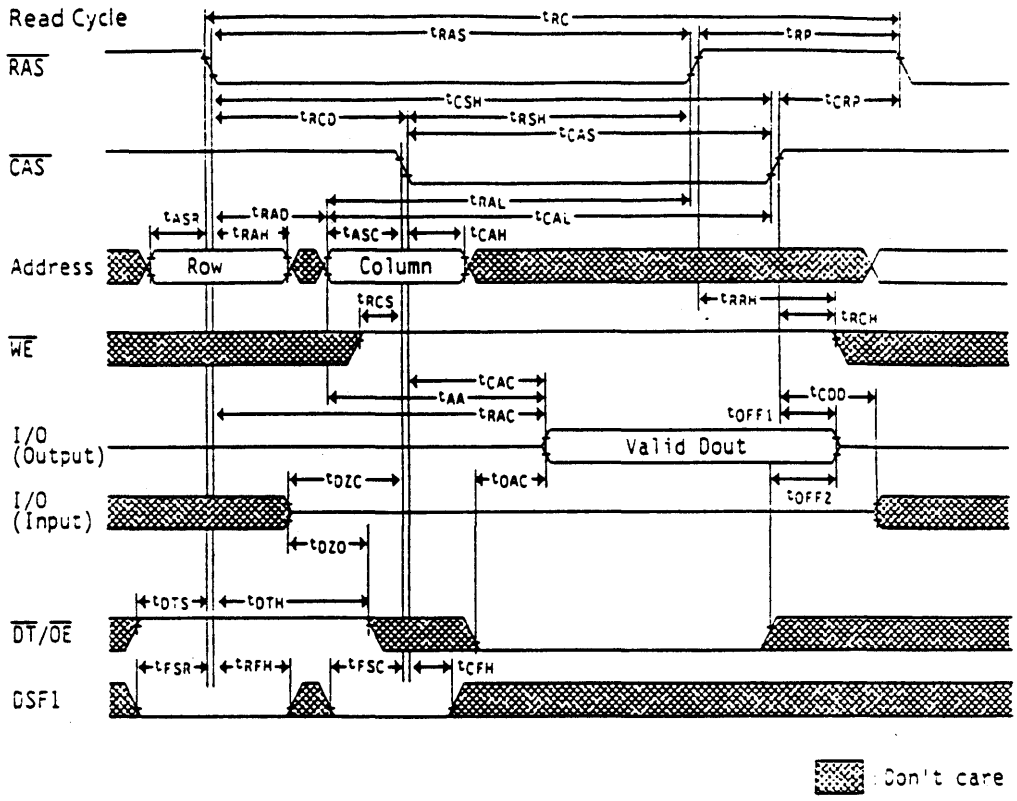
		HM538253-7		HM538253-8		HM538253-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Split transfer setup time	t_{STS}	20	—	20	—	25	—	ns	
Split transfer hold time referenced to $\overline{RAS}$	t_{RST}	70	—	80	—	100	—	ns	
Split transfer hold time referenced to $\overline{CAS}$	t_{CST}	20	—	20	—	25	—	ns	
Split transfer hold time referenced to column address	t_{AST}	35	—	40	—	45	—	ns	
SC to QSF delay time	t_{SQD}	—	30	—	30	—	30	ns	15
QSF hold time referenced to SC	t_{SQH}	5	—	5	—	5	—	ns	
Serial clock cycle time	t_{SCC}	25	—	28	—	30	—	ns	
SC pulse width	t_{SC}	5	—	10	—	10	—	ns	
SC precharge time	t_{SCP}	10	—	10	—	10	—	ns	
SC access time	t_{SCA}	—	20	—	23	—	25	ns	15
Serial data-out hold time	t_{SOH}	5	—	5	—	5	—	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	15	—	15	—	ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	15	55	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	—	40	—	45	—	ns	

Serial Read Cycle, Serial Write Cycle

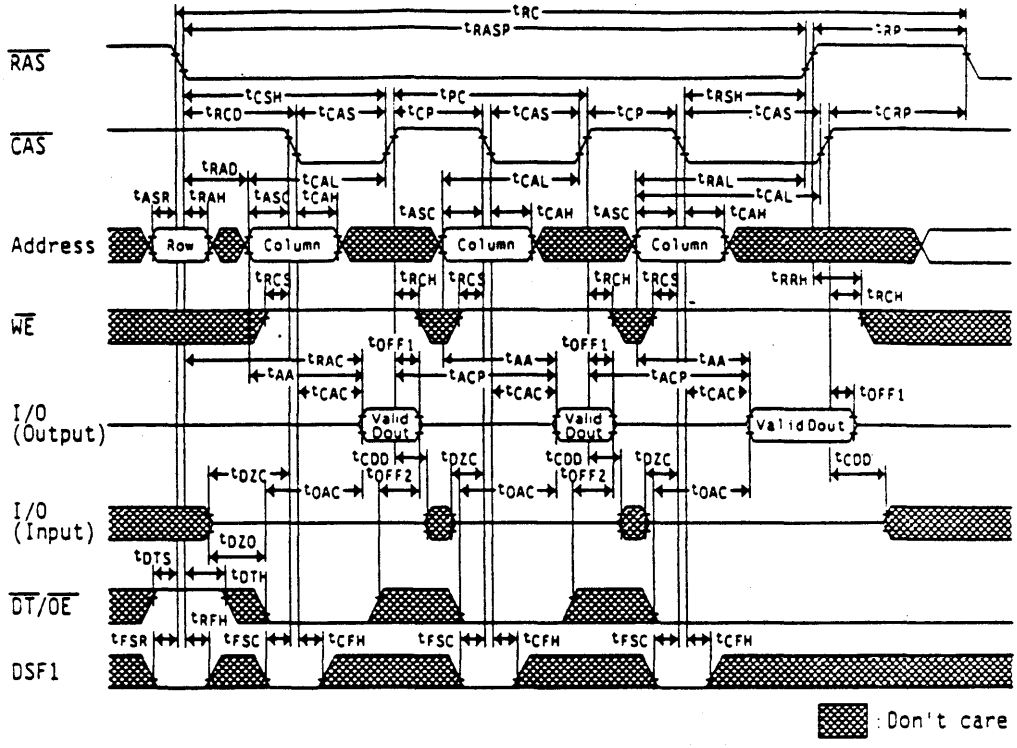
		HM538253-7		HM538253-8		HM538253-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Serial clock cycle time	t_{SCC}	25	—	28	—	30	—	ns	
SC pulse width	t_{SC}	5	—	10	—	10	—	ns	
SC precharge width	t_{SCP}	10	—	10	—	10	—	ns	
Access time from SC	t_{SCA}	—	20	—	23	—	25	ns	15
Access time from $\overline{SE}$	t_{SEA}	—	17	—	20	—	25	ns	15
Serial data-out hold time	t_{SOH}	5	—	5	—	5	—	ns	
Serial output buffer turn-off time referenced to $\overline{SE}$	t_{SHZ}	—	15	—	20	—	20	ns	5,17
$\overline{SE}$ to serial output in low-Z	t_{SLZ}	0	—	0	—	0	—	ns	5,17
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	15	—	15	—	ns	
Serial write enable setup time	t_{SWS}	0	—	0	—	0	—	ns	
Serial wrtie enbable hold time	t_{SWH}	15	—	15	—	15	—	ns	
Serial write disable setup time	t_{SWIS}	0	—	0	—	0	—	ns	
Serial write disable hold time	t_{SWIH}	15	—	15	—	15	—	ns	

Notes:
1. AC measurements assume t_T = 5 ns.
2. When $t_{RCD} > t_{RCD}$ (max) and $t_{RAD} > t_{RAD}$ (max), access time is specified by t_{CAC} or t_{AA}.
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition time t_T is measured between V_{IH} and V_{IL}.
4. Data input must be floating before output buffer is turned on. In read cycle, read-modify-write cycle and delayed write cycle, either t_{DZC} (min) or t_{DZO} (min) must be satisfied.
5. t_{OFF1} (max), t_{OFF2} (max), t_{SHZ} (max) and t_{SLZ} (min) are defined as the time at which the output acheives the open circuit condition (V_{OH} – 100 mV, V_{OL} + 100 mV). This parameter is sampled and not 100% tested.
6. Assume that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
7. Measured with a load circuit equivalent to 1 TTL loads and 50 pF.
8. When $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max), access time is specified by t_{CAC}.
9. When $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max), access time is specified by t_{AA}.
10. If either t_{RCH} or t_{RRH} is satisfied, operation is guaranteed.
11. When $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle, and I/O pins remain in an open circuit (high impedance) condition.
12. These parameters are specified by the later falling edge of $\overline{CAS}$ or $\overline{WE}$.
13. Either t_{CDD} (min) or t_{ODD} (min) must be satisfied because output buffer must be turned off by $\overline{CAS}$ or $\overline{OE}$ prior to applying data to the device when output buffer is on.
14. When $t_{AWD} \geq t_{AWD}$ (min) and $t_{CWD} \geq t_{CWD}$ (min) in read-modify-write cycle, the data of the selected address outputs to an I/O pin and input data is written into the selected address. t_{ODD} (min) must be satisfied because output buffer must be turned off by $\overline{OE}$ prior to applying data to the device.
15. Measured with a load circuit equivalent to 1 TTL loads and 30 pF.
16. After power-up, pause for 100 µs or more and execute at least 8 initialization cycle (normal memory cycle or refresh cycle), then start operation. Hitachi recommends that least 8 initialization cycle is the CBRR for internal register reset. This CBRR need not t_{STS} and t_{RST}.
17. When t_{SHZ} and t_{SLZ} are measured in the same VCC and Ta condition and tr and tf of $\overline{SE}$ are less than 5 ns, $t_{SHZ} \leq t_{SLZ} + 5$ ns. This parameter is sampled and not 100% tested.
18. After power-up, QSF output may be High-Z, so 1SC cycle is needed to be Low-Z it.
19. DSF2 pin is open pin, but Hitachi recommends it is fixed low in all operation for the addition mode in future.

■ Timing Waveforms



Fast Page Mode Read Cycle



Write Cycle

The write cycle state table as shown below is applied to early write, delayed write, page mode write, and read-modify write.

Write Cycle State Table

Menu	Cycle	$\overline{RAS}$	$\overline{CAS}$	$\overline{RAS}$	$\overline{RAS}$	$\overline{CAS}$
		DSF1	DSF1	$\overline{WE}$	I/O	I/O
		W1	W2	W3	W4	W5
RWM	Write mask (new/old) Write DQs to I/Os	0	0	0	Write mask*1	Valid data
BWM	Write mask (new/old) Block write	0	1	0	Write mask*2	Column mask*2
RW	Normal write (no mask)	0	0	1	Don't care*1	Valid data
BW	Block write (no mask)	0	1	1	Don't care*2	Column mask*2
LMR*4	Load mask resister	1	0	1	Don't care	Mask data*3
LCR*4	Load color resister	1	1	1	Don't care	Color data

Note 1

$\overline{WE}$	Mode	I/O data/$\overline{RAS}$
Low	New Mask Mode	Mask
	Persistent Mask Mode	Don't care (mask register used)
High	No mask	Don't care

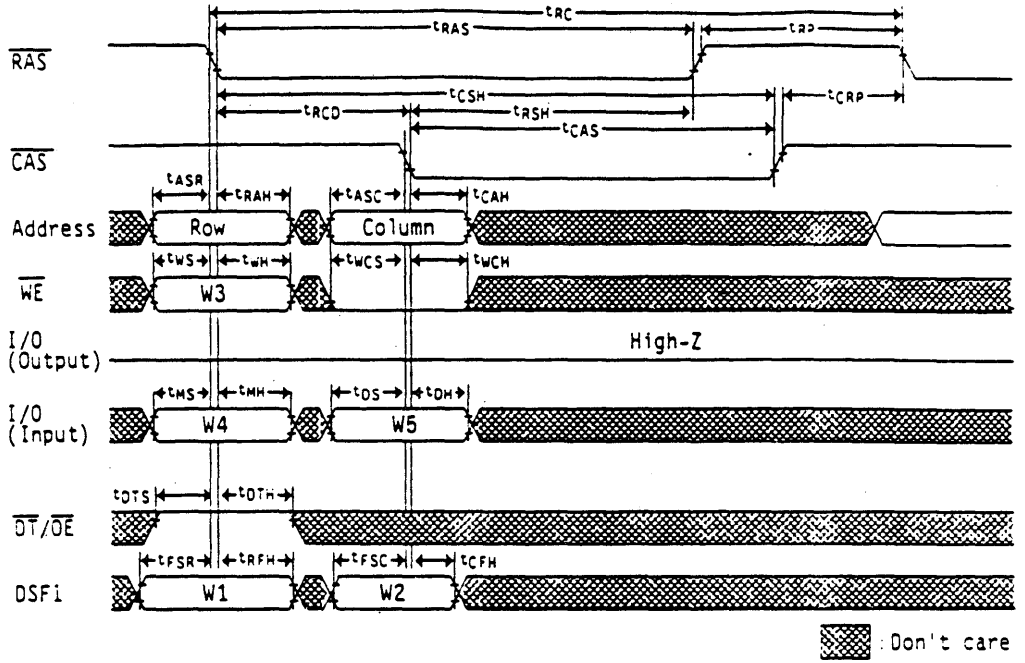
I/O Mask Data (In new mask mode)
Low: Mask
High: Non Mask
In persistent mask mode, I/O don't care

Note 2: reference Figure 2 use of Block Write

Note 3: I/O Write Mask Data
Low: Mask
High: Non mask

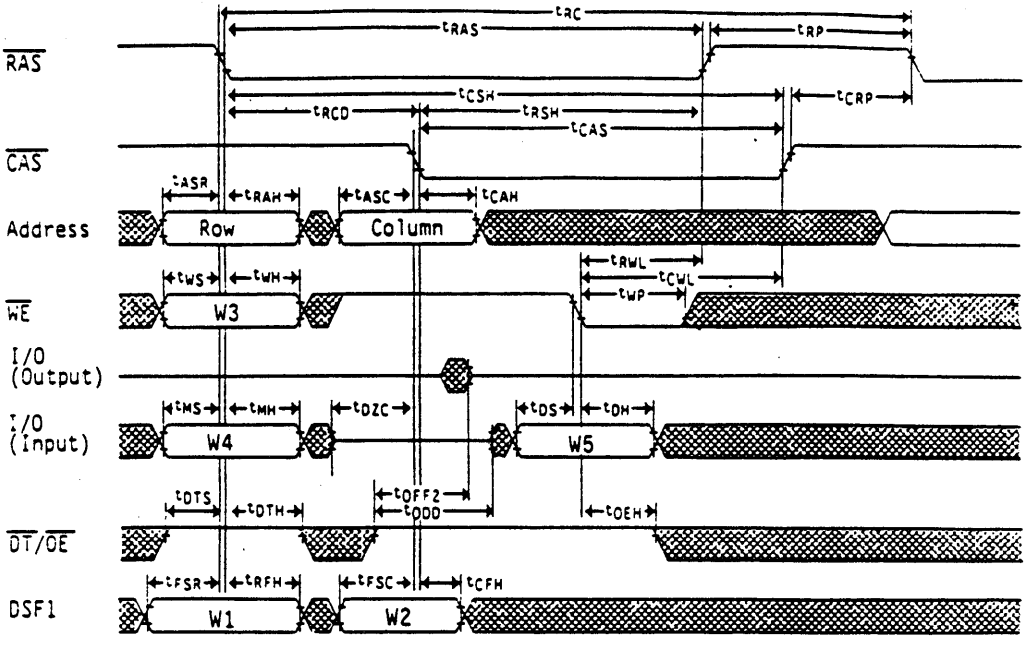
Note 4: Column Address: Don't care

Early Write Cycle



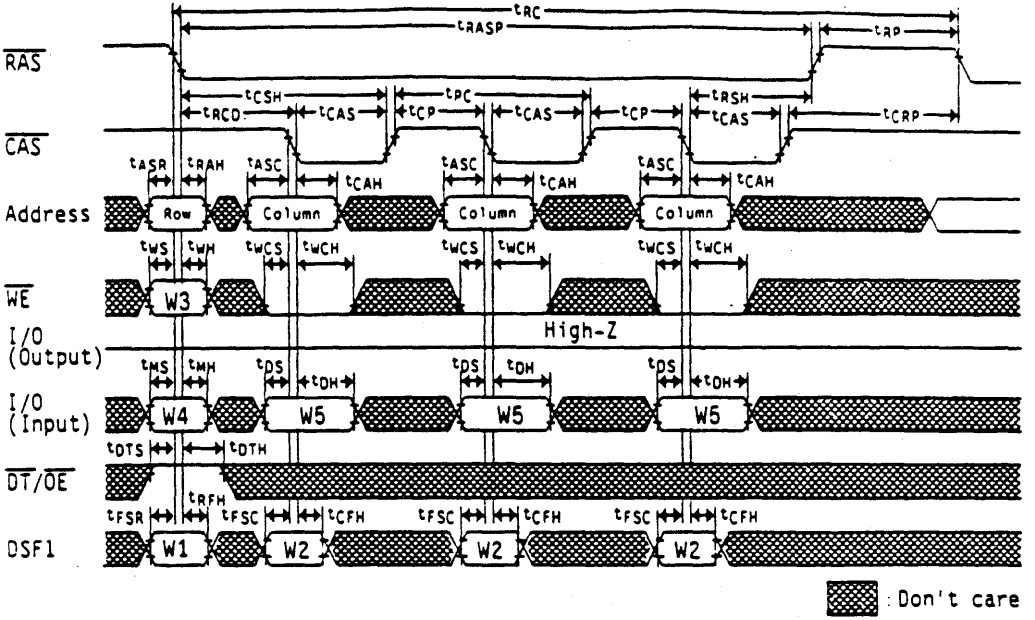
W1 to W5: See Write Cycle State Table for the logic states.

Delayed Write Cycle



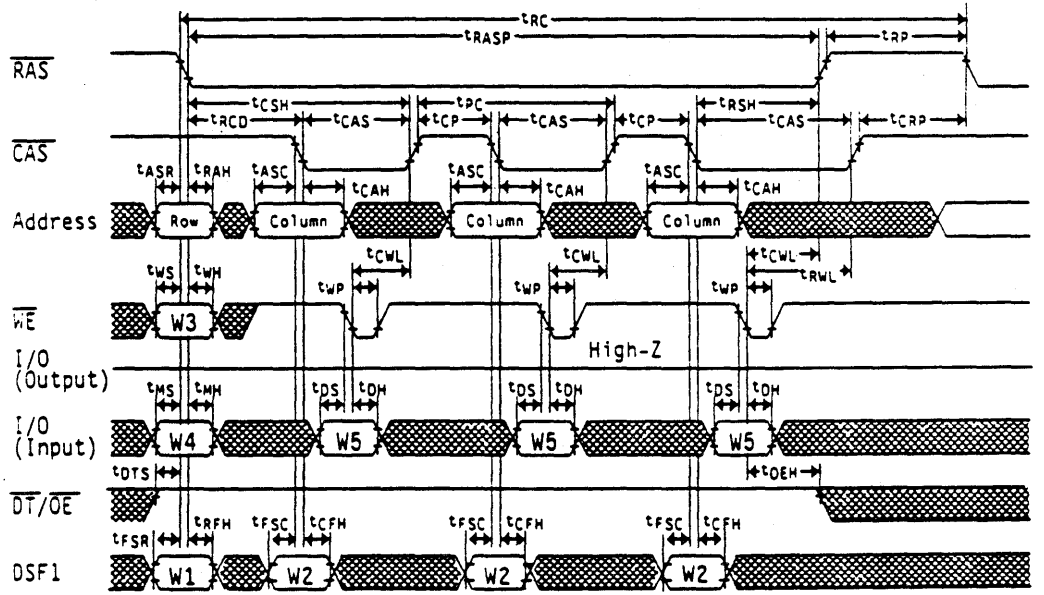
W1 to W5: See Write Cycle State Table for the logic states.

Fast Page Mode Write Cycle (Early Write)



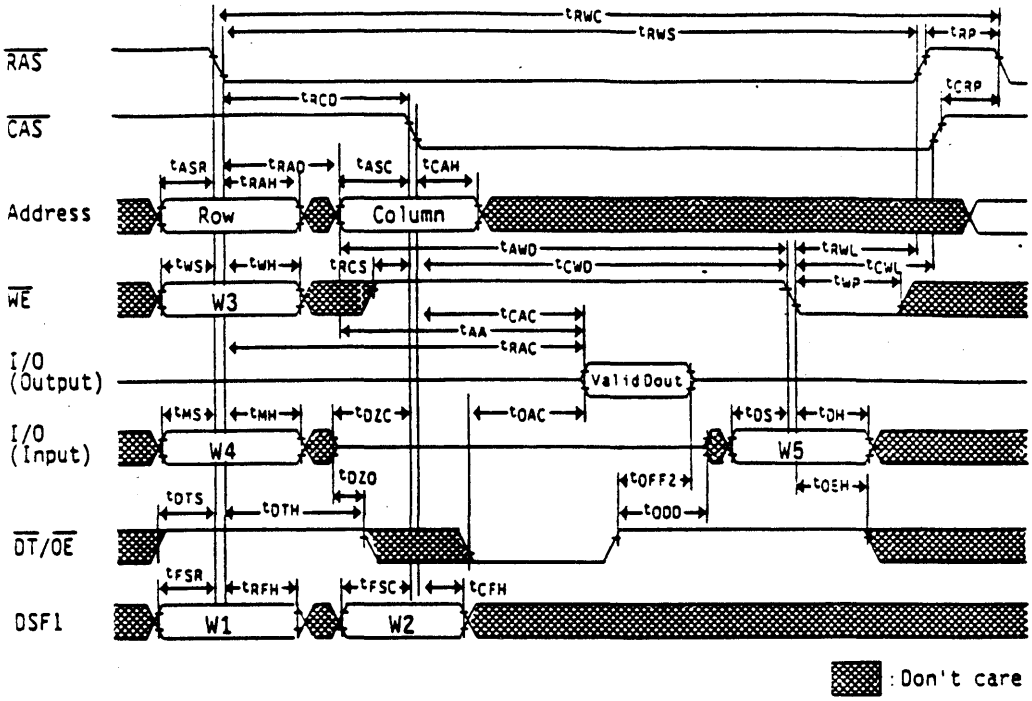
W1 to W5: See Write Cycle State Table for the logic states.

Fast Page Mode Write Cycle (Delayed Write)



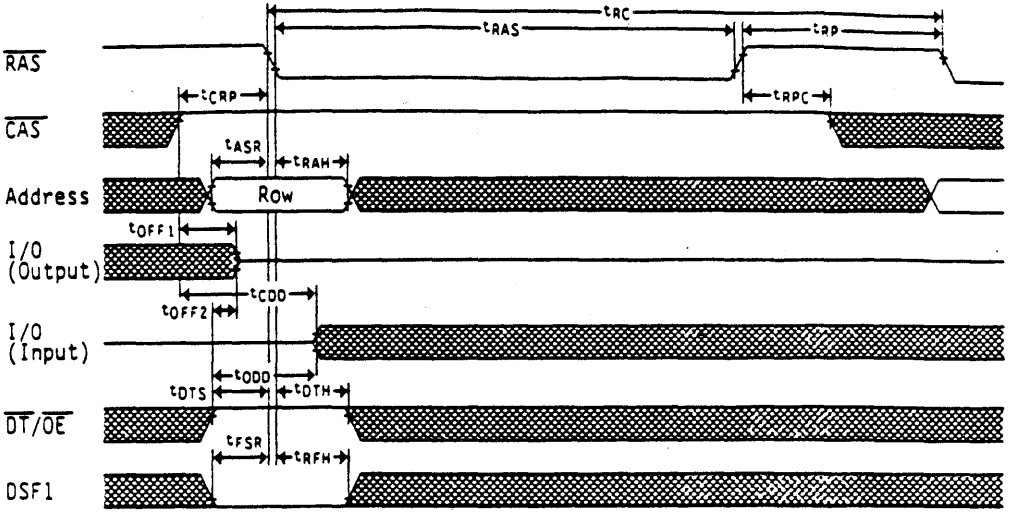
W1 to W5: See Write Cycle State Table for the locgic states.

Read- Modify-Write Cycle



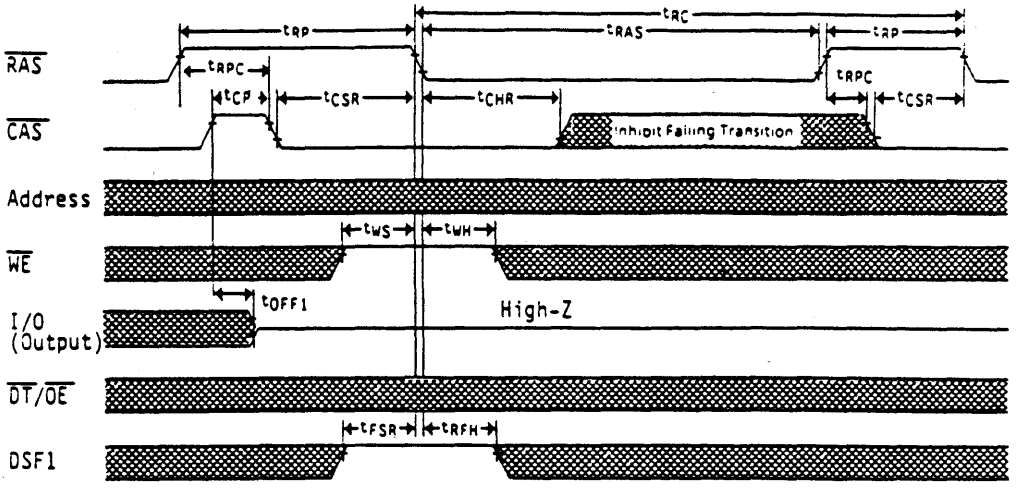
W1 to W5: See Write Cycle State Table for the logic states.

- $\overline{RAS}$-Only Refresh Cycle



$\overline{WE}$: Don't care

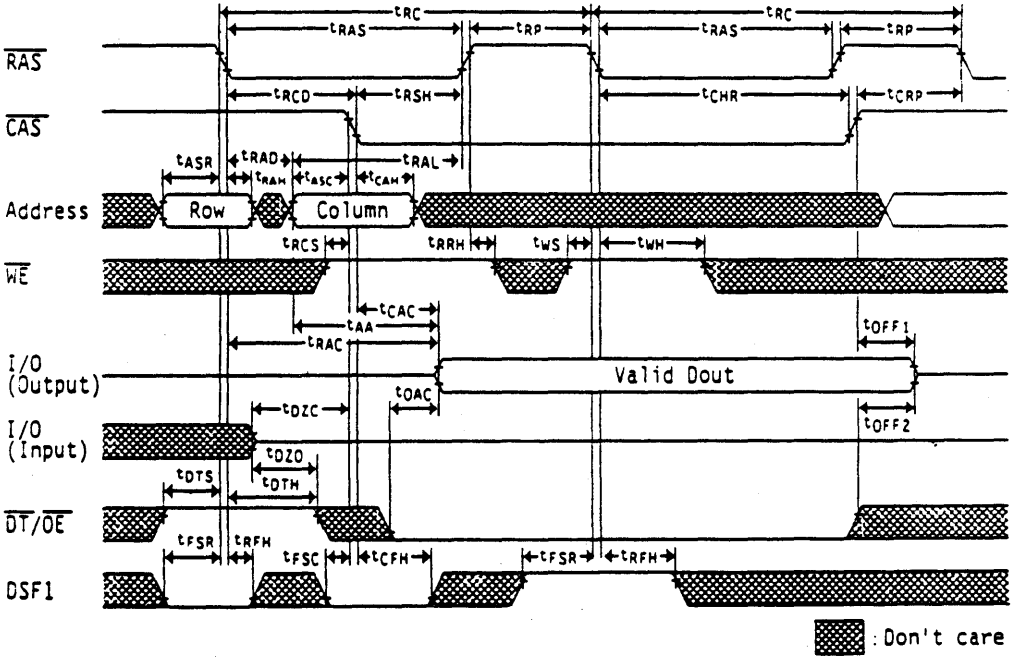
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle (CBRN)



Note: SC : Don't care

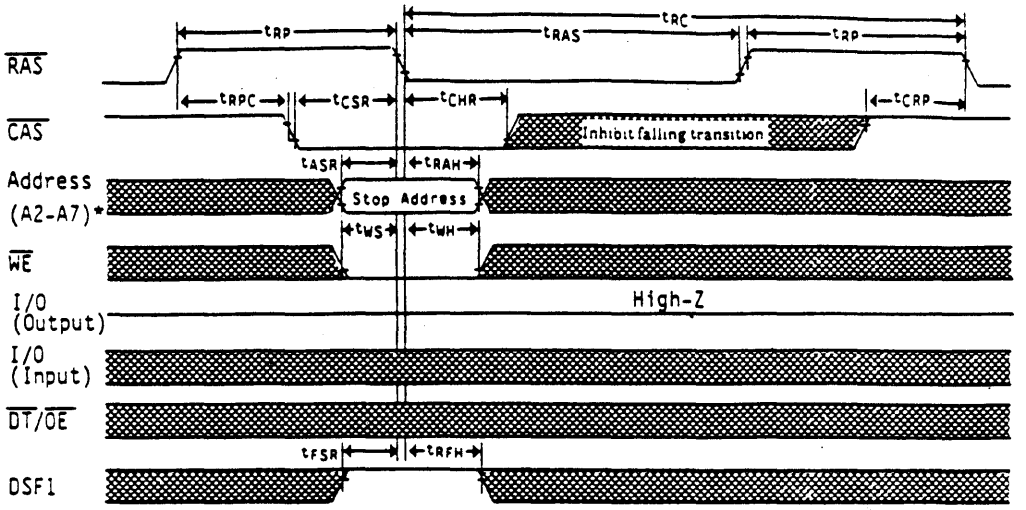
: Don't care

Hidden Refresh Cycle



: Don't care

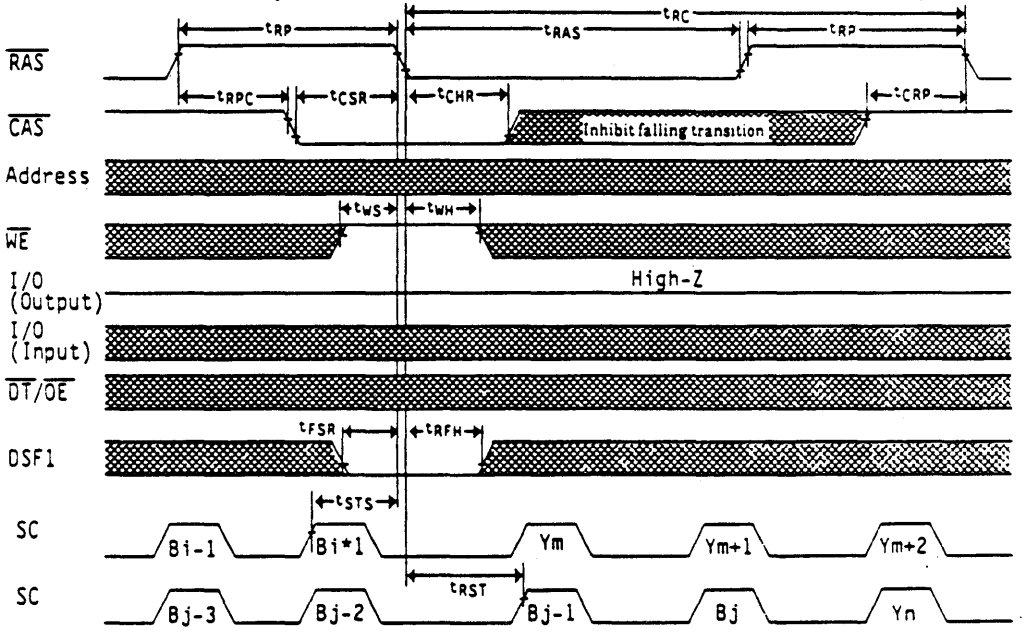
$\overline{CAS}$-Before-$\overline{RAS}$ Set Cycle (CBRS)



Note: A0, A1, A8: Don't care
SC: Don't care

: Don't care

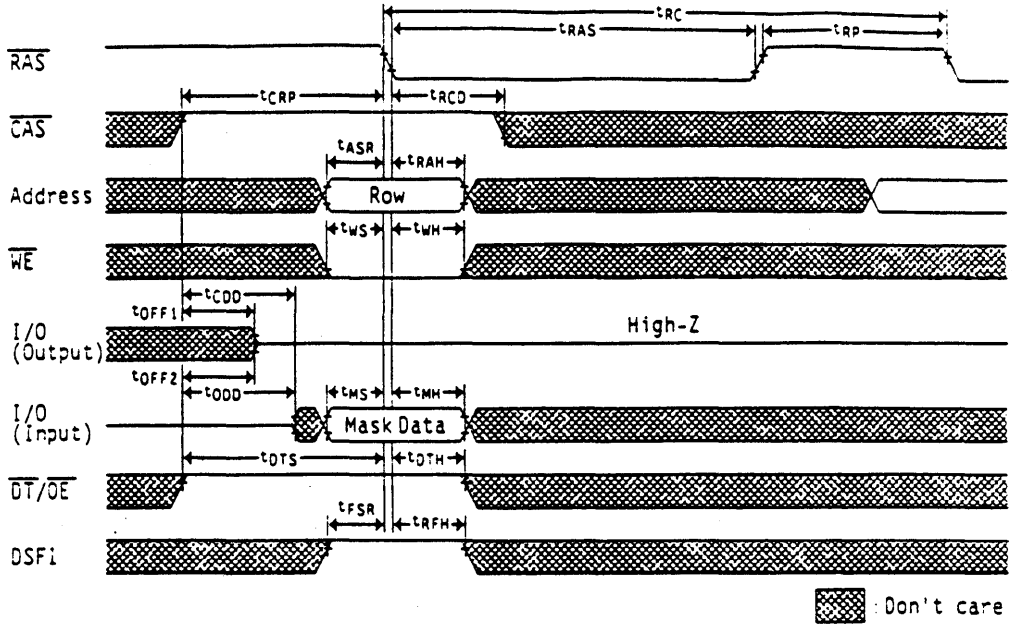
$\overline{CAS}$-Before-$\overline{RAS}$ Reset Cycle (CBRR)



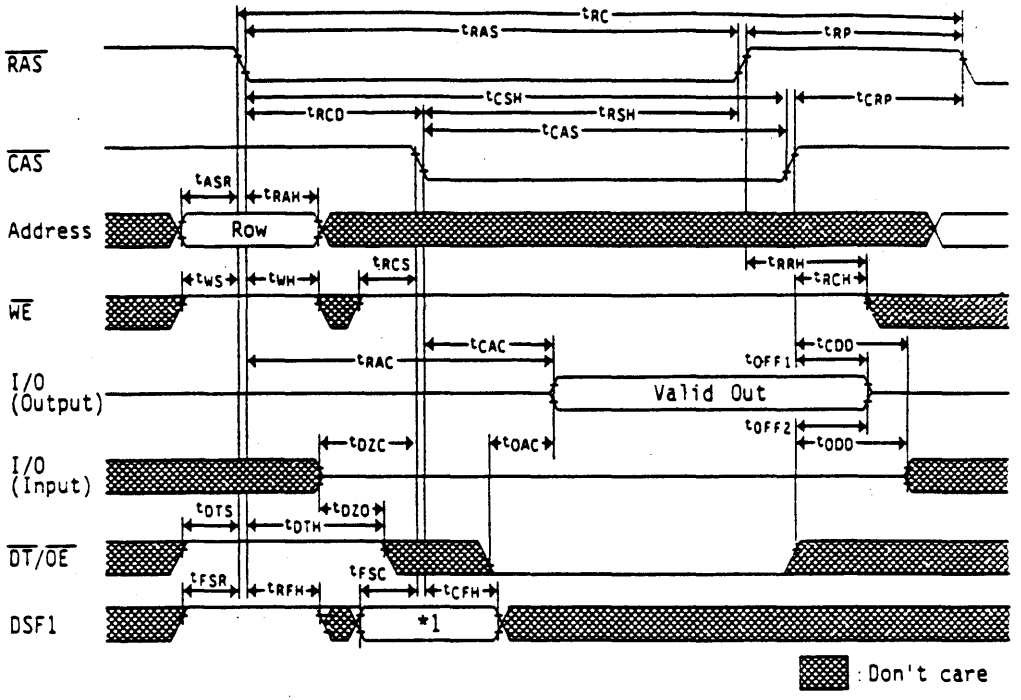
Note: 1. Bi, Bj initiate the boundary addresses.
2. Ym, Yn are the SAM start address in before SRT/MSWT.

: Don't care

Flash Write Cycle



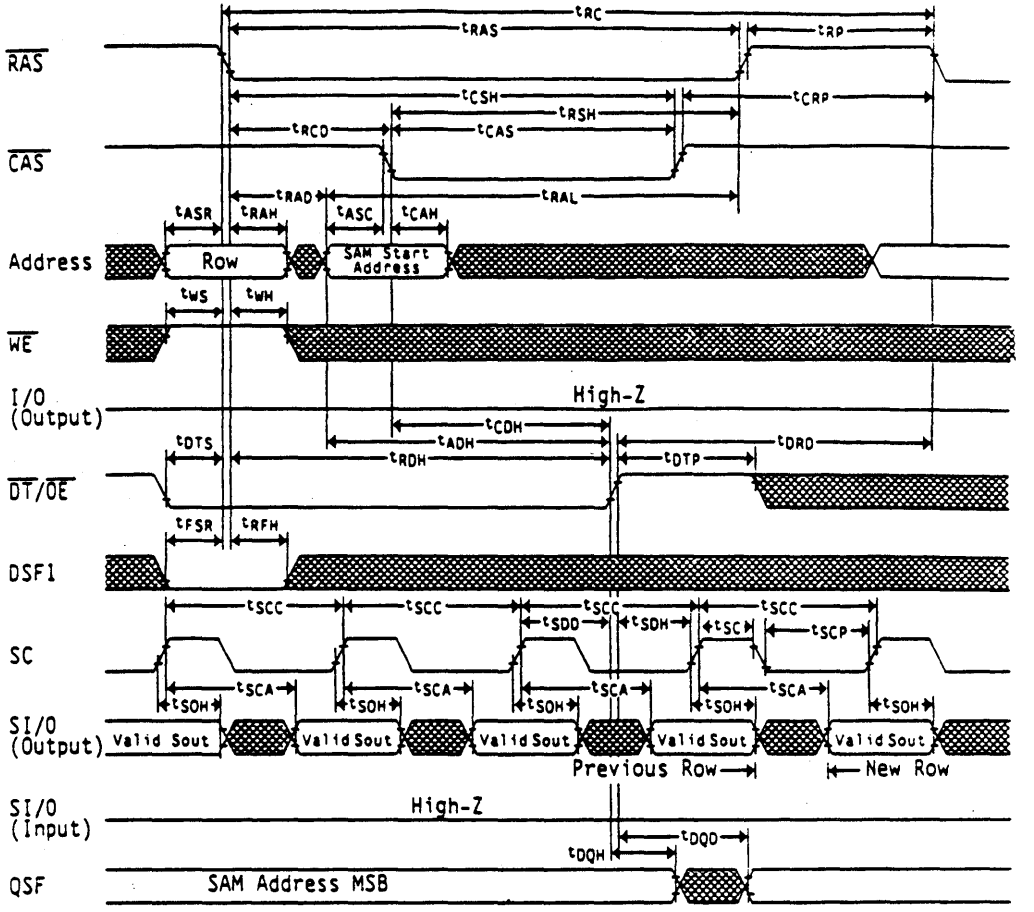
Register Read Cycle (Mask data, Color data)



Note: 1. State of DSF1 at falling edge of $\overline{CAS}$

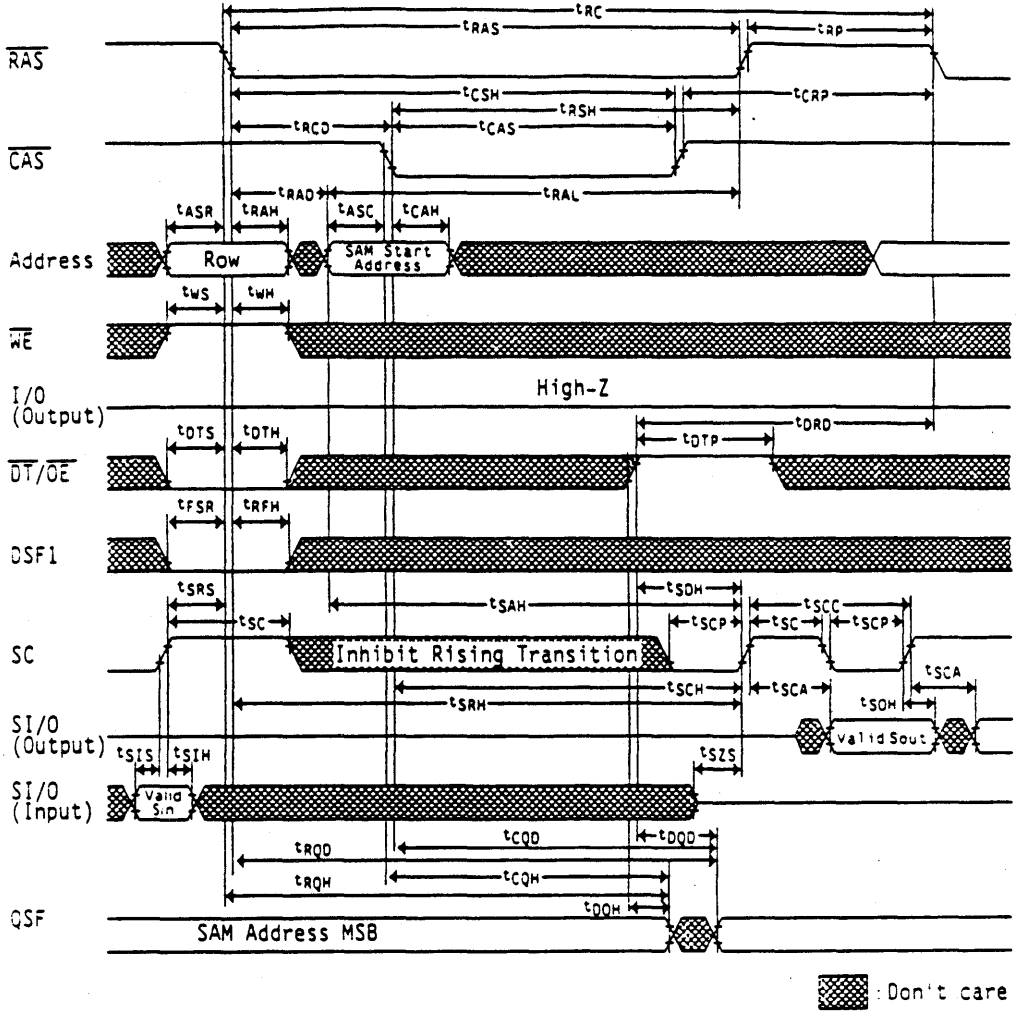
State	0	1
Accessed Data	Mask Data (LMR)	Color Data (LCR)

Read Transfer Cycle-1 (Real Time Read Transfer)

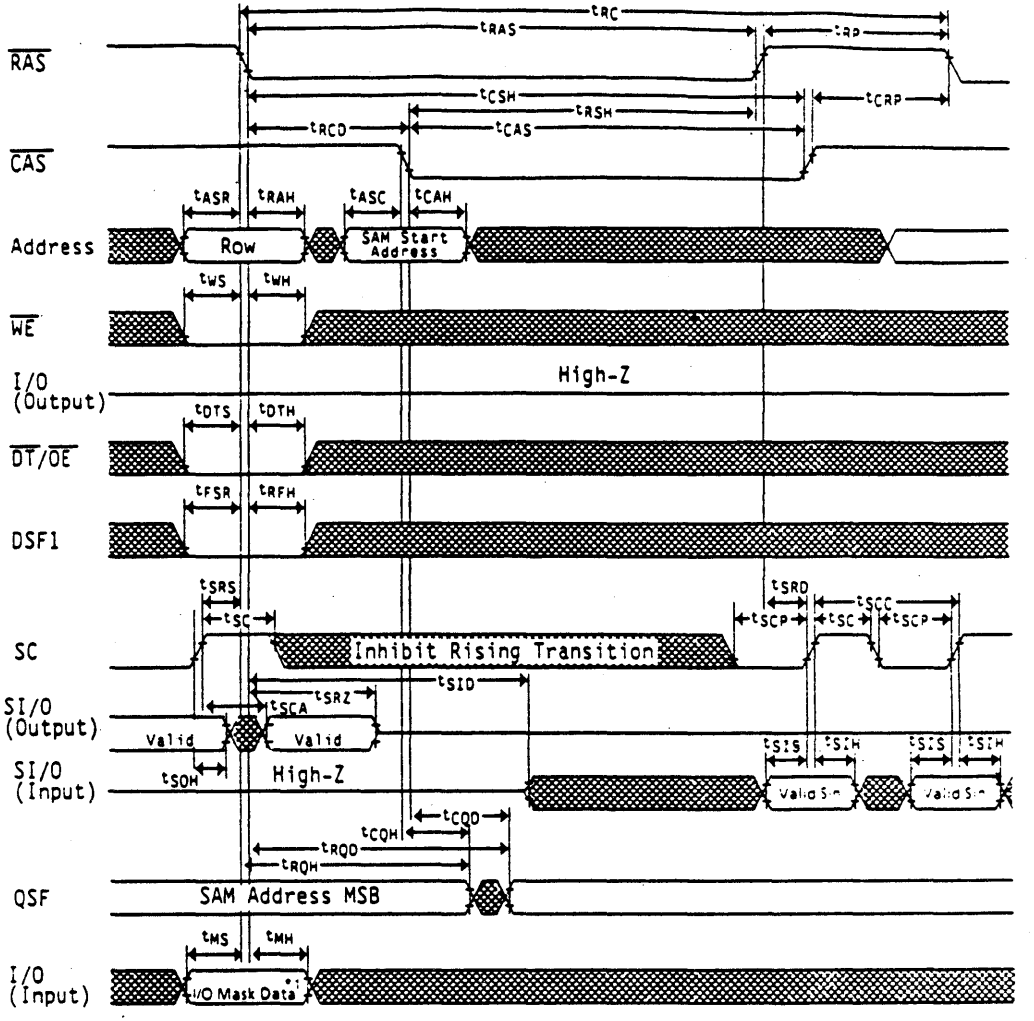


: Don't care

Read Transfer Cycle – 2



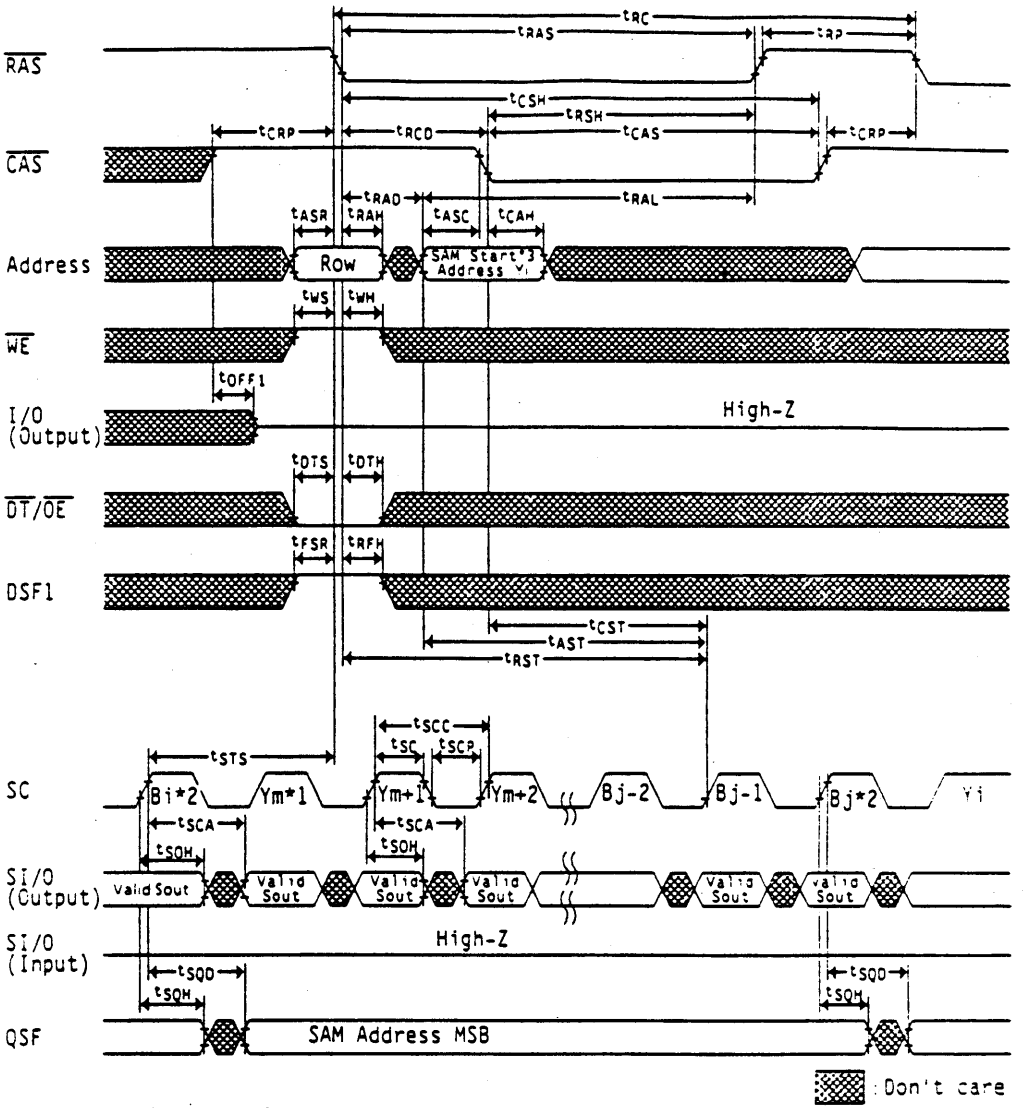
Masked Write Transfer Cycle



Note: 1. I/O Mask Data (In new mask mode)
Low : Mask
High : Non Mask
I/O : Don't care in persistent mask mode.

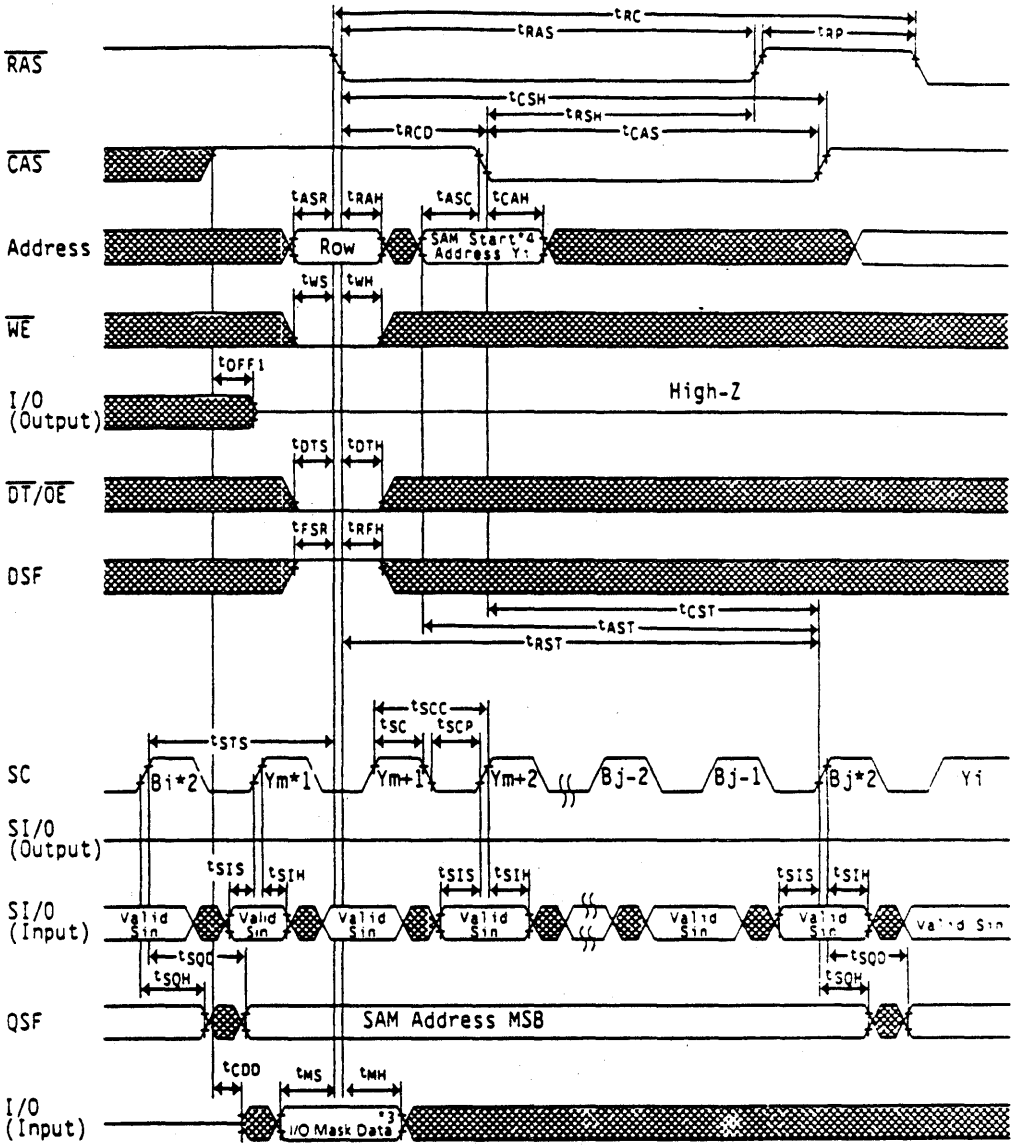
: Don't care

Split Read Transfer Cycle



Notes: 1. Ym is the SAM start address in before SRT.
2. Bi, Bj initiate the boundary address.
3. A8 : Don't care, and upper SAM or lower SAM is set automatically by the internal circuit.
SAM start address can't set on the boundary address.

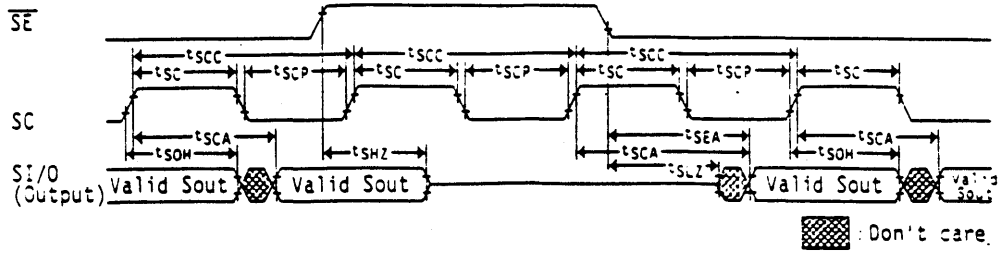
Masked Split Write Transfer Cycle



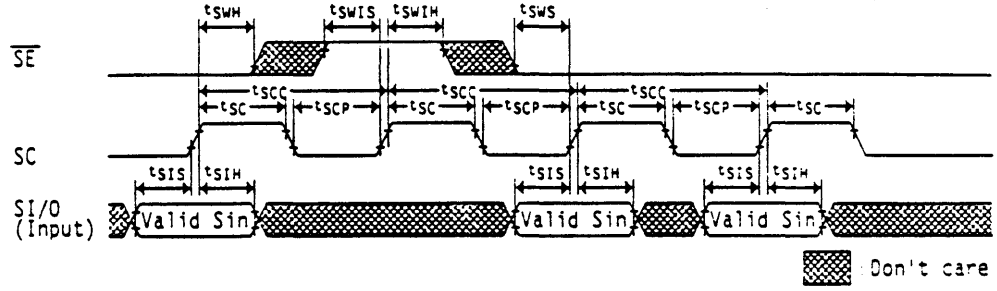
Notes: 1. Ym is the SAM start address in before MSWT.
2. Bi, Bj initiate the boundary address.
3. I/O Mask Data (In new mask mode)
Low : Mask
High : Non Mask
I/O : Don't care in persistent mask mode.
4. A8 : Don't care, and upper SAM or lower SAM is set automatically by the internal circuit.
SAM start address can't set on the boundary address.

Don't care

Serial Read Cycle

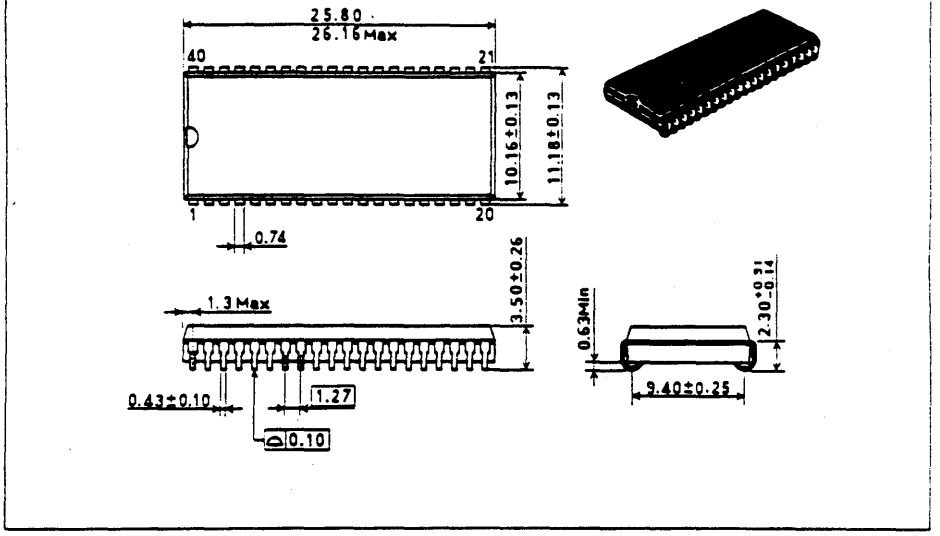


Sereal Write Cycle



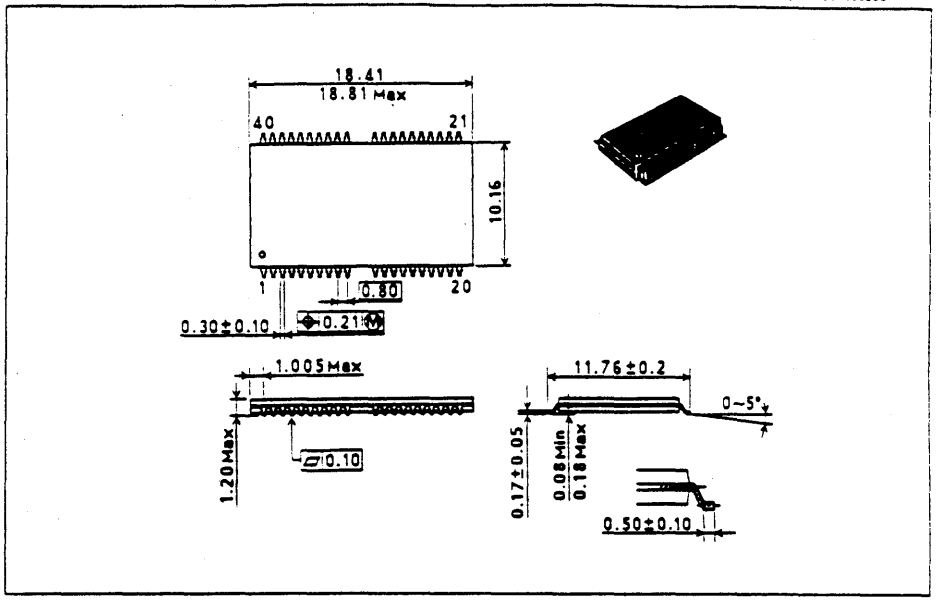
Package Dimensions

HM538253J Series (CP-40D) Unit: mm

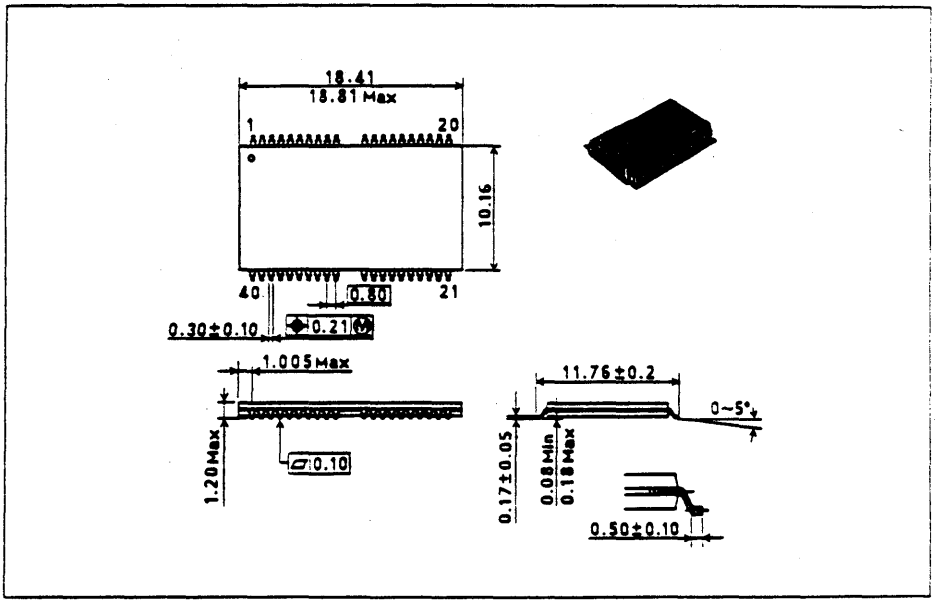


Package Dimensions (cont)

HM538253TT Series (TTP-40DA) Unit: mm



HM538253RR Series (TTP-40DAR) Unit: mm



HM538254 Series

262,144-Word x 8-Bit Multiport CMOS Video RAM

HITACHI

Rev. 3
Jul. 7, 1993

The HM538254 is a 2-Mbit multiport video RAM equipped with a 256-kword x 8-bit dynamic RAM and a 512-word x 8-bit SAM (full-sized SAM). Its RAM and SAM operate independently and asynchronously. The HM538254 has basically upward-compatibility with the HM534253A / HM538123A except that pseudo-write-transfer cycle is replaced with masked-write-transfer cycle, which has been approved by JEDEC. Furthermore, several new features are added to the HM538254 without conflict with the conventional features. Stopping column feature realizes much flexibility to the length of split SAM register. Persistent mask is also installed according to the TMS34020 features. The HM538254 has Hyper page mode.

Features

- Multiport organization
  - Asynchronous and simultaneous operation of RAM and SAM capability
    - RAM: 256 kword x 8 bit
    - SAM: 512 word x 8 bit
- Access time
  - RAM: 70 ns/80 ns/100 ns (max)
  - SAM: 20 ns/23 ns/25 ns (max)
- Cycle time
  - RAM: 130 ns/150 ns/180 ns (min)
  - SAM: 25 ns/28 ns/30 ns (min)
- Low power
  - Active RAM: 578 mW/495 mW/468 mW
    SAM: 358 mW/330 mW/303 mW
  - Standby 38.5 mW (max)
- Hyper page mode capability
  - Cycle time: 35 ns/40 ns/45 ns
  - Power RAM: 825 mW/715 mW/605 mW
- Masked-write-transfer cycle capability
- Stopping column feature capability
- Persistent mask capability
- Mask write mode capability
- Bidirectional data transfer cycle between RAM and SAM capability
- Split transfer cycle capability
- Block write mode capability
- Flash write mode capability
- 3 variations of refresh (8 ms/512 cycles)
  - $\overline{\text{RAS}}$-only refresh
  - $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - Hidden refresh
- TTL compatible

Ordering Information

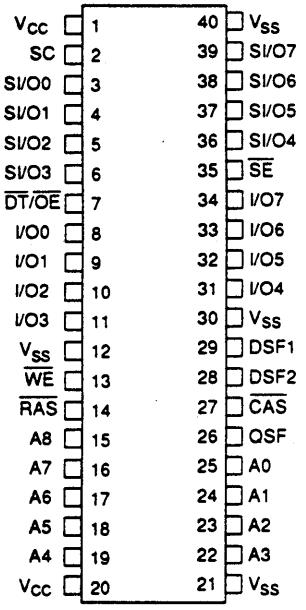
Type No.	Access time	Package
HM538254J-7	70 ns	400 mil 40-pin plastic SOJ (CP-40D)
HM538254J-8	80 ns	
HM538254J-10	100 ns	
HM538254TT-7	70 ns	44-pin thin small outline package (TTP-40DA)
HM538254TT-8	80 ns	
HM538254TT-10	100 ns	
HM538254RR-7	70 ns	44-pin thin small outline package (TTP-40DAR)
HM538254RR-8	80 ns	
HM538254RR-10	100 ns	

Hitachi semiconductor

93.09.02
ADE-203-112C(Z)

Pin Arrangement

HM538254J Series

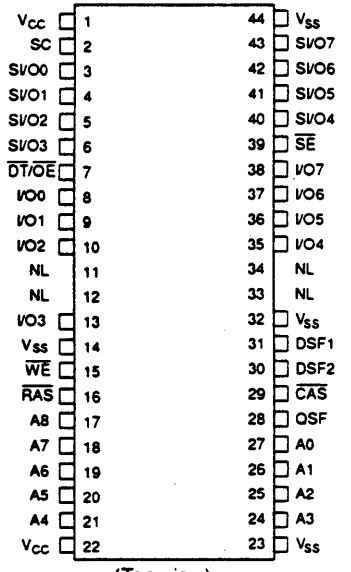


(Top view)

Pin Description

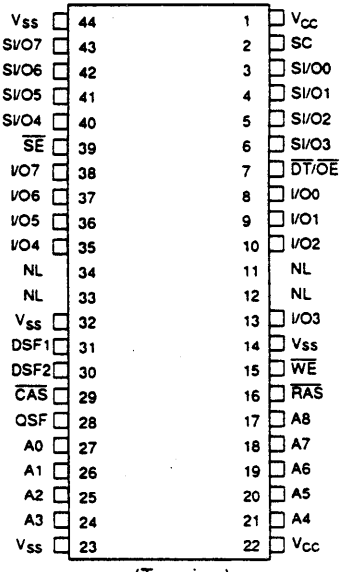
Pin name	Function
A0 – A8	Address inputs
I/O0 – I/O7	RAM port data inputs/outputs
SI/O0 – SI/O7	SAM port data inputs/outputs
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
$\overline{DT/OE}$	Data transfer/output enable
SC	Serial clock
$\overline{SE}$	SAM port enable
DSF1, DSF2	Special function input flag
QSF	Special function output flag
V_{CC}	Power supply
V_{SS}	Ground
NL	No lead

HM538254TT Series



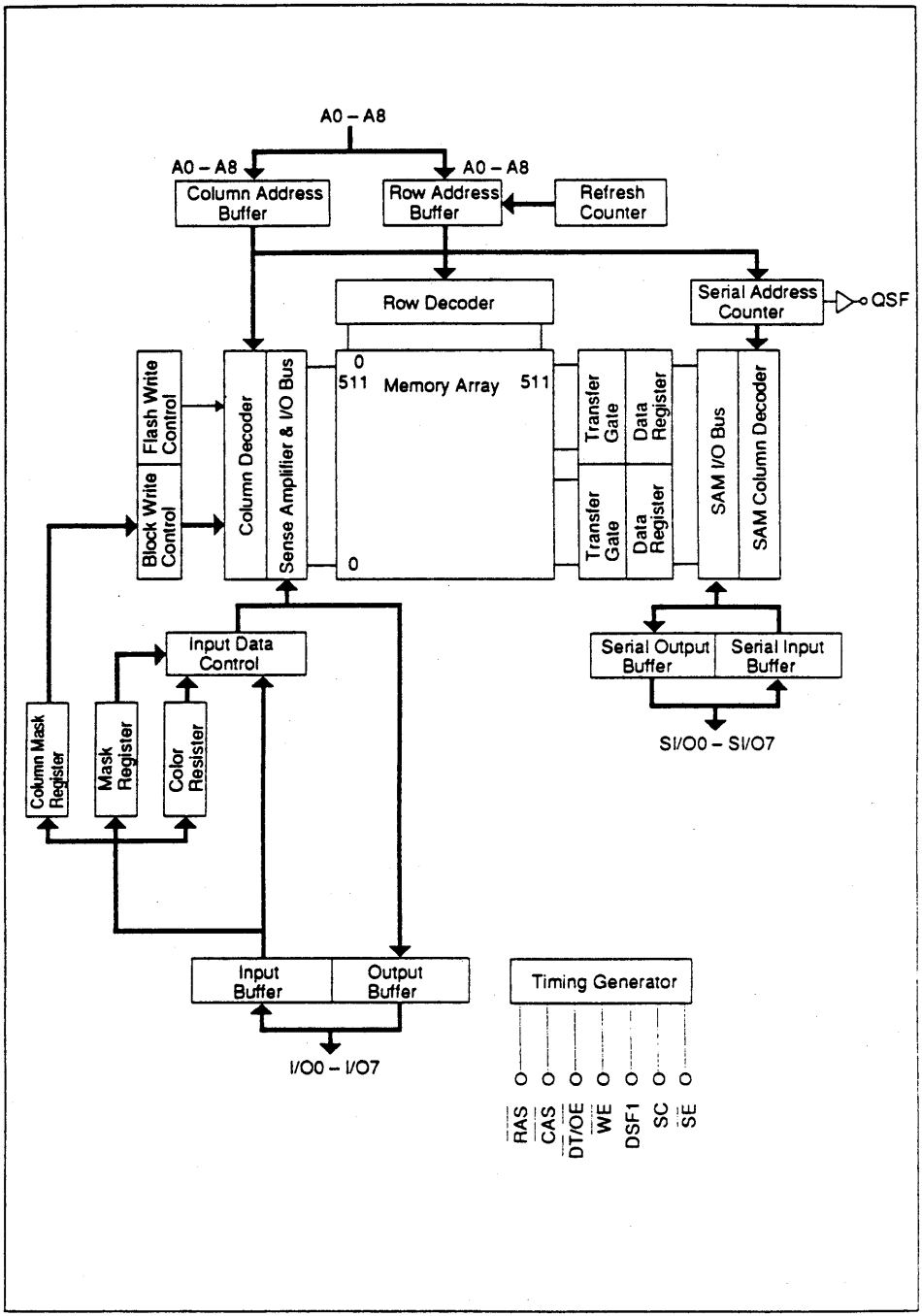
(Top view)

HM538254RR Series



(Top view)

Block Diagram



Pin Functions

$\overline{RAS}$ (input pin): $\overline{RAS}$ is a basic RAM signal. It is active in low level and standby in high level. Row address and signals as shown in table 1 are input at the falling edge of $\overline{RAS}$. The input level of these signals determine the operation cycle of the HM538254.

Table 1. Operation Cycles of the HM538254

Mnemonic Code	$\overline{RAS}$					$\overline{CAS}$		Address		I/On Input	
	$\overline{CAS}$	DT/$\overline{OE}$	$\overline{WE}$	DSF1	DSF2	DSF1	DSF2	$\overline{RAS}$	$\overline{CAS}$	$\overline{RAS}$	$\overline{CAS}$/$\overline{WE}$
CBRS	0	–	0	1	0	–	0	Stop	–	–	–
CBRR	0	–	1	0	0	–	0	–	–	–	–
CBRN	0	–	1	1	0	–	0	–	–	–	–
MWT	1	0	0	0	0	–	0	Row	TAP	WM	–
MSWT	1	0	0	1	0	–	0	Row	TAP	WM	–
RT	1	0	1	0	0	–	0	Row	TAP	–	–
SRT	1	0	1	1	0	–	0	Row	TAP	–	–
RWM	1	1	0	0	0	0	0	Row	Column	WM	Input data

Mnemonic Code	Write Mask	Pers W.M.	Register WM	Register Color	No.of Bndry	Function
CBRS	–	–	–	–	Set	CBR refresh with stop resister set
CBRR	–	Reset	Reset	–	Reset	CBR refresh with register reset
CBRN	–	–	–	–	–	CBR refresh (no reset)
MWT	Yes	No Yes	Load/use Use	–	–	Masked write transfer (new/old mask)
MSWT	Yes	No Yes	Load/use Use	–	Use	Masked split write transfer (new/old mask)
RT	–	–	–	–	–	Read transfer
SRT	–	–	–	–	Use	Split read transfer
RWM	Yes	No Yes	Load/use Use	–	–	Read/write (new/old mask)

Table 1. Operation Cycles of the HM538254 (cont)

Mnemonic	$\overline{RAS}$					$\overline{CAS}$		Address		I/On Input	
Code	$\overline{CAS}$	DT/$\overline{OE}$	$\overline{WE}$	DSF1	DSF2	DSF1	DSF2	$\overline{RAS}$	$\overline{CAS}$	$\overline{RAS}$	$\overline{CAS}$/$\overline{WE}$
BWM	1	1	0	0	0	1	0	Row	Column	WM	Column Mask
RW (No)	1	1	1	0	0	0	0	Row	Column	–	Input Data
BW (No)	1	1	1	0	0	1	0	Row	Column	–	Column Mask
FWM	1	1	0	1	0	–	0	Row	–	WM	–
LMR and Old Mask Set	1	1	1	1	0	0	0	(Row)	–	–	Mask Data
LCR	1	1	1	1	0	1	0	(Row)	–	–	Color
Option	0	0	0	0	0	–	0	Mode	–	Data	–

Mnemonic Code	Write Mask	Pers W.M.	Register WM	Register Color	No.of Bndry	Function
BWM	Yes	No Yes	Load/use Use	Use	–	Block write (new/old mask)
RW (No)	No	No	–	–	–	Read/write (no mask)
BW (No)	No	No	–	Use	–	Block write (no mask)
FWM	Yes	No Yes	Load/use Use	Use	–	Masked flash write (new/old mask)
LMR and Old Mask Set	–	Set	Load	–	–	Load mask register and old mask set
LCR	–	–	–	Load	–	Load color resister set
Option	–	–	–	–	–	–

Notes: 1. With CBRS, all SAM operations use stop register.
2. After LMR, RWM, BWM, FWM, MWT, and MSWT, use old mask which can be reset by CBRR.
3. DSF2 is fixed low in all operation. (for the addition of operation mode in future)

$\overline{CAS}$ (input pin): Column address and DSF1 signals are fetched into chip at the falling edge of $\overline{CAS}$, which determines the operation mode of the HM538254.

A0 – A8 (input pins): Row address (AX0 – AX8) is determined by A0 – A8 level at the falling edge of $\overline{RAS}$. Column address (AY0 – AY8) is determined by A0 – A8 level at the falling edge of $\overline{CAS}$. In transfer cycles, row address is the address on the word line which transfers data with SAM data register, and column address is the SAM start address after transfer.

$\overline{WE}$ (input pin): $\overline{WE}$ pin has two functions at the falling edge of $\overline{RAS}$ and after. When $\overline{WE}$ is low at the falling edge of $\overline{RAS}$, the HM538254 turns to mask write mode. According to the I/O level at the time, write on each I/O can be masked. ($\overline{WE}$ level at the falling edge of $\overline{RAS}$ is don't care in read cycle.) When $\overline{WE}$ is high at the falling edge of $\overline{RAS}$, a no mask write cycle is executed. After that, $\overline{WE}$ switches read/write cycles. In a transfer cycle, the direction of transfer is determined by $\overline{WE}$ level at the falling edge of $\overline{RAS}$. When $\overline{WE}$ is low, data is transferred from SAM to RAM (data is written into RAM), and when $\overline{WE}$ is high, data is transferred from RAM to SAM (data is read from RAM).

I/O0 – I/O7 (input/output pins): I/O pins function as mask data at the falling edge of $\overline{RAS}$ (in mask write mode). Data is written only to high I/O pins. Data on low I/O pins are masked and internal data are retained. After that, they function as inut/output pins as those of a standard DRAM. In block write cycle, they function as column mask data at the falling edges of $\overline{CAS}$ and $\overline{WE}$.

$\overline{DT}/\overline{OE}$ (input pin): $\overline{DT}/\overline{OE}$ pin functions as $\overline{DT}$ (data transfer) pin at the falling edge of $\overline{RAS}$ and as $\overline{OE}$ (output enable) pin after that. When $\overline{DT}$ is low at the falling edge of $\overline{RAS}$, this cycle becomes a transfer cycle. When $\overline{DT}$ is high at the falling edge of $\overline{RAS}$, RAM and SAM operate independently.

SC (input pin): SC is a basic SAM clock. In a serial read cycle, data outputs from an SI/O pin synchronously with the rising edge of SC. In a serial write cycle, data on an SI/O pin at the rising edge of SC is fetched into the SAM data register.

$\overline{SE}$ (input pin): $\overline{SE}$ pin activates SAM. When $\overline{SE}$ is high, SI/O is in the high impedance state in serial read cycle and data on SI/O is not fetched into the SAM data register in serial write cycle. $\overline{SE}$ can be used as a mask for serial write because the internal pointer is incremented at the rising edge of SC.

SI/O0 – SI/O7 (input/output pins): SI/Os are input/output pins in SAM. Direction of input/output is determined by the previous transfer cycle. When it was a read transfer cycle, SI/O outputs data. When it was a masked write transfer cycle, SI/O inputs data.
DSF1 (input pin): DSF1 is a special function data input flag pin. It is set to high at the falling edge of $\overline{RAS}$ when new functions such as color register and mask register read/write, split transfer, and flash write, are used.

DSF2 (input pin): DSF2 is also a special function data input flag pin. This pin is fixed to low level in all operations of the HM538254.

QSF (output pin): QSF outputs data of address A8 in SAM. QSF is switched from low to high by accessing address 255 in SAM and from high to low by accessing address 511 in SAM.

Operation of HM538254

RAM Port Operation

RAM Read Cycle ($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high and DSF1 low at the falling edge of $\overline{RAS}$, DSF1 low at the falling edge of $\overline{CAS}$)

Row address is entered at the $\overline{RAS}$ falling edge and column address at the $\overline{CAS}$ falling edge to the device as in standard DRAM. Then, when $\overline{WE}$ is high and $\overline{DT}/\overline{OE}$ is low while $\overline{CAS}$ is low, the selected address data outputs through I/O pin. At the falling edge of $\overline{RAS}$, $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ become high to distinguish RAM read cycle from transfer cycle and CBR refresh cycle. Address access time (t_{AA}) and $\overline{RAS}$ to column address delay time (t_{RAD}) specifications are added to enable hyper page mode.

RAM Write Cycle (Eraly Write, Delayed Write, Read-Modify-Write)
($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high and DSF1 low at the falling edge of $\overline{RAS}$, DSF1 low at the falling edge of $\overline{CAS}$)

• No Mask Write Cycle ($\overline{WE}$ high at the falling edge of $\overline{RAS}$)
When $\overline{CAS}$ is set low and $\overline{WE}$ is set low after $\overline{RAS}$ low, a write cycle is executed.
If $\overline{WE}$ is set low before the $\overline{CAS}$ falling edge, this cycle becomes an early write cycle and all I/O become in high impedance.
If $\overline{WE}$ is set low after the $\overline{CAS}$ falling edge, this cycle becomes a delayed write cycle. I/O does not become high impedance in this cycle, so data should be entered with $\overline{OE}$ in high.
If $\overline{WE}$ is set low after t_{CWD} (min) and t_{AWD} (min) after the $\overline{CAS}$ falling edge, this cycle becomes a read-modify-write cycle and enables read/write at the same address in one cycle. In this cycle also, to avoid I/O contention, data should be input after reading data and driving $\overline{OE}$ high.

• Mask Write Mode ($\overline{WE}$ low at the falling edge of $\overline{RAS}$)
If $\overline{WE}$ is set low at the falling edge of $\overline{RAS}$, two modes of mask write cycle are capable.
1. In new mask mode, mask data is loaded from I/O pin and used. Whether or not an I/O is written depends on I/O level at the falling edge of $\overline{RAS}$. The data is written in high level I/Os, and the data is masked and retained in low level I/Os. This mask data is effective during the $\overline{RAS}$ cycle. So, in page mode cycles the mask data is retained during the page access.
2. If a load mask register cycle (LMR) has been performed, the mask data is not loaded from I/O pins and the mask data stored in mask registers persistently are used. This operation is known as persistent write mask, set by LMR cycle and reset by CBRR cycle.

Hyper Page Mode Cycle ($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high and DSF1 low at the falling edge of $\overline{RAS}$)

Hyper page mode cycle reads/writes the data of the same row address at high speed by toggling $\overline{CAS}$ while $\overline{RAS}$ is low. Its cycle time is one forth of the random read/write cycle. In this cycle, read, write, and block write cycles can be mixed. Note that address access time (t_{AA}), $\overline{RAS}$ to column address delay time (t_{RAD}), and access time from $\overline{CAS}$ precharge (t_{ACP}) are added. Column address is latched by $\overline{CAS}$ low edge triger, access time from $\overline{CAS}$ is determined by t_{CAC} (t_{AA} from column address, t_{ACP} from $\overline{CAS}$ high edge). Dout data is held during $\overline{CAS}$ high and is sustained until next Dout. Data output enable/disable is controlled by $\overline{DT}/\overline{OE}$ and when both $\overline{RAS}$ and $\overline{CAS}$ become high, Data output become High-Z. In one $\overline{RAS}$ cycle, 512-word memory cells of the same row address can be accessed. It is necessary to specify access frequency within t_{RASP} max (100 μs).

Color Register Set/Read Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ high, $\overline{WE}$ high and DSF1 high at the falling edge of $\overline{RAS}$)

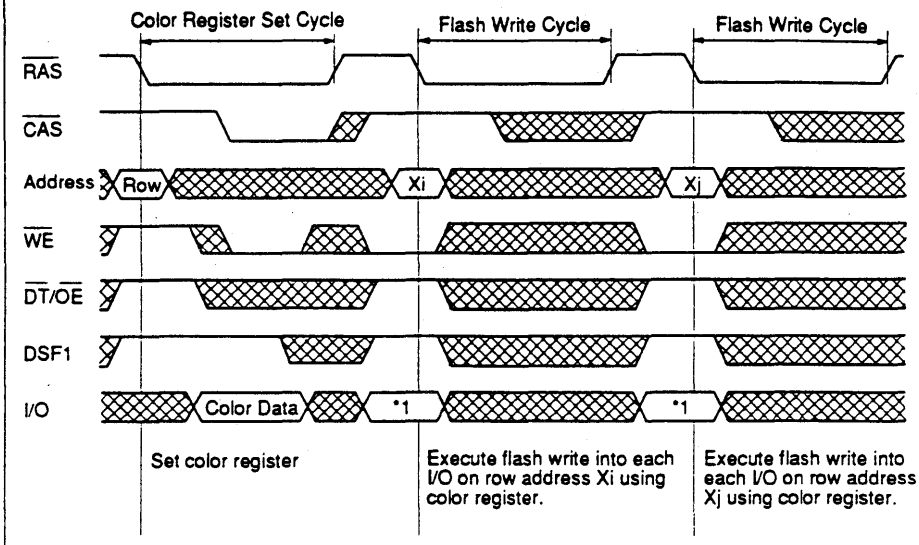
In color register set cycle, color data is set to the internal color register used in flash write cycle or block write cycle. 8 bits of internal color register are provided at each I/O. This register is composed of static circuits, so once it is set, it retains the data until reset. Since color register set cycle is just as same as the usual read and write cycle, so read, early write and delayed write cycle can be executed. In this cycle, the HM538253 refreshes the row address fetched at the falling edge of $\overline{RAS}$.

Mask Register Set/Read Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ high, $\overline{WE}$ high, and DSF1 high at the falling edge of $\overline{RAS}$)

In mask register set cycle, mask data is set to the internal mask register used in mask write cycle, block write cycle, flash write cycle, masked write transfer, and masked split write transfer. 8 bits of internal mask register are provided at each I/O. This mask register is composed of static circuits, so once it is set, it retains the data until next mask register set or reset (CBRR). Since mask register set cycle is just as same as the usual read and write cycle, so read, early write and delayed write cycle can be executed.

Flash Write Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ high, $\overline{WE}$ low, and DSF1 high at the falling edge of $\overline{RAS}$)

In a flash write cycle, a row of data (512 word x 8 bit) is cleared to 0 or 1 at each I/O according to the data of color register mentioned before. It is also necessary to mask I/O in this cycle. When $\overline{CAS}$ and $\overline{DT}/\overline{OE}$ is set high, $\overline{WE}$ is low, and DSF1 is high at the falling edge of $\overline{RAS}$, this cycle starts. Then, the row address to clear is given to row address. Mask data is as same as that of a RAM write cycle. Cycle time is the same as those of RAM read/write cycles, so all bits can be cleared in 1/512 of the usual cycle time. (See figure 1.)



*1 I/O Mask Data (In new mask mode)
Low: Mask
High: Non Mask
In persistent mask mode, I/O don't care

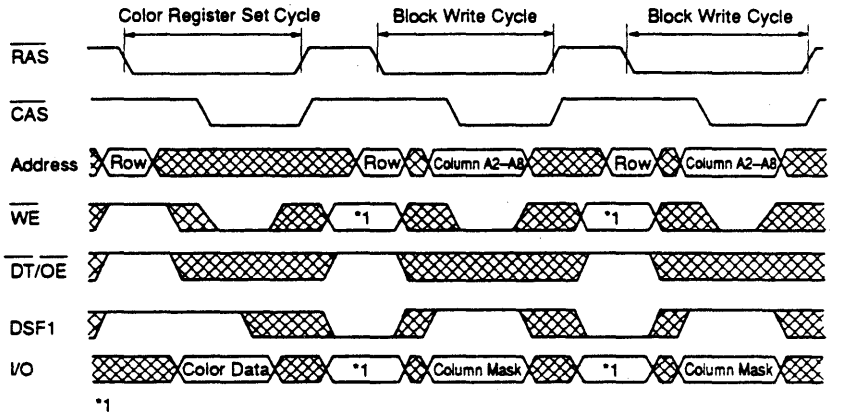
Figure 1 Use of Flash Write

Block Write Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ high and DSF1 low at the falling edge of $\overline{RAS}$, DSF1 high and $\overline{WE}$ low at the falling edge of $\overline{CAS}$)

In a block write cycle, 4 columns of data (4 column x 8 bit) are cleared to 0 or 1 at each I/O according to the data of color register. Column addresses A0 and A1 are disregarded. The mask data on I/Os and the mask data on column addresses can be determined independently. I/O level at the falling edge of $\overline{CAS}$ determines the address to be cleared. (See Figure 2.) The block write cycle is as the same as the usual write cycle, so early and delayed write, read-modify-write, and page mode write cycle can be executed.

• No mask Mode Block Write Cycle ($\overline{WE}$ high at the falling edge of $\overline{RAS}$)
The data on 8 I/Os are all cleared when $\overline{WE}$ is high at the falling edge of $\overline{RAS}$.

• Mask Block Write Cycle ($\overline{WE}$ low at the falling edge of $\overline{RAS}$)
When $\overline{WE}$ is low at the falling edge of $\overline{RAS}$, the HM538254 starts mask block write cycle to clear the data on an optional I/O. The mask data is the same as that of a RAM write cycle. High I/O is cleared, low I/O is not cleared and the internal data is retained. In new mask mode, the mask data is available in the $\overline{RAS}$ cycle. In persistent mask mode, I/O don't care about mask mode.



*1

$\overline{WE}$	Mode	I/O data/$\overline{RAS}$
Low	New Mask Mode	Mask
	Persistent Mask Mode	Don't care (mask register used)
High	No mask	Don't care

I/O Mask Data (In new mask mode)
Low: Mask
High: Non Mask
In persistent mask mode, I/O don't care

Column Mask Data

I/O0	Column0 (A0 = 0, A1 = 0) Mask Data	Low: Mask
I/O1	Column1 (A0 = 1, A1 = 0) Mask Data	
I/O2	Column2 (A0 = 0, A1 = 1) Mask Data	
I/O3	Column3 (A0 = 1, A1 = 1) Mask Data	High: Non Mask

Figure 2 Use of Block Write

Transfer Operation

The HM538254 provides the read transfer cycle, split read transfer cycle, masked write transfer cycle and masked split write transfer cycle as data transfer cycles. Theses transfer cycles are set by driving $\overline{CAS}$ high and $\overline{DT/OE}$ low at the falling edge of $\overline{RAS}$. They have following functions:
(1) Transfer data between row address and SAM data register
Read transfer cycle and split read transfer cycle: RAM to SAM
Masked write transfer cycle and masked split write transfer cycle: SAM to RAM
(2) Determine SI/O state (except for split read transfer cycle and masked split write transfer cycle)
Read transfer cycle: SI/O output
Masked write transfer cycle: SI/O input
(3) Determine first SAM address to access after transferring at column address (SAM start address).
SAM start address must be determined by read transfer cycle or masked write transfer cycle (split transfer cycle isn't available)before SAM access, after power on, and determined for each transfer cycle.
(4) Use the stopping columns (boundaries) in the serail shift register. If the stopping columns have been set, split transfer cycles use the stopping columns, but any boundaries cannot be set as the start address.
(5) Load/use mask data in masked write transfer cycle and masked split write transfer cycle.

Read Transfer Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ low, $\overline{WE}$ high and DSF1 low at the falling edge of $\overline{RAS}$)

This cycle becomes read transfer cycle by driving $\overline{DT/OE}$ low, $\overline{WE}$ high and DSF1 low at the falling edge of $\overline{RAS}$. The row address data (512 x 8 bits) determined by this cycle is transferred to SAM data register synchronously at the rising edge of $\overline{DT/OE}$. After the rising edge of $\overline{DT/OE}$, the new address data outputs from SAM start address determined by column address. In read transfer cycle, $\overline{DT/OE}$ must be risen to transfer data from RAM to SAM.
This cycle can access SAM even during transfer (real time read transfer). In this case, the timing t_{SDD} (min) specified between the last SAM access before transfer and $\overline{DT/OE}$ rising edge and t_{SDH} (min) specified between the first SAM access and $\overline{DT/OE}$ rising edge must be satisfied. (See figure 3.)
When read transfer cycle is executed, SI/O becomes output state by first SAM access. Input must be set high impedance before t_{SZS} (min) of the first SAM access to avoid data contention.

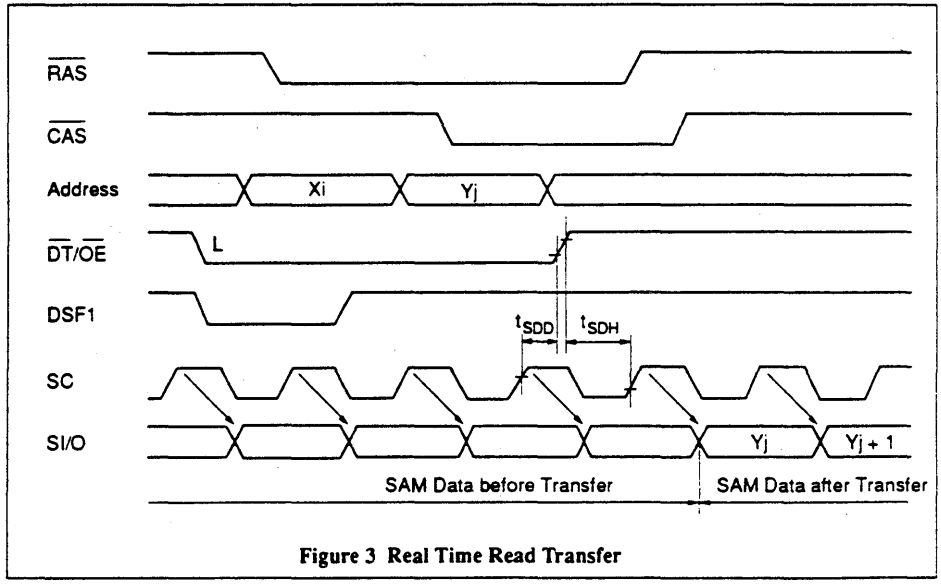


Figure 3 Real Time Read Transfer

Masked Write Transfer cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ low, $\overline{WE}$ low, and DSF1 low at the falling edge of $\overline{RAS}$)

Masked write transfer cycle can transfer only selected I/O data in a row of data input by serial write cycle to RAM. Whether SAM data is transferred or not depends on the corresponding I/O level (mask data) at the falling edge of $\overline{RAS}$. This mask transfer operation is the same as a mask write operation in RAM cycles, so the persistent mode can be supported. The row address of data transferred into RAM is determined by the address at the falling edge of $\overline{RAS}$. The column address is specified as the first address for serial write after terminating this cycle. Also in this cycle, SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. SAM access is inhibited during $\overline{RAS}$ low. In this period, SC must bot be risen. Data transferred to SAM by read transfer cycle or split read transfer cycle can be written to other addreses of RAM by write transfer cycle. However, the adddress to write data must be the same as that of the read transfer cycle or the split read transfer cycle (row address AX8)

Split Read Transfer Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ low, $\overline{WE}$ high and DSF1 high at the falling edge of $\overline{RAS}$)

To execute a continuous serial read by real time read transfer, the HM538254 must satisfy SC and $\overline{DT/OE}$ timings and requires an external circuit to detect SAM last address. Split read transfer cycle makes it possible to execute a continuous serial read without the above timing limitation.

The HM538254 supports two types of split register operation. One is the normal split register operation to split the data register into two halves. The other is the boundary split register operation using stopping columns described later.

Figure 4 shows the block diagram for the normal split register operation. SAM data register (DR) consists of 2 split buffers, whose organizations are 256-word x 8-bit each. Let us suppose that data is read from upper data reagister DR1 (The row address AX8 is 0 and SAM address A8 is 1.). When split read transfer is executed setting row address AX8 to 0 and SAM start addresses A0 to A7, 256-word x 8-bit data are transferred from RAM to the lower data register DR0 (SAM address A8 is 0) automatically. After data are read from data register DR1, data start to be read from SAM start addresses of data register DR0. If the next split read transfer isn't executed while data are read from data register DR0, data start to be read from SAM start address 0 of DR1 after data are read from data register DR0. If split read transfer is executed setting row address AX8 to 1 and SAM start addresses A0 to A7 while data are read from data register DR1, 256-word x 8-bit data are transferred to data register DR2. After data are read from data register DR1, data start to be read from SAM start addresses of data register DR2. If the next split read transfer isn't executed while data is read from data register DR2, data start to be read from SAM start address 0 of data register DR1 after data are read from data register DR2. In split read data transfer, the SAM start address A8 is automatically set in the data register, which isn't used.

The data on SAM address A8, which will be accessed next, outputs to QSF, QSF is switched from low to high by accessing SAM last address 255 and from high to low by accessing address 511.

Split read transfer cycle is set when $\overline{CAS}$ is high, $\overline{DT/OE}$ is low, $\overline{WE}$ is high and DSF1 is high at the falling edge of $\overline{RAS}$. The cycle can be executed asyncronously with SC. However, HM538254 must be satisfied tSTS (min) timing specified between SC rising (Boundary address) and $\overline{RAS}$ falling. In split transfer cycle, the HM538254 must satisfy t_{RST} (min), t_{CST} (min) and t_{AST} (min) timings specified between $\overline{RAS}$ or $\overline{CAS}$ falling and column address. (See figure 5.)

In split read transfer, SI/O isn't switched to output state. Therefore, read transfer must be executed to switch SI/O to output state when the previous transfer cycle is masked write transfer cycle or masked split write transfer cycle, or power on. SAM start address must be set in every split read transfer cycle.

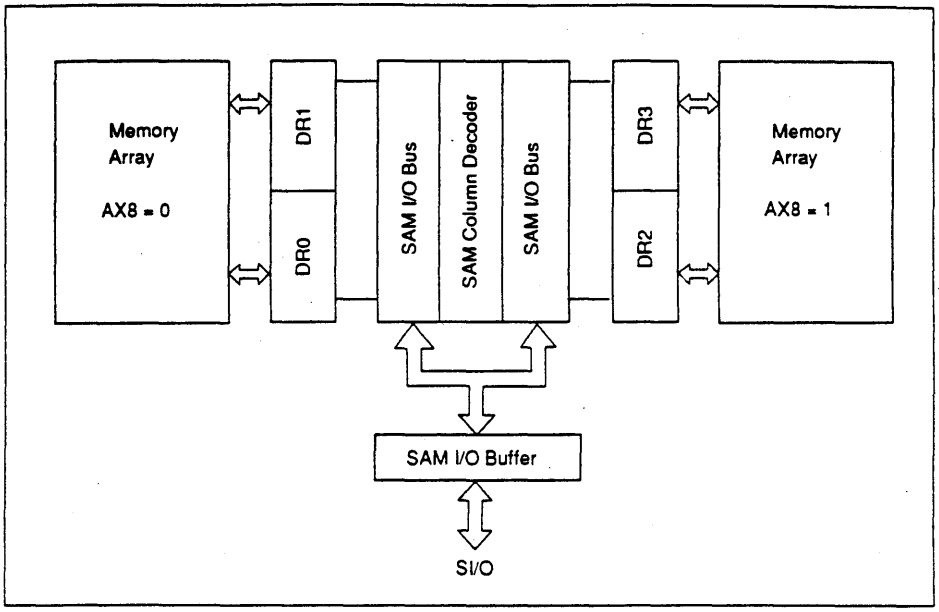
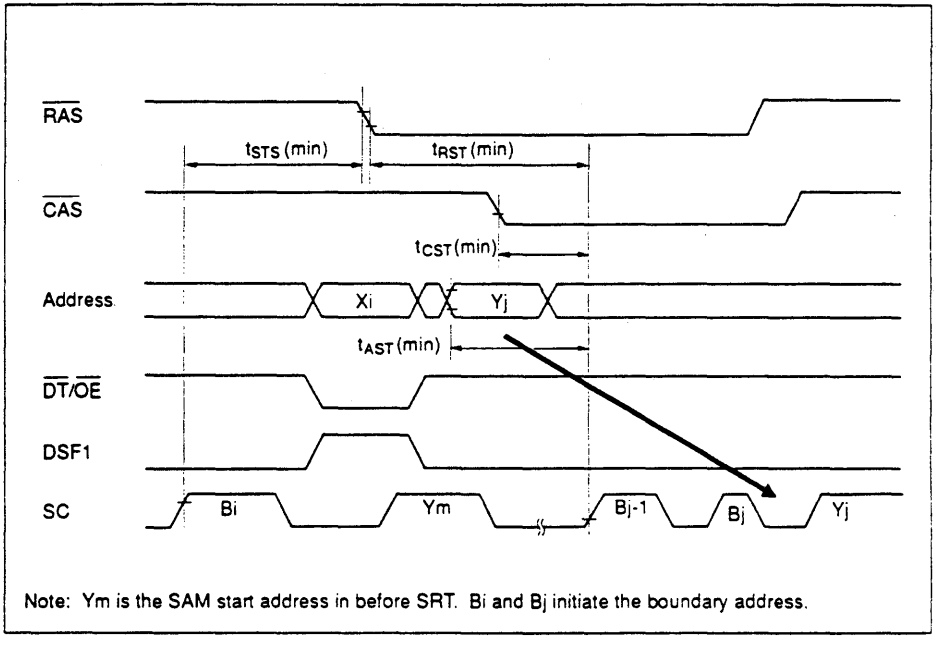


Figure 4 Block Diagram for Split Transfer



Note: Ym is the SAM start address in before SRT. Bi and Bj initiate the boundary address.

Figure 5 Limitation in Split Transfer

Masked Split Write Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low and DSF1 high at the falling edge of $\overline{RAS}$)

A continuous serial write cannot be executed because accessing SAM is inhibited during $\overline{RAS}$ low in write transfer. Masked split write transfer cycle makes it possible. In this cycle, t_{STS} (min), t_{RST} (min), t_{CST} (min) and t_{AST} (min) timings must be satisfied like split read transfer cycle. And it is impossible to switch SI/O to input state in this cycle. If SI/O is in output state, masked write transfer cycle should be executed to switch SI/O into input state. Data transferred to SAM by read transfer cycle or split read transfer cycle can be written to other addresses of RAM by masked split write transfer cycle. However masked write transfer cycle must be executed before masked split write transfer cycle. And in this masked split write transfer cycle, the MSB of row address (AX8) to write data must be the same as that of the read transfer cycle or the split read transfer cycle. In this cycle, the boundary split register operation using stopping columns is capable like split read transfer cycle.

Stopping Column in Split Transfer Cycle

The HM538254 has the boundary split register operation using stopping columns. If a CBRS cycle has been performed, split transfer cycle performs the boundary operation. Figure 6 shows an example of boundary split register. (Boundary code is B7.)
First of all a read transfer cycle is executed, and SAM start addresses A0 to A8 are set. The RAM data are transferred to the SAM, and SAM serial read starts from the start address (Y1) on the lower SAM. After that, a split read transfer cycle is executed, and the next start address (Y2) is set. The RAM data are transferred to the upper SAM. When the serial read arrive at the first boundary after the split read transfer cycle, the next read jumps to the start address (Y2) on the upper SAM (jump 1) and continues. Then the second split read transfer cycle is executed, and another start address (Y3) is set. The RAM data are transferred to the lower SAM. When the serial read arrive at the other boundary again, the next read jumps to the start address (Y3) on the lower SAM. In stopping column, split transfer is needed for jump operation between lower SAM and upper SAM.

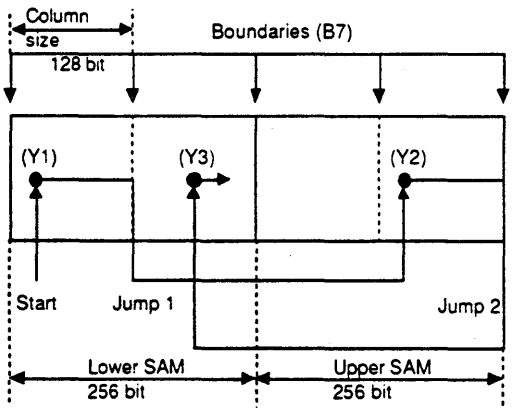


Figure 6 Example of Boundary Split Register

Stopping Column Set Cycle (CBRS)

This cycle becomes stopping column set cycle by driving $\overline{CAS}$ low, $\overline{WE}$ low, DSF1 high at the falling edge of $\overline{RAS}$. Stopping column data (boundaries) are latched from address inputs on the falling edge of $\overline{RAS}$. To determine the boundary, A2 to A7 can be used and don't care A0, A1, and A8. In the HM538254, 7 types of boundary (B2 to B8) can be set including the default case. (See stopping column boundary table.) If A2 to A6 are set to high and A7 is set to low, the boundaries (B7) are selected. Figure 6 shows the example. The stop address that is set by the CBRS is used from next split transfer cycle. Once a CBRS is executed, the stopping column operation mode continues until CBRR.

Stopping Column Boundary Table

		Stop Address					
Boundary code	Column size	A2	A3	A4	A5	A6	A7
B2	4	0	*	*	*	*	*
B3	8	1	0	*	*	*	*
B4	16	1	1	0	*	*	*
B5	32	1	1	1	0	*	*
B6	64	1	1	1	1	0	*
B7	128	1	1	1	1	1	0
B8	256	1	1	1	1	1	1

Notes: 1.A0, A1, and A8: don't care
2.*: don't care

Register Reset Cycle (CBRR)

This cycle becomes register reset cycle (CBRR) by driving $\overline{CAS}$ low, $\overline{WE}$ high, and DSF1 low at the falling edge of $\overline{RAS}$. A CBRR can reset the persistent mask operation and stopping column operation, so the HM538254 become the new mask operation and boundary code B8. When a CBRR is executed for stopping column operation reset and split transfer operation, it needs to satisfy t_{STS} (min) and t_{RST} (min) between $\overline{RAS}$ falling and SC rising for correct SAM read/write operation.

No Reset CBR Cycle (CBRN)

This cycle becomes no reset CBR cycle (CBRN) by driving $\overline{CAS}$ low, $\overline{WE}$ high and DSF1 high at the falling edge of $\overline{RAS}$. The CBRN can only execute the refresh operation.

SAM Port Operation

Serial Read Cycle

SAM port is in read mode when the previous data transfer cycle is a read transfer cycle. Access is synchronized with SC rising, and SAM data is output from SI/O. When $\overline{SE}$ is set high, SI/O becomes high impedance, and the internal pointer is incremented by the SC rising. After indicating the last address (address 511), the internal pointer indicates address 0 at the next access.

Serial Write Cycle

If previous data transfer cycle is masked write transfer cycle, SAM port goes into write mode. In this cycle, SI/O data is fetched into data register at the SC rising edge like in the serial read cycle. If $\overline{SE}$ is high, SI/O data isn't fetched into data register. The internal pointer is incremented by the SC rising, so $\overline{SE}$ high can be used as mask data for SAM. After indicating the last address (address 511), the internal pointer indicates address 0 at the next access.

Refresh

RAM Refresh

RAM, which is composed of dynamic circuits, requires refresh cycle to retain data. Refresh is executed by accessing all 512 row addresses within 8 ms. There are three refresh cycles: (1) $\overline{RAS}$-only refresh cycle, (2) $\overline{CAS}$-before-$\overline{RAS}$ (CBRN, CBRS, and CBRR) refresh cycle, and (3) Hidden refresh cycle. Besides them, the cycles which activate $\overline{RAS}$, such as read/write cycles or transfer cycles, can also refresh the row address. Therefore, no refresh cycle is required when all row addresses are accessed within 8 ms.

(1) $\overline{RAS}$-Only Refresh Cycle: $\overline{RAS}$-only refresh cycle is executed by activating only the $\overline{RAS}$ cycle with $\overline{CAS}$ fixed to high after inputting the row address (= refresh address) from external circuits. To distinguish this cycle from a data transfer cycle, $\overline{DT}/\overline{OE}$ must be high at the falling edge of $\overline{RAS}$.

(2) CBR Refresh Cycle: CBR refresh cycle (CBRN, CBRS and CBRR) are set by activating $\overline{CAS}$ before $\overline{RAS}$. In this cycle, the refresh address need not to be input through external circuits because it is input through an internal refresh counter. In this cycle, output is in high impedance and power dissipation is lowered because $\overline{CAS}$ circuits don't operate.

(3) Hidden Refresh Cycle: Hidden refresh cycle executes CBR refresh with the data output by reactivating $\overline{RAS}$ when $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ keep low in normal RAM read cycles. In the mask register read cycle and the color register read cycle, Dout data guaranteed while $\overline{RAS}$ and $\overline{CAS}$ are low, and so after the mask register read cycle or the color register read cycle is performed, in hidden refresh cycle Dout data is not guaranteed.

SAM Refresh

SAM parts (data register, shift resister and selector), organized as fully static circuitry, require no refresh.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	−0.5 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{CC}	4.5	5.0	5.5	V	1
Input high voltage	V_{IH}	2.4	—	6.5	V	1
Input low voltage	V_{IL}	−0.5*2	—	0.8	V	1

Notes: 1. All voltage referenced to V_{SS}
2 −3.0 V for pulse width ≤ 10 ns.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

		HM538254-7		HM538254-8		HM538254-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**
Operating current	I_{CC1}	—	110	—	100	—	90	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min; SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC7}	—	165	—	150	—	140	mA	$\overline{SE}$ = V_{IL}, SC cycling, t_{SCC} = min
Block write current*3	I_{CC1BW}	—	115	—	105	—	90	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min; SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC7BW}	—	170	—	155	—	140	mA	$\overline{SE}$ = V_{IL}, SC cycling, t_{SCC} = min
Standby current	I_{CC2}	—	7	—	7	—	7	mA	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}; SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC8}	—	65	—	60	—	55	mA	$\overline{SE}$ = V_{IL}, SC cycling, t_{SCC} = min
$\overline{RAS}$-only refresh current	I_{CC3}	—	110	—	100	—	90	mA	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC9}	—	165	—	150	—	135	mA	t_{RC} = min; $\overline{SE}$ = V_{IL}, SC cycling, t_{SCC} = min
Hyper page mode current	I_{CC4}	—	130	—	120	—	110	mA	$\overline{CAS}$ cycling, $\overline{RAS}$ = V_{IL}; SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC10}	—	185	—	170	—	160	mA	t_{PC} = min; $\overline{SE}$ = V_{IL}, SC cycling, t_{SCC} = min
Hyper page mode block write current*3	I_{CC4BW}	—	155	—	140	—	130	mA	$\overline{CAS}$ cycling, $\overline{RAS}$ = V_{IL}; SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC10BW}	—	210	—	190	—	175	mA	t_{PC} = min; $\overline{SE}$ = V_{IL}, SC cycling, t_{SCC} = min
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC5}	—	85	—	75	—	65	mA	$\overline{RAS}$ cycling, t_{RC} = min; SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC11}	—	140	—	130	—	120	mA	$\overline{SE}$ = V_{IL}, SC cycling, t_{SCC} = min
Data transfer current	I_{CC6}	—	130	—	115	—	100	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min; SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC12}	—	180	—	165	—	145	mA	$\overline{SE}$ = V_{IL}, SC cycling, t_{SCC} = min
Input leakage current	I_{LI}	−10	10	−10	10	−10	10	µA	0 V ≤ Vin ≤ 7 V
Output leakage current	I_{LO}	−10	10	−10	10	−10	10	µA	0 V ≤ Vin ≤ 7 V Dout, Sout = disable
Output high voltage	V_{OH}	2.4	—	2.4	—	2.4	—	V	I_{OH} = −1 mA
Output low voltage	V_{OL}	—	0.4	—	0.4	—	0.4	V	I_{OL} = 2.1 mA

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed once while $\overline{RAS}$ is low and $\overline{CAS}$ is high.
3. Address can be changed once in 1 page cycle (t_{PC}).

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 10%, f = 1 MHz, Bias: Clock, I/O = V_{CC}, address = V_{SS})

Parameter	Symbol	Typ	Max	Unit	Note
Input capacitance (Address)	C_{I1}	—	5	pF	1
Input capacitance (Clocks)	C_{I2}	—	5	pF	1
Output capacitance (I/O, SI/O, QSF)	$C_{I/O}$	—	7	pF	1

Notes: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V) *1, *16

Test Conditions

- Input rise and fall times: 5 ns
- Input pulse levels: V_{SS} to 3.0 V
- Input timing reference levels: 0.8 V, 2.4 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: RAM 1TTL + CL (50 pF)
  SAM, QSF 1TTL + CL (30 pF)
  (Including scope and jig)

Common Parameter

		HM538254-7		HM538254-8		HM538254-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Random read or write cycle time	t_{RC}	130	—	150	—	180	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	50	—	60	—	70	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10000	80	10000	100	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	—	20	—	25	—	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	12	—	15	—	15	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	20	75	ns	2
$\overline{RAS}$ hold time referenced to $\overline{CAS}$	t_{RSH}	20	—	20	—	25	—	ns	
$\overline{CAS}$ hold time referenced to $\overline{RAS}$	t_{CSH}	70	—	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	10	—	ns	

Common Parameter (cont)

Parameter	Symbol	HM538254-7 Min	HM538254-7 Max	HM538254-8 Min	HM538254-8 Max	HM538254-10 Min	HM538254-10 Max	Unit	Notes
Transition time (rise to fall)	t_T	3	50	3	50	3	50	ns	3
DSF1 to $\overline{CAS}$ setup time	t_{FSC}	0	—	0	—	0	—	ns	
Refresh period	t_{REF}	—	8	—	8	—	8	ms	
$\overline{DT}$ to $\overline{RAS}$ setup time	t_{DTS}	0	—	0	—	0	—	ns	
$\overline{DT}$ to $\overline{RAS}$ hold time	t_{DTH}	10	—	10	—	10	—	ns	
DSF1 to $\overline{RAS}$ setup time	t_{FSR}	0	—	0	—	0	—	ns	
DSF1 to $\overline{RAS}$ hold time	t_{RFH}	10	—	10	—	10	—	ns	
DSF1 to $\overline{CAS}$ hold time	t_{CFH}	12	—	15	—	15	—	ns	
Data-in to $\overline{CAS}$ delay time	t_{DZC}	0	—	0	—	0	—	ns	4
Data-in to $\overline{OE}$ delay time	t_{DZO}	0	—	0	—	0	—	ns	4
Output buffer turn-off delay referenced to $\overline{OE}$	t_{OFF2}	—	15	—	20	—	20	ns	5

Read Cycle (RAM), Hyper Page Mode Read Cycle

		HM538254-7		HM538254-8		HM538254-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Access time from $\overline{RAS}$	t_{RAC}	—	70	—	80	—	100	ns	6, 7
Access time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	25	ns	7, 8
Access time from $\overline{OE}$	t_{OAC}	—	20	—	20	—	25	ns	7
Address access time	t_{AA}	—	35	—	40	—	45	ns	7, 9
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	0	—	ns	10
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0	—	5	—	10	—	ns	10
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	15	55	ns	2
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	—	40	—	45	—	ns	
Column address to $\overline{CAS}$ lead time	t_{CAL}	25	—	30	—	35	—	ns	
Hyper page mode cycle time	t_{PC}	35	—	40	—	45	—	ns	
Hyper page $\overline{CAS}$ precharge time	t_{CP}	5	—	10	—	10	—	ns	
Hyper page access time from $\overline{CAS}$ precharge	t_{ACP}	—	40	—	45	—	50	ns	
Hyper page mode $\overline{RAS}$ pulse width	t_{RASP}	70	100000	80	100000	100	100000		ns
Hyper page data out hold time	t_{DOH}	4	—	5	—	5	—	ns	
Data-out buffer turn-off time ($\overline{RAS}$)	t_{RHZ}	—	15	—	20	—	20	ns	5
Data-out buffer turn-off time ($\overline{CAS}$)	t_{CHZ}	—	15	—	20	—	20	ns	5

Write Cycle (RAM), Hyper Page Mode Write Cycle, Color Register Set Cycle

		HM538254-7		HM538254-8		HM538254-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	11
Write command hold time	t_{WCH}	12	—	15	—	15	—	ns	
Write command pulse width	t_{WP}	12	—	15	—	15	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	—	20	—	20	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	—	20	—	20	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	12
Data-in hold time	t_{DH}	12	—	15	—	15	—	ns	12
$\overline{WE}$ to $\overline{RAS}$ setup time	t_{WS}	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ hold time	t_{WH}	10	—	10	—	10	—	ns	
Mask data to $\overline{RAS}$ setup time	t_{MS}	0	—	0	—	0	—	ns	
Mask data to $\overline{RAS}$ hold time	t_{MH}	10	—	10	—	10	—	ns	
$\overline{OE}$ hold time referenced to $\overline{WE}$	t_{OEH}	15	—	20	—	20	—	ns	
Hyper page mode cycle time	t_{PC}	35	—	40	—	45	—	ns	
Hyper page $\overline{CAS}$ precharge time	t_{CP}	5	—	10	—	10	—	ns	
$\overline{CAS}$ to data-in delay time	t_{CDD}	15	—	20	—	20	—	ns	13
Hyper page mode $\overline{RAS}$ pulse width	t_{RASP}	70	100000	80	100000	100	100000	ns	

Read-Modify-Write Cycle

Parameter	Symbol	HM538254-7 Min	HM538254-7 Max	HM538254-8 Min	HM538254-8 Max	HM538254-10 Min	HM538254-10 Max	Unit	Notes
Read-modify-write cycle time	t_{RWC}	180	—	200	—	230	—	ns	
$\overline{RAS}$ pulse width (read-modify-write cycle)	t_{RWS}	120	10000	130	10000	150	10000	ns	
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	40	—	45	—	50	—	ns	14
Column address to $\overline{WE}$ delay time	t_{AWD}	60	—	65	—	70	—	ns	14
$\overline{OE}$ to data-in delay time	t_{ODD}	15	—	20	—	20	—	ns	12
Access time from $\overline{RAS}$	t_{RAC}	—	70	—	80	—	100	ns	6, 7
Access time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	25	ns	7, 8
Access time from $\overline{OE}$	t_{OAC}	—	20	—	20	—	25	ns	7
Address access time	t_{AA}	—	35	—	40	—	45	ns	7, 9
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	15	55	ns	
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	—	20	—	20	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	—	20	—	20	—	ns	
Write command pulse width	t_{WP}	12	—	15	—	15	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	12
Data-in hold time	t_{DH}	12	—	15	—	15	—	ns	12
$\overline{OE}$ hold time referenced to $\overline{WE}$	t_{OEH}	15	—	20	—	20	—	ns	

Refresh Cycle

Parameter	Symbol	HM538254-7 Min	HM538254-7 Max	HM538254-8 Min	HM538254-8 Max	HM538254-10 Min	HM538254-10 Max	Unit	Notes
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10	—	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	—	10	—	10	—	ns	

Flash Write Cycle, Block Write Cycle, and Register Read Cycle

		HM538254-7		HM538254-8		HM538254-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
$\overline{CAS}$ to data-in delay time	t_{CDD}	15	—	20	—	20	—	ns	13
$\overline{OE}$ to data-in delay time	t_{ODD}	15	—	20	—	20	—	ns	13
$\overline{RAS}$ to data-in delay time	t_{RDD}	20	—	20	—	20	—	ns	13

CBR Refresh with Register Reset

		HM538254-7		HM538254-8		HM538254-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Split transfer setup time	t_{STS}	20	—	20	—	25	—	ns	
Split transfer hold time referenced to $\overline{RAS}$	t_{RST}	70	—	80	—	100	—	ns	

Read Transfer Cycle

		HM538254-7		HM538254-8		HM538254-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
$\overline{DT}$ hold time referenced to $\overline{RAS}$	t_{RDH}	60	10000	65	10000	80	10000	ns	
$\overline{DT}$ hold time referenced to $\overline{CAS}$	t_{CDH}	20	—	20	—	25	—	ns	
$\overline{DT}$ hold time referenced to column address	t_{ADH}	25	—	30	—	30	—	ns	
$\overline{DT}$ precharge time	t_{DTP}	20	—	20	—	30	—	ns	
$\overline{DT}$ to $\overline{RAS}$ delay time	t_{DRD}	60	—	70	—	80	—	ns	
SC to $\overline{RAS}$ setup time	t_{SRS}	15	—	20	—	30	—	ns	
1st SC to $\overline{RAS}$ hold time	t_{SRH}	70	—	80	—	100	—	ns	
1st SC to $\overline{CAS}$ hold time	t_{SCH}	25	—	25	—	25	—	ns	
1st SC to column address hold time	t_{SAH}	40	—	45	—	50	—	ns	
Last SC to $\overline{DT}$ delay time	t_{SDD}	5	—	5	—	5	—	ns	
1st SC to $\overline{DT}$ hold time	t_{SDH}	10	—	13	—	15	—	ns	
$\overline{DT}$ to QSF delay time	t_{DQD}	—	30	—	35	—	35	ns	15

Read Transfer Cycle (cont)

		HM538254-7		HM538254-8		HM538254-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
QSF hold time referenced to $\overline{DT}$	t_{DQH}	5	—	5	—	5	—	ns	
Serial data-in to 1st SC delay time	t_{SZS}	0	—	0	—	0	—	ns	
Serial clock cycle time	t_{SCC}	25	—	28	—	30	—	ns	
SC pulse width	t_{SC}	5	—	10	—	10	—	ns	
SC precharge time	t_{SCP}	10	—	10	—	10	—	ns	
SC access time	t_{SCA}	—	20	—	23	—	25	ns	15
Serial data-out hold time	t_{SOH}	5	—	5	—	5	—	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	15	—	15	—	ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	15	55	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	—	40	—	45	—	ns	
$\overline{RAS}$ to QSF delay time	t_{RQD}	—	70	—	75	—	85	ns	15
$\overline{CAS}$ to QSF delay time	t_{CQD}	—	35	—	35	—	35	ns	15
QSF hold time referenced to$\overline{RAS}$	t_{RQH}	20	—	20	—	25	—	ns	
QSF hold time referenced to $\overline{CAS}$	t_{CQH}	5	—	5	—	5	—	ns	

Masked Write Transfer Cycle

		HM538254-7		HM538254-8		HM538254-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
SC setup time referenced to $\overline{RAS}$	t_{SRS}	15	—	20	—	30	—	ns	
$\overline{RAS}$ to SC delay time	t_{SRD}	20	—	25	—	25	—	ns	
Serial output buffer turn-off time referenced to $\overline{RAS}$	t_{SRZ}	10	30	10	35	10	50	ns	
$\overline{RAS}$ to serial data-in delay time	t_{SID}	30	—	35	—	50	—	ns	
$\overline{RAS}$ to QSF delay time	t_{RQD}	—	70	—	75	—	85	ns	15
$\overline{CAS}$ to QSF delay time	t_{CQD}	—	35	—	35	—	35	ns	15
QSF hold time referenced to $\overline{RAS}$	t_{RQH}	20	—	20	—	25	—	ns	
QSF hold time referenced to $\overline{CAS}$	t_{CQH}	5	—	5	—	5	—	ns	
Serial clock cycle time	t_{SCC}	25	—	28	—	30	—	ns	
SC pulse width	t_{SC}	5	—	10	—	10	—	ns	
SC precharge time	t_{SCP}	10	—	10	—	10	—	ns	
SC access time	t_{SCA}	—	20	—	23	—	25	ns	15
Serial data-out hold time	t_{SOH}	5	—	5	—	5	—	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	15	—	15	—	ns	

Split Read Transfer Cycle, Masked Split Write Transfer Cycle

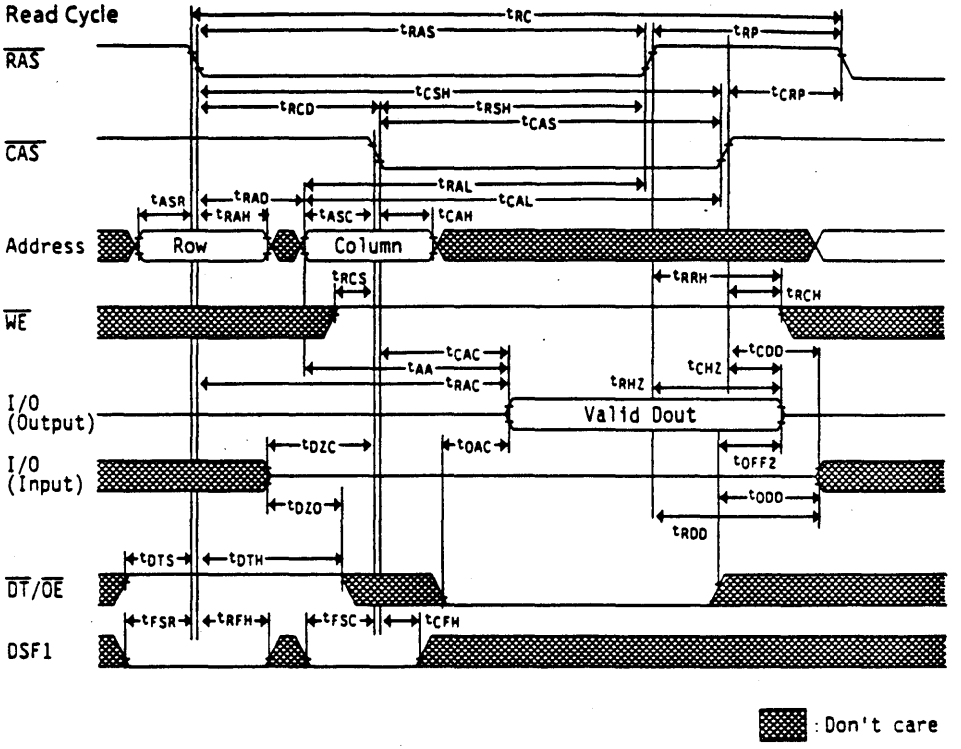
		HM538254-7		HM538254-8		HM538254-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Split transfer setup time	t_{STS}	20	—	20	—	25	—	ns	
Split transfer hold time referenced to $\overline{RAS}$	t_{RST}	70	—	80	—	100	—	ns	
Split transfer hold time referenced to $\overline{CAS}$	t_{CST}	20	—	20	—	25	—	ns	
Split transfer hold time referenced to column address	t_{AST}	35	—	40	—	45	—	ns	
SC to QSF delay time	t_{SQD}	—	30	—	30	—	30	ns	15
QSF hold time referenced to SC	t_{SQH}	5	—	5	—	5	—	ns	
Serial clock cycle time	t_{SCC}	25	—	28	—	30	—	ns	
SC pulse width	t_{SC}	5	—	10	—	10	—	ns	
SC precharge time	t_{SCP}	10	—	10	—	10	—	ns	
SC access time	t_{SCA}	—	20	—	23	—	25	ns	15
Serial data-out hold time	t_{SOH}	5	—	5	—	5	—	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	15	—	15	—	ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	15	55	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	—	40	—	45	—	ns	

Serial Read Cycle, Serial Write Cycle

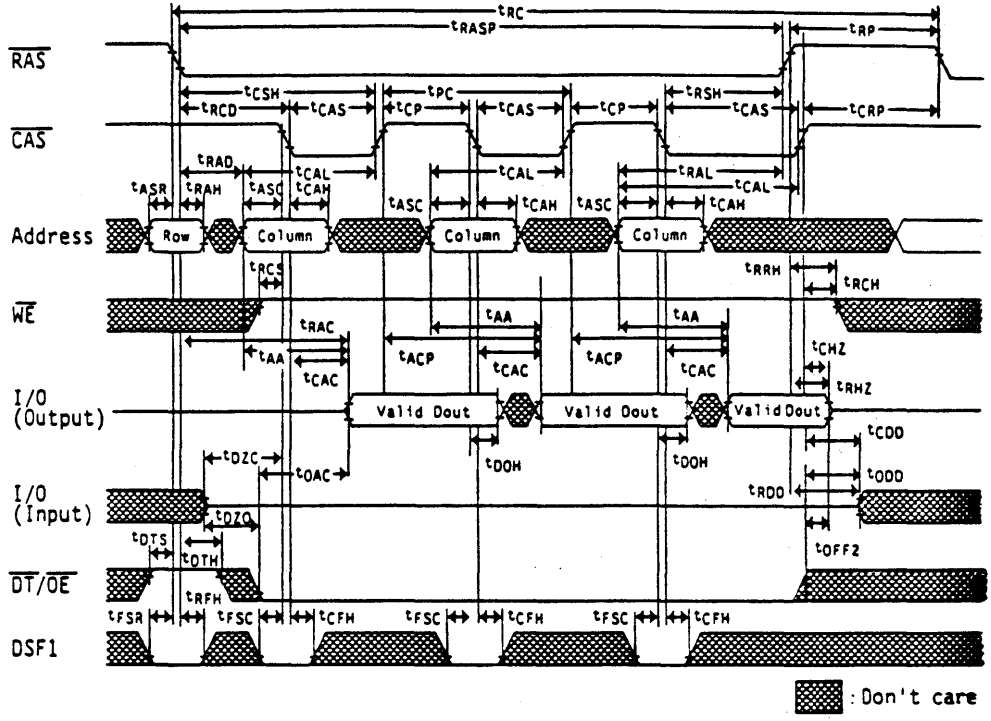
		HM538254-7		HM538254-8		HM538254-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Serial clock cycle time	t_{SCC}	25	—	28	—	30	—	ns	
SC pulse width	t_{SC}	5	—	10	—	10	—	ns	
SC precharge width	t_{SCP}	10	—	10	—	10	—	ns	
Access time from SC	t_{SCA}	—	20	—	23	—	25	ns	15
Access time from $\overline{SE}$	t_{SEA}	—	17	—	20	—	25	ns	15
Serial data-out hold time	t_{SOH}	5	—	5	—	5	—	ns	
Serial output buffer turn-off time referenced to $\overline{SE}$	t_{SHZ}	—	15	—	20	—	20	ns	5,17
$\overline{SE}$ to serial output in low-Z	t_{SLZ}	0	—	0	—	0	—	ns	5,17
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	15	—	15	—	ns	
Serial write enable setup time	t_{SWS}	0	—	0	—	0	—	ns	
Serial wrtie enbable hold time	t_{SWH}	15	—	15	—	15	—	ns	
Serial write disable setup time	t_{SWIS}	0	—	0	—	0	—	ns	
Serial write disable hold time	t_{SWIH}	15	—	15	—	15	—	ns	

Notes:
1. AC measurements assume t_T = 5 ns.
2. When $t_{RCD} > t_{RCD}$ (max) and $t_{RAD} > t_{RAD}$ (max), access time is specified by t_{CAC} or t_{AA}.
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition time t_T is measured between V_{IH} and V_{IL}.
4. Data input must be floating before output buffer is turned on. In read cycle, read-modify-write cycle and delayed write cycle, either t_{DZC} (min) or t_{DZO} (min) must be satisfied.
5. t_{RHZ} (max), t_{CHZ} (max), t_{OFF2} (max), t_{SHZ} (max) and t_{SLZ} (min) are defined as the time at which the output acheives the open circuit condition (V_{OH} – 100 mV, V_{OL} + 100 mV). This parameter is sampled and not 100% tested.
6. Assume that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
7. Measured with a load circuit equivalent to 1 TTL loads and 50 pF.
8. When $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max), access time is specified by t_{CAC}.
9. When $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max), access time is specified by t_{AA}.
10. If both t_{RCH} and t_{RRH} are satisfied, operation is guaranteed.
11. When $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle, and I/O pins remain in an open circuit (high impedance) condition.
12. These parameters are specified by the later falling edge of $\overline{CAS}$ or $\overline{WE}$.
13. Either t_{CDD} (min), t_{ODD} (min) or t_{RDD} (min) must be satisfied because output buffer must be turned off by $\overline{CAS}$, $\overline{OE}$ or $\overline{RAS}$ prior to applying data to the device when output buffer is on.
14. When $t_{AWD} \geq t_{AWD}$ (min) and $t_{CWD} \geq t_{CWD}$ (min) in read-modify-write cycle, the data of the selected address outputs to an I/O pin and input data is written into the selected address. t_{ODD} (min) must be satisfied because output buffer must be turned off by $\overline{OE}$ prior to applying data to the device.
15. Measured with a load circuit equivalent to 1 TTL loads and 30 pF.
16. After power-up, pause for 100 µs or more and execute at least 8 initialization cycle (normal memory cycle or refresh cycle), then start operation. Hitachi recommends that least 8 initialization cycle is the CBRR for internal register reset. This CBRR need not t_{STS} and t_{RST}.
17. When t_{SHZ} and t_{SLZ} are measured in the same VCC and Ta condition and tr and tf of $\overline{SE}$ are less than 5 ns, $t_{SHZ} \leq t_{SLZ}$ + 5 ns. This parameter is sampled and not 100% tested.
18. After power-up, QSF output may be High-Z, so 1 sc cycle is needed to be low-Z it.
19. DSF2 pin is open pin, but Hitachi recommends it is fixed low in all operation for the addition mode in future.

■ Timing Waveforms



Hyper Page Mode Read Cycle



Write Cycle

The write cycle state table as shown below is applied to early write, delayed write, page mode write, and read-modify write.

Write Cycle State Table

Menu	Cycle	$\overline{RAS}$	$\overline{CAS}$	$\overline{RAS}$	$\overline{RAS}$	$\overline{CAS}$
		DSF1	DSF1	$\overline{WE}$	I/O	I/O
		W1	W2	W3	W4	W5
RWM	Write mask (new/old) Write DQs to I/Os	0	0	0	Write mask*1	Valid data
BWM	Write mask (new/old) Block write	0	1	0	Write mask*2	Column mask*2
RW	Normal write (no mask)	0	0	1	Don't care*1	Valid data
BW	Block write (no mask)	0	1	1	Don't care*2	Column mask*2
LMR*4	Load mask resister	1	0	1	Don't care	Mask data*3
LCR*4	Load color resister	1	1	1	Don't care	Color data

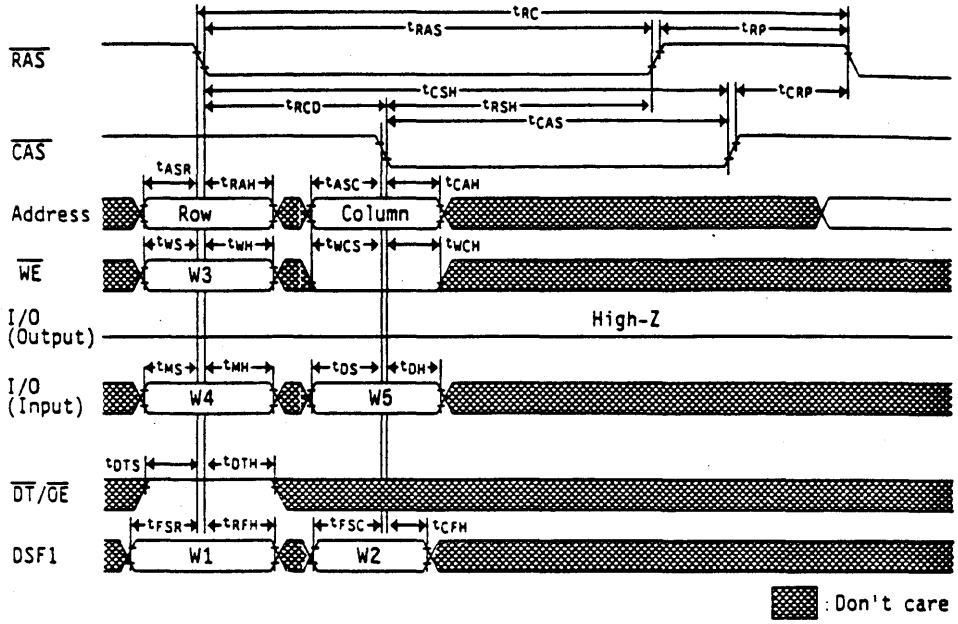
Note 1

$\overline{WE}$	Mode	I/O data/$\overline{RAS}$
Low	New Mask Mode	Mask
	Persistent Mask Mode	Don't care (mask register used)
High	No mask	Don't care

I/O Mask Data (In new mask mode)
Low: Mask
High: Non Mask
In persistent mask mode, I/O don't care

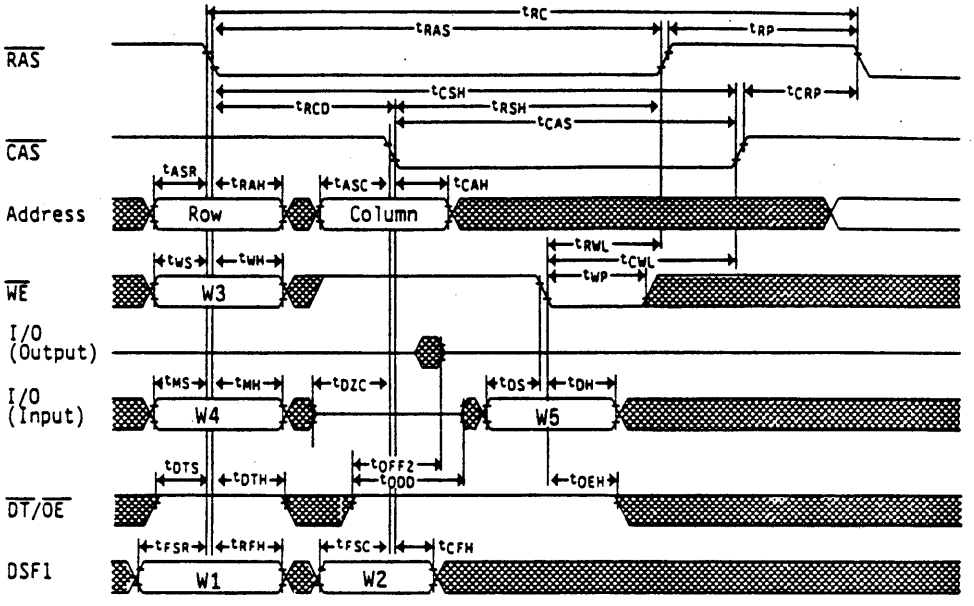
Note 2: reference Figure 2 use of Block Write
Note 3: I/O Write Mask Data
Low: Mask
High: Non mask
Note 4: Column Address: Don't care

Early Write Cycle



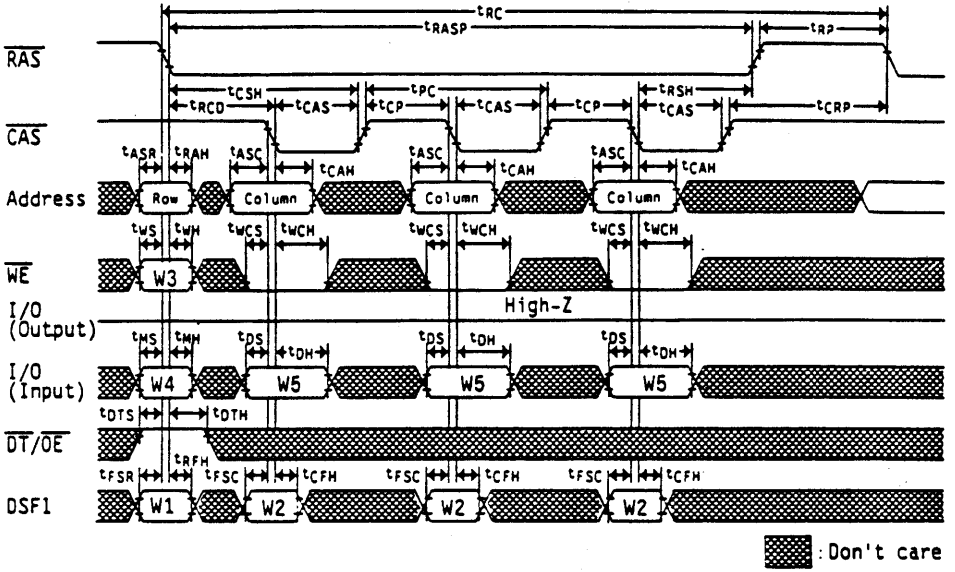
W1 to W5: See Write Cycle State Table for the logic states.

Delayed Write Cycle



W1 to W5: See Write Cycle State Table for the logic states.

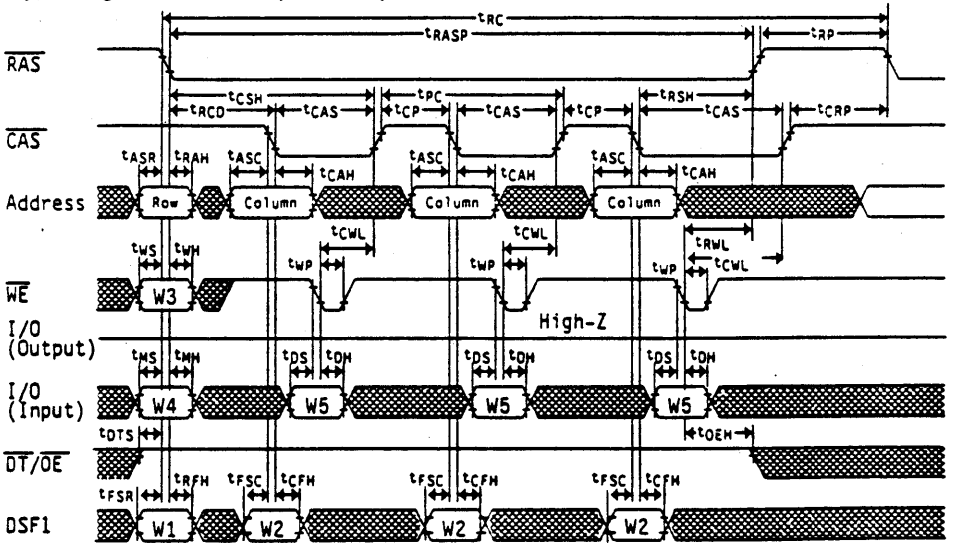
Hyper Page Mode Write Cycle (Early Write)



: Don't care

W1 to W5: See Write Cycle State Table for the logic states.

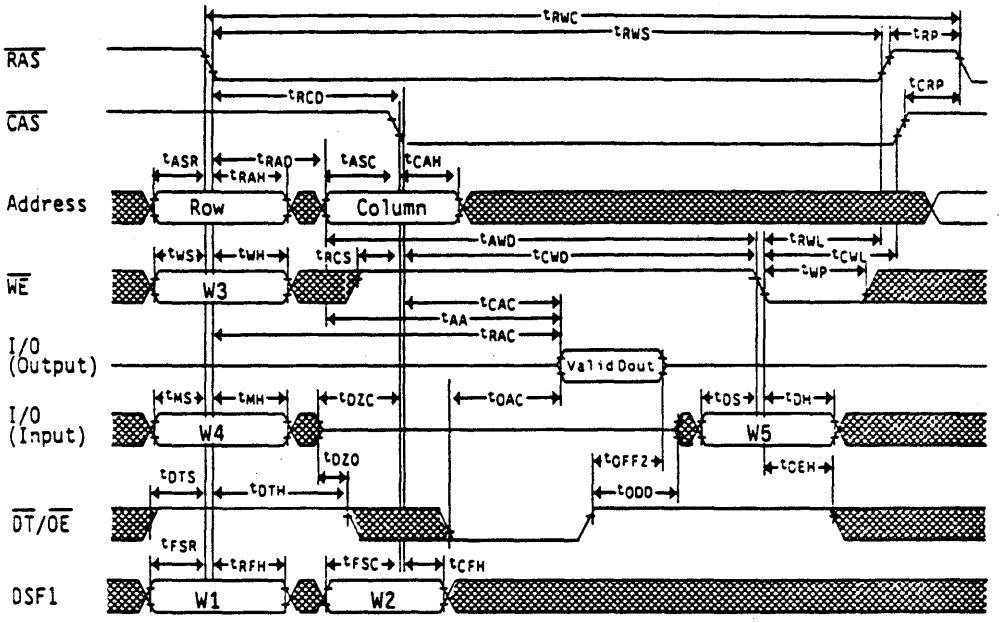
Hyper Page Mode Write Cycle (Delayed Write)



W1 to W5: See Write Cycle State Table for the locgic states.

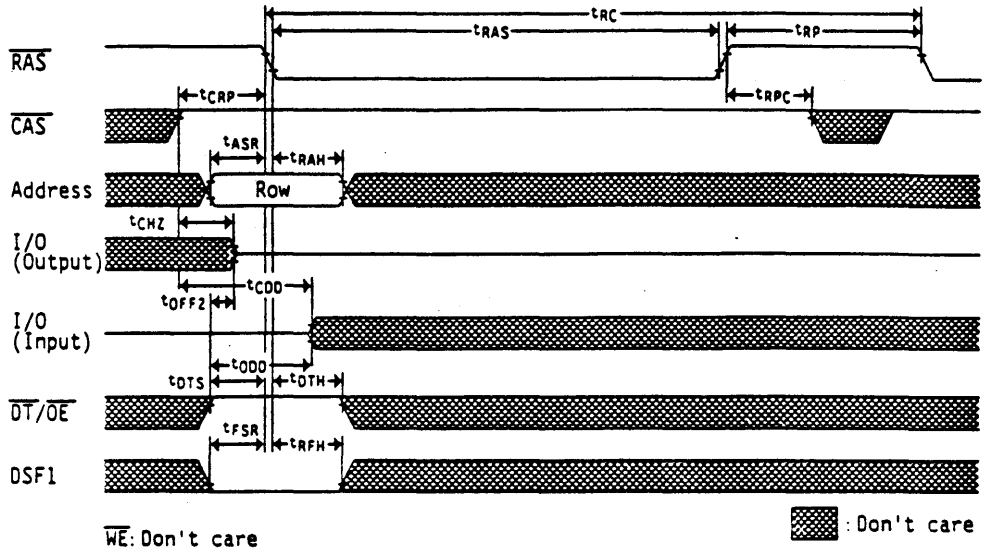
: Don't care

Read- Modify-Write Cycle

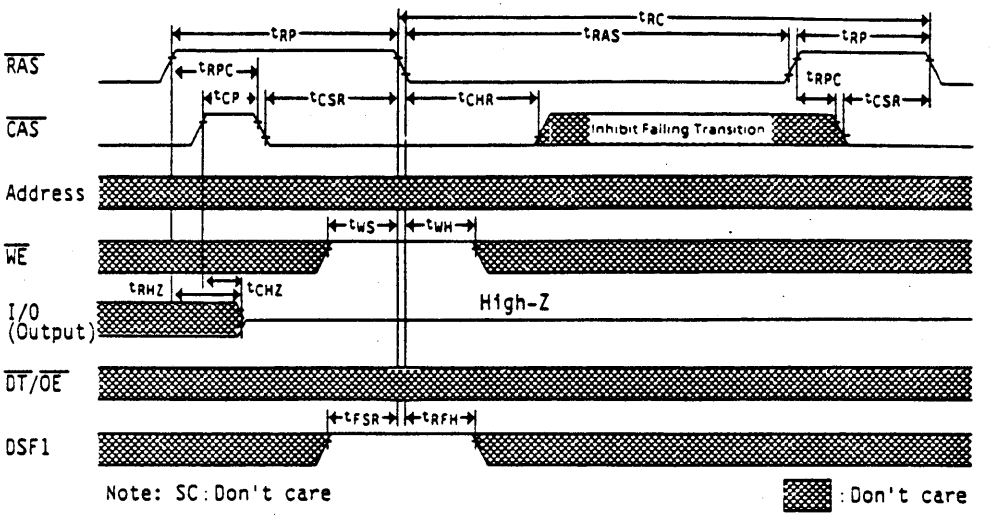


W1 to W5: See Write Cycle State Table for the logic states.

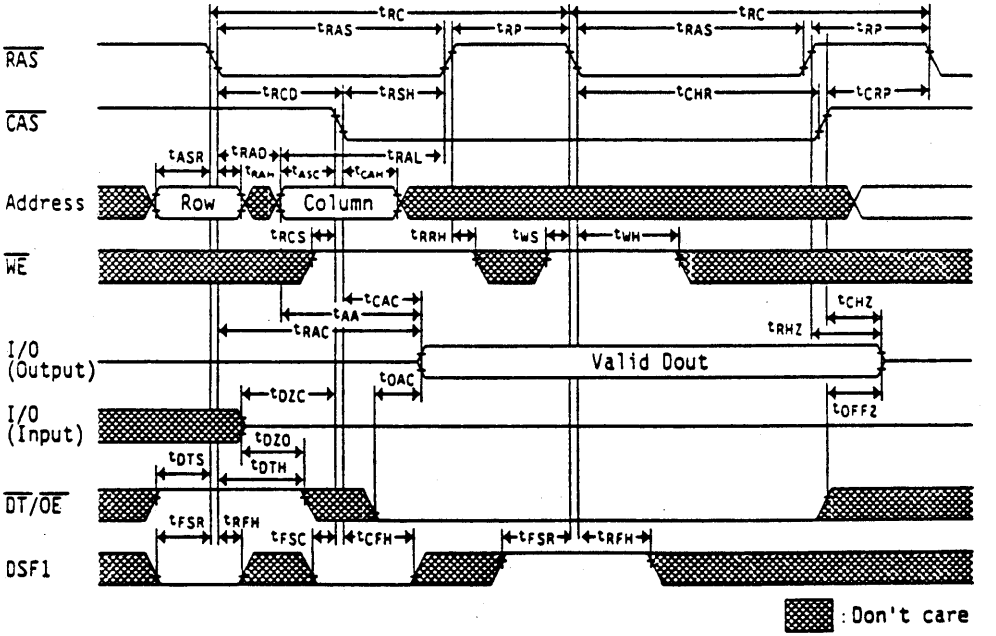
- $\overline{RAS}$-Only Refresh Cycle



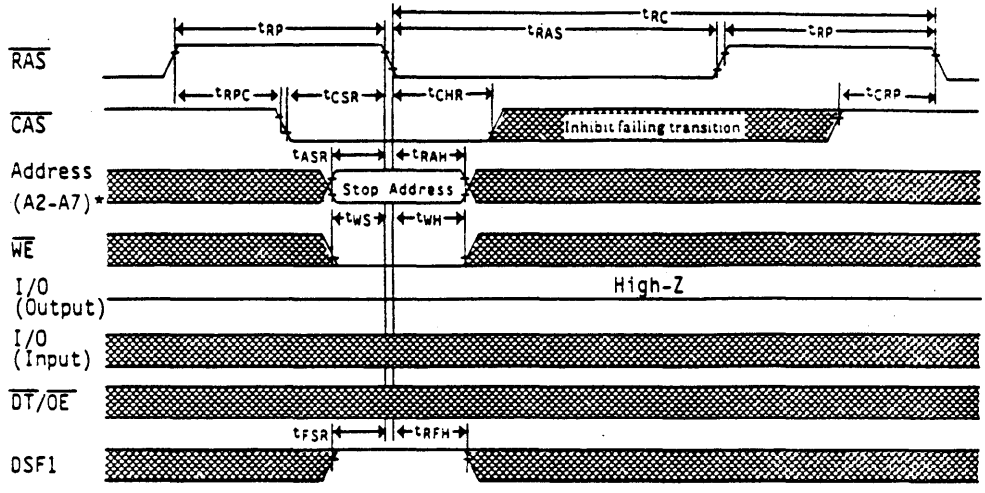
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle (CBRN)



Hidden Refresh Cycle



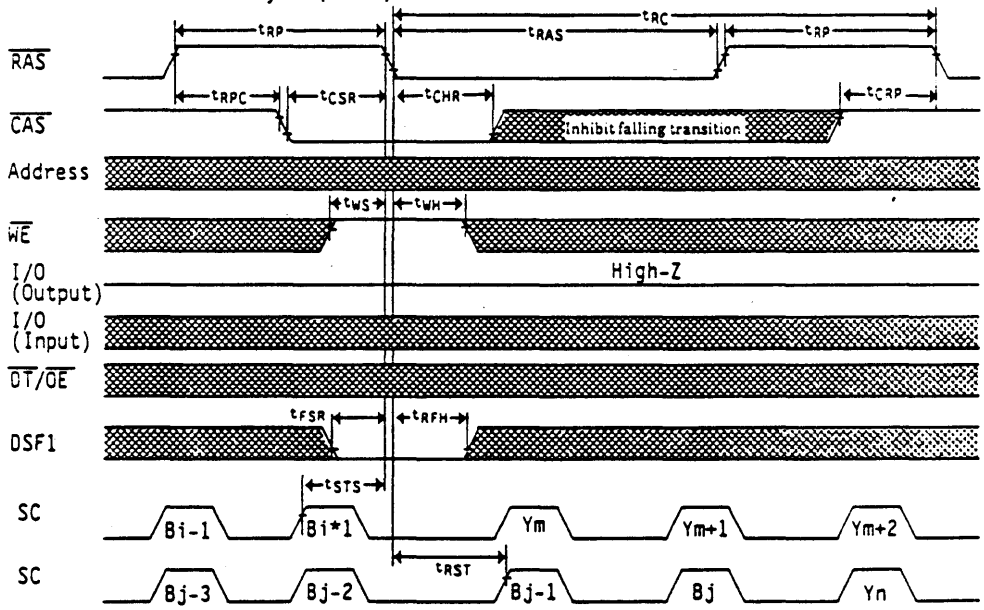
$\overline{CAS}$-Before-$\overline{RAS}$ Set Cycle (CBRS)



Note: A0, A1, A8: Don't care
SC: Don't care

: Don't care

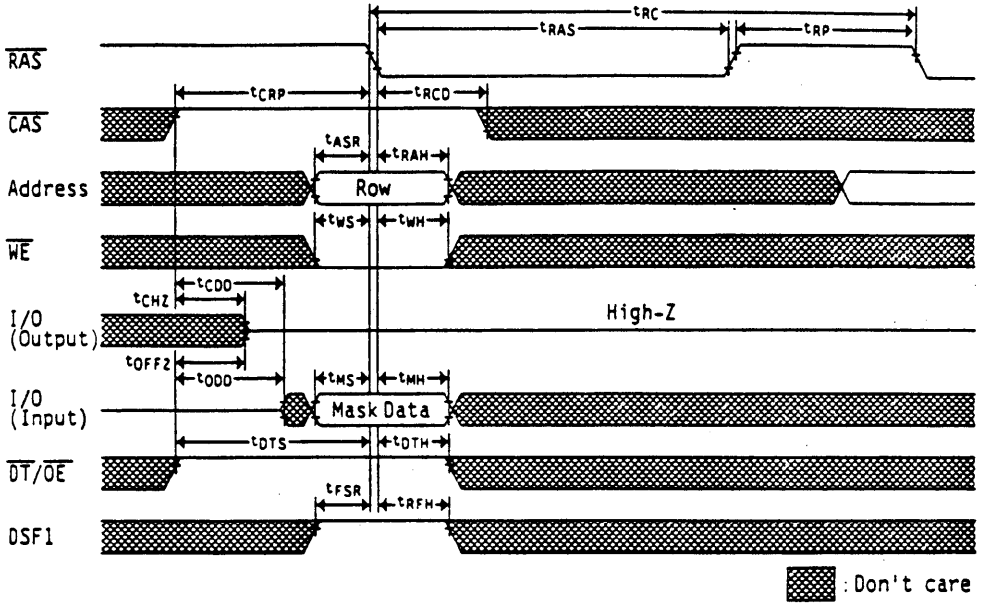
$\overline{CAS}$-Before-$\overline{RAS}$ Reset Cycle (CBRR)



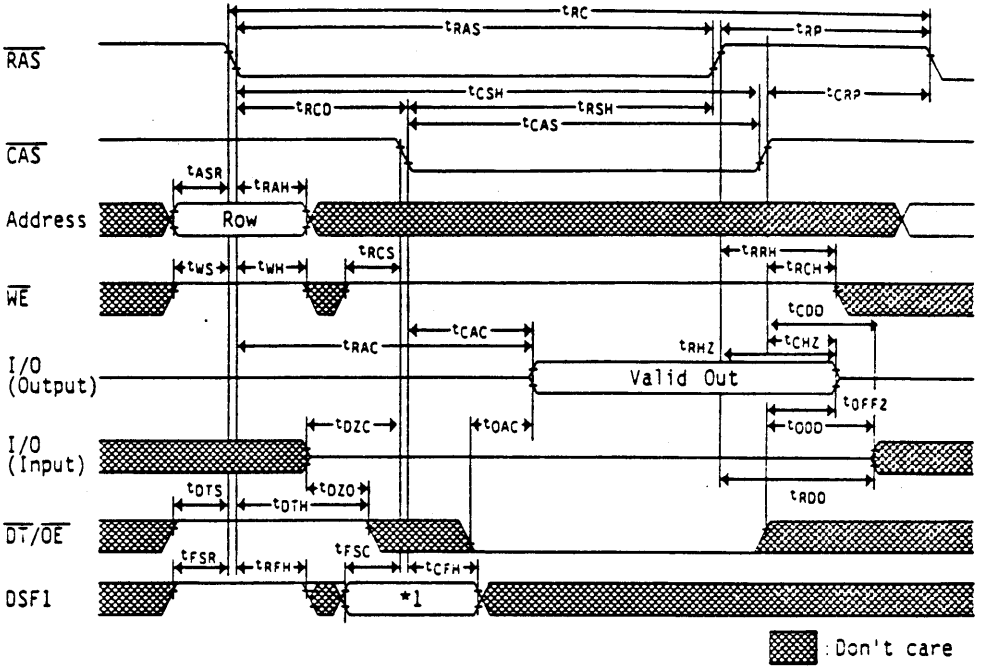
Note: 1. Bi, Bj initiate the boundary addresses.
2. Ym, Yn are the SAM start address in before SRT/MSWT.

: Don't care

Flash Write Cycle



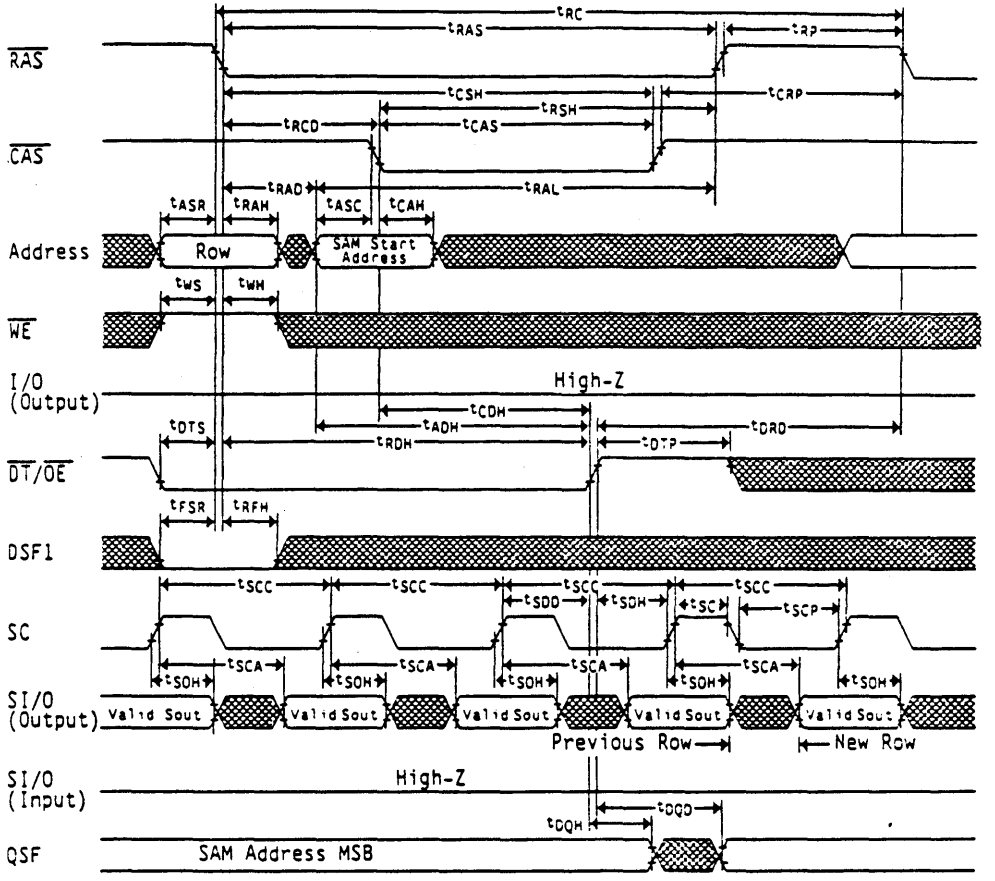
Register Read Cycle (Mask data, Color data)



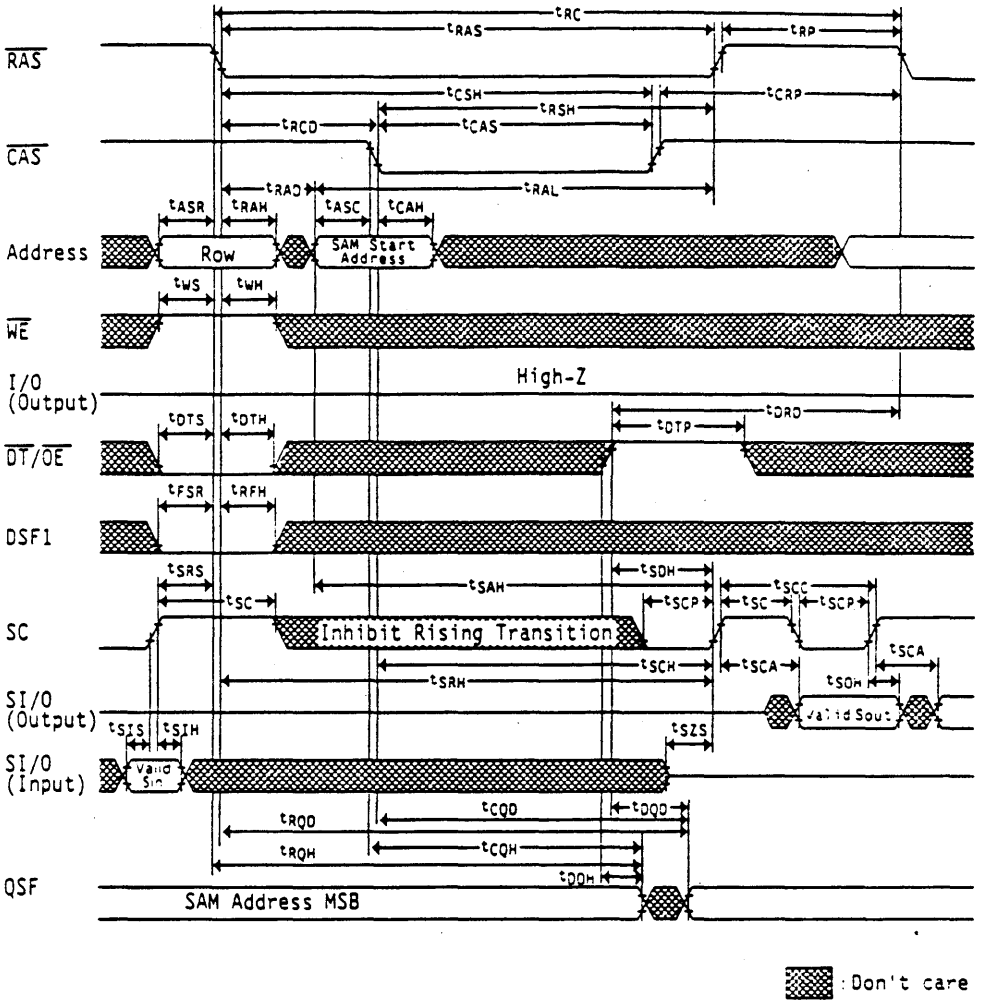
Note: 1. State of DSF1 at falling edge of $\overline{CAS}$

State	0	1
Accessed Data	Mask Data (LMR)	Color Data (LCR)

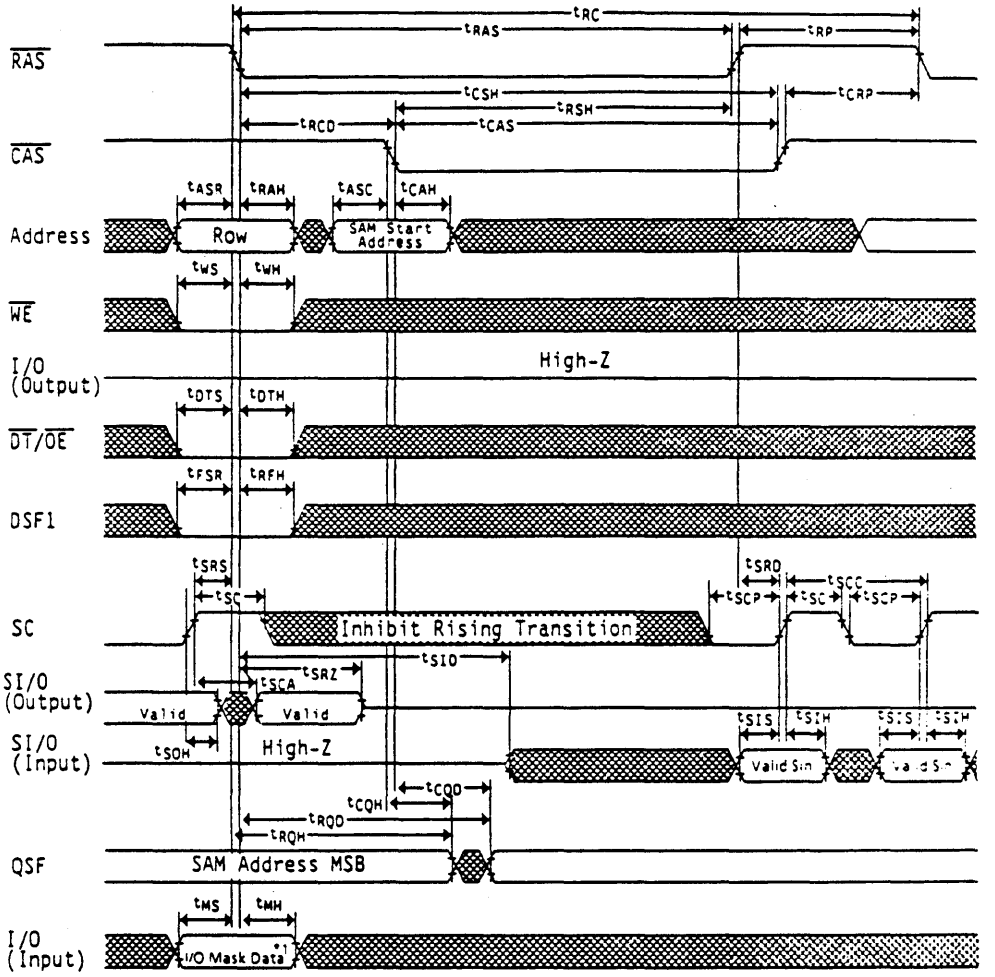
Read Transfer Cycle-1 (Real Time Read Transfer)



Read Transfer Cycle – 2



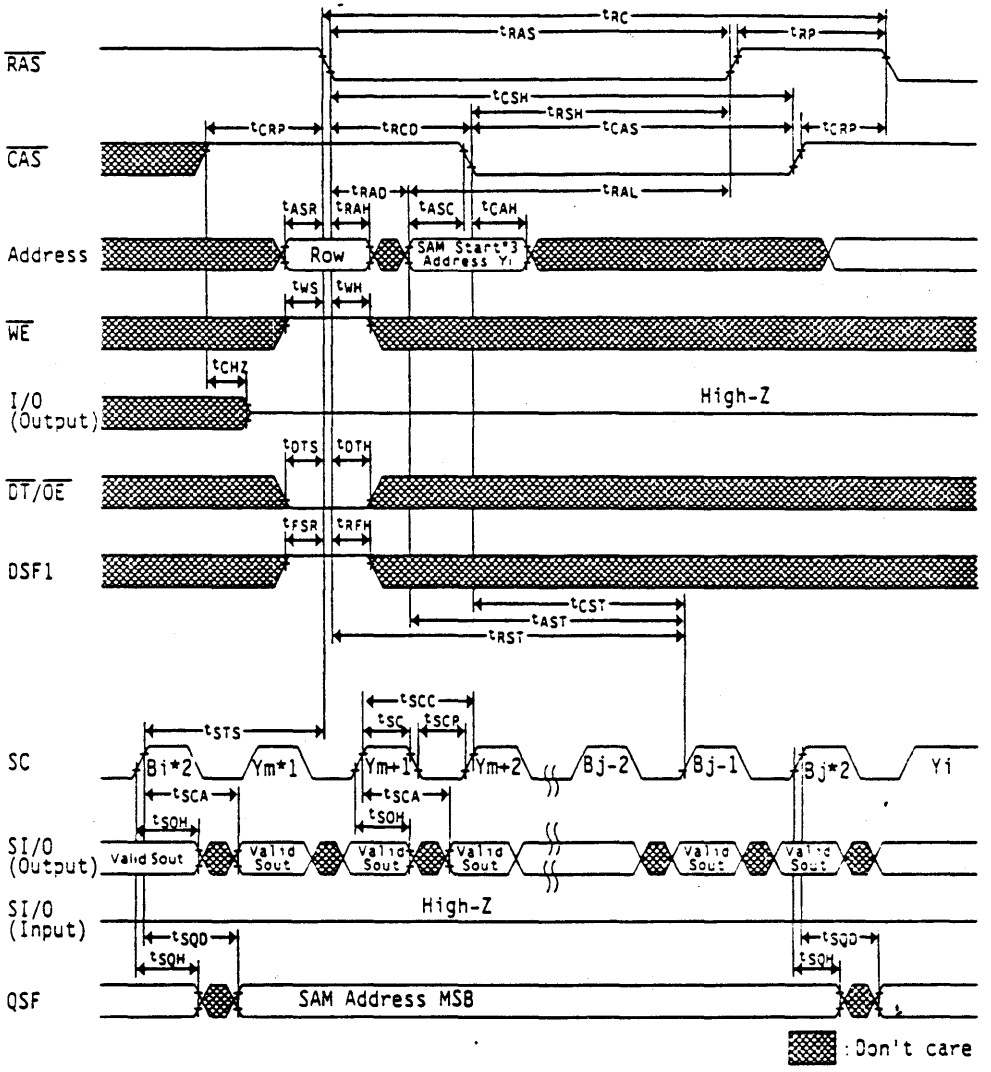
Masked Write Transfer Cycle



Note: 1. I/O Mask Data (In new mask mode)
Low : Mask
High : Non Mask
I/O : Don't care in persistent mask mode.

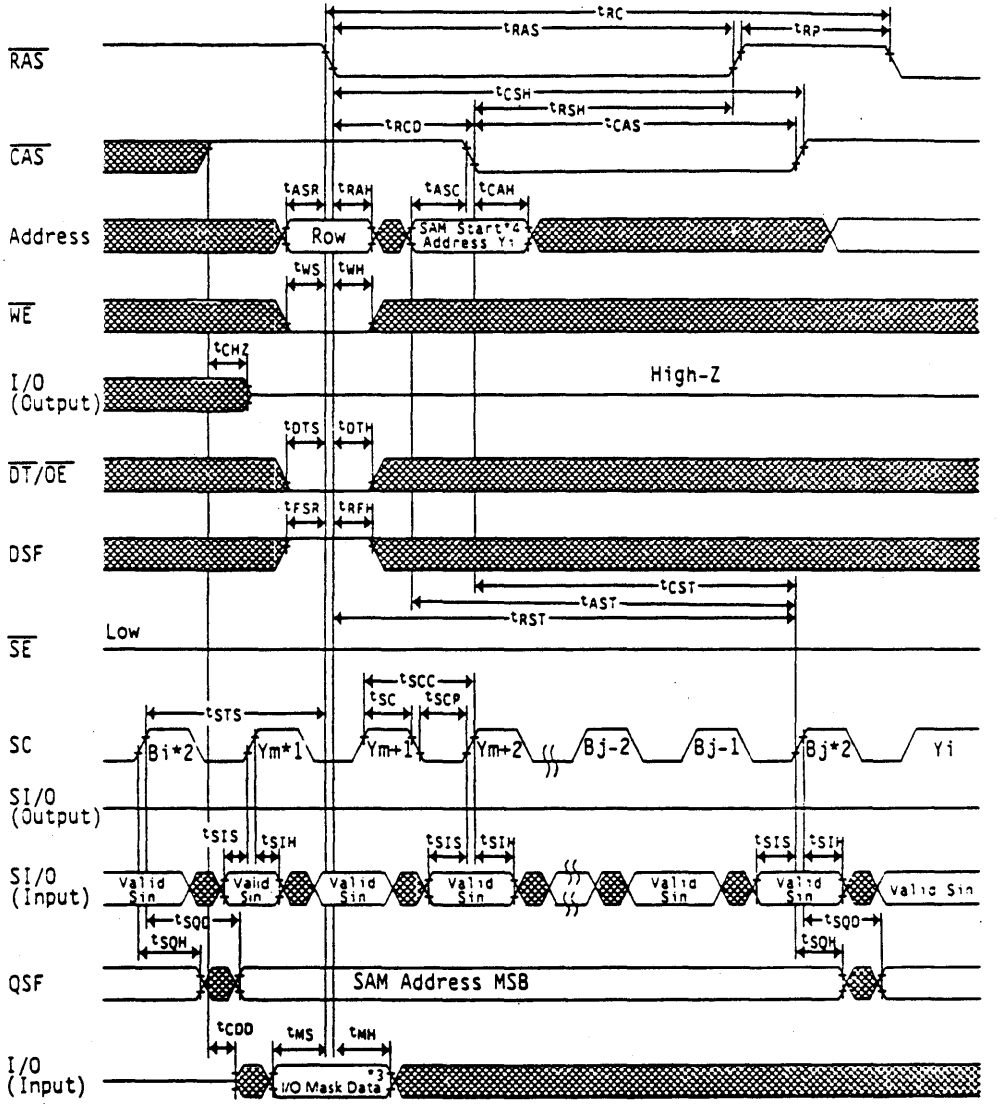
: Don't care

Split Read Transfer Cycle



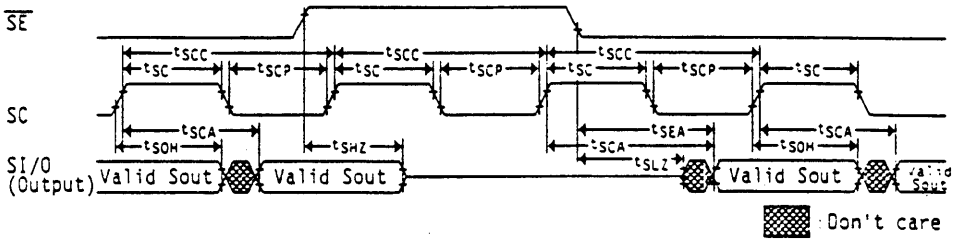
Notes: 1. Ym is the SAM start address in before SRT.
2. Bi, Bj initiate the boundary address.
3. A8 : Don't care, and upper SAM or lower SAM is set automatically by the internal circuit.
SAM start address can't set on the boundary address.

Masked Split Write Transfer Cycle

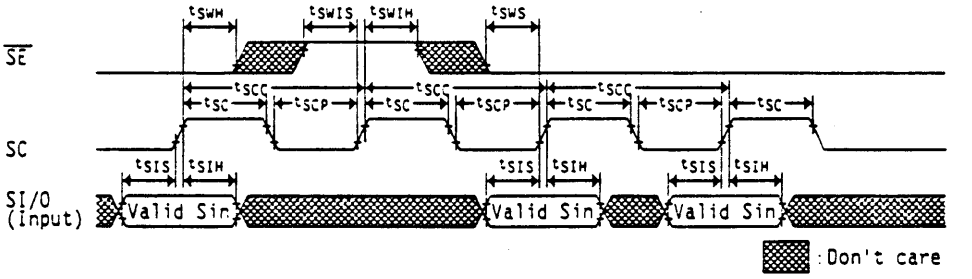


Notes: 1. Ym is the SAM start address in before MSWT.
2. Bi, Bj initiate the boundary address.
3. I/O Mask Data (In new mask mode)
Low : Mask
High : Non Mask
I/O : Don't care in persistent mask mode.
4. A8 : Don't care, and upper SAM or lower SAM is set automatically by the internal circuit.
SAM start address can't set on the boundary address.

Serial Read Cycle

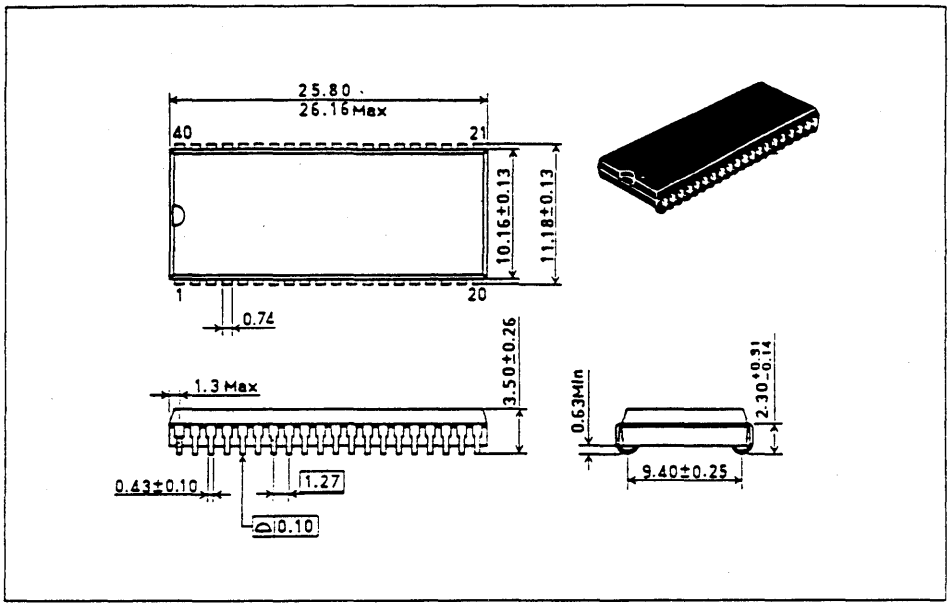


Sereal Write Cycle



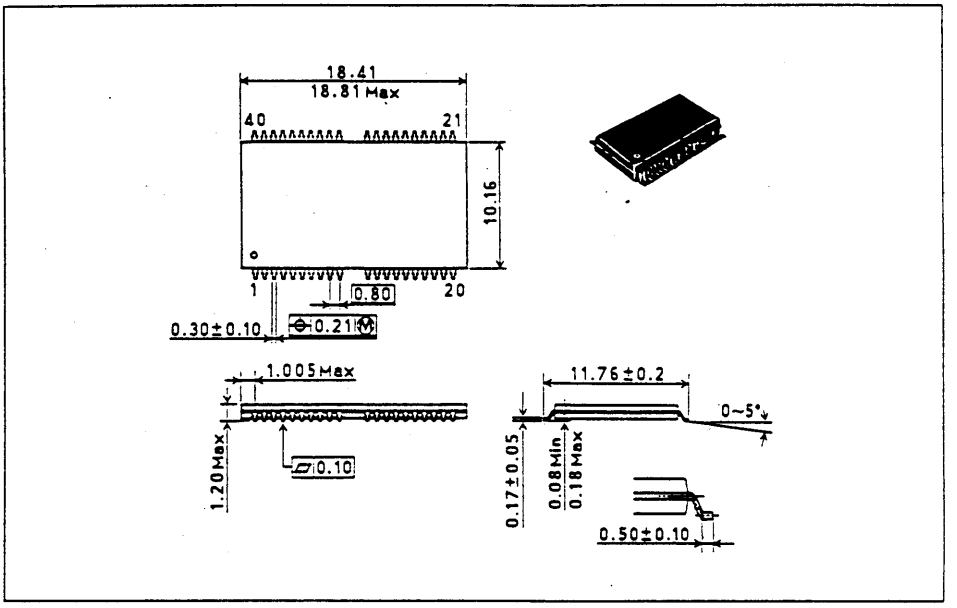
Package Dimensions

HM538254J Series (CP-40D) **Unit: mm**

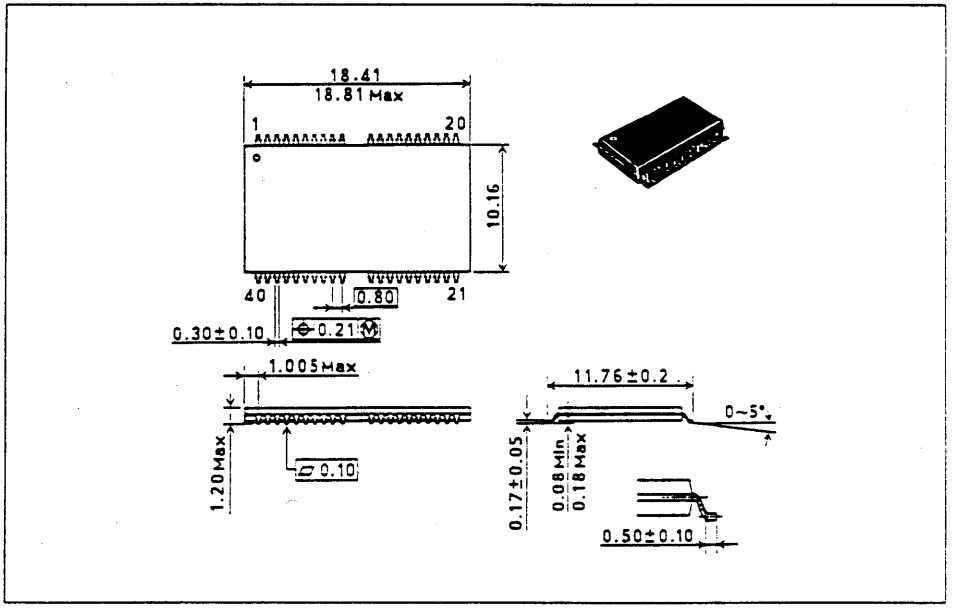


Package Dimensions (cont)

HM538254TT Series (TTP-40DA) Unit: mm



HM538254RR Series (TTP-40DAR) Unit: mm



HM5316123 Series

Preliminary

131,072-Word x 16-Bit Multiport CMOS Video RAM

HITACHI

Rev. 2
Feb. 10, 1993

The HM5316123 is a 2-Mbit multiport video RAM equipped with a 128-kword x 16-bit dynamic RAM and a 256-word x 16-bit SAM (full-sized SAM). Its RAM and SAM operate independently and asynchronously. The HM5316123 has basically upward-compatibility with the HM534253A/HM538123A except that pseudo-write-transfer cycle is replaced with masked-write-transfer cycle, which has been approved by JEDEC. Furthermore, several new features are added to the HM5316123 without conflict with the conventional features. Stopping column feature realizes much flexibility to the length of split SAM register. Persistent mask is also installed according to the TMS34020 features. Byte-write-control is useful for x16 organization to be fit to 8-bit bus system.

Features

- Multiport organization
  - Asynchronous and simultaneous operation of RAM and SAM capability
  - RAM: 128 kword x 16 bit
  - SAM: 256 word x 16 bit
- Access time
  - RAM: 70 ns/80 ns/100 ns (max)
  - SAM: 20 ns/23 ns/25 ns (max)
- Cycle time
  - RAM: 130 ns/150 ns/180 ns (min)
  - SAM: 25 ns/28 ns/30 ns (min)
- Low power
  - Active RAM: 660 mW/605 mW/550 mW
  - SAM: 468 mW/413 mW/385 mW
  - Standby 38.5 mW (max)
- Masked-write-transfer cycle capability
- Stopping column feature capability
- Persistent mask capability
- Byte write control capability: 2$\overline{WE}$ control
- Fast page mode capability
  - Cycle time: 45 ns/50 ns/55 ns
  - Power RAM: 688 mW/660 mW/633 mW
- Mask write mode capability
- Bidirectional data transfer cycle between RAM and SAM capability
- Split transfer cycle capability
- Block write mode capability
- Flash write mode capability
- 3 variations of refresh (8 ms/512 cycles)
  - $\overline{RAS}$-only refresh
  - $\overline{CAS}$-before-$\overline{RAS}$ refresh
  - Hidden refresh
- TTL compatible

Preliminary: This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

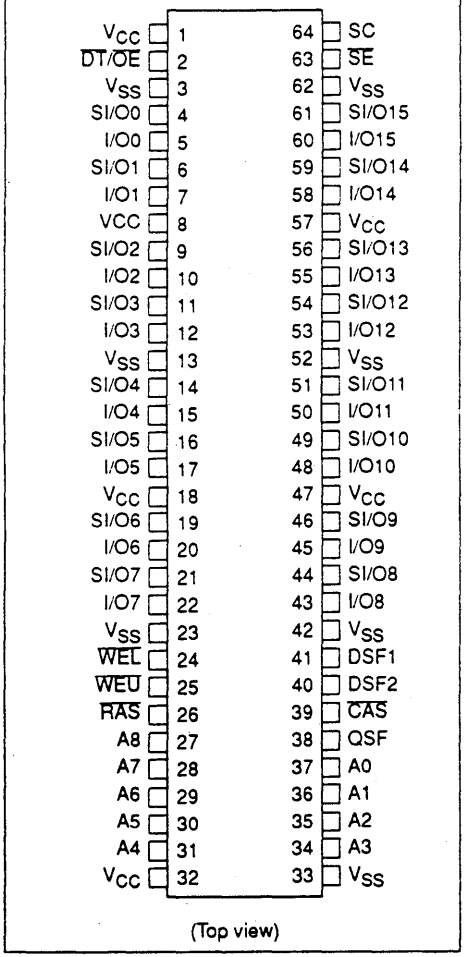
Hitachi semiconductor

Ordering Information

Type No.	Access time	Package
HM5316123F-7	70 ns	64-pin plastic shrink SOP (FP-64DS)
HM5316123F-8	80 ns	
HM5316123F-10	100 ns	

Pin Arrangement

HM5316123F Series

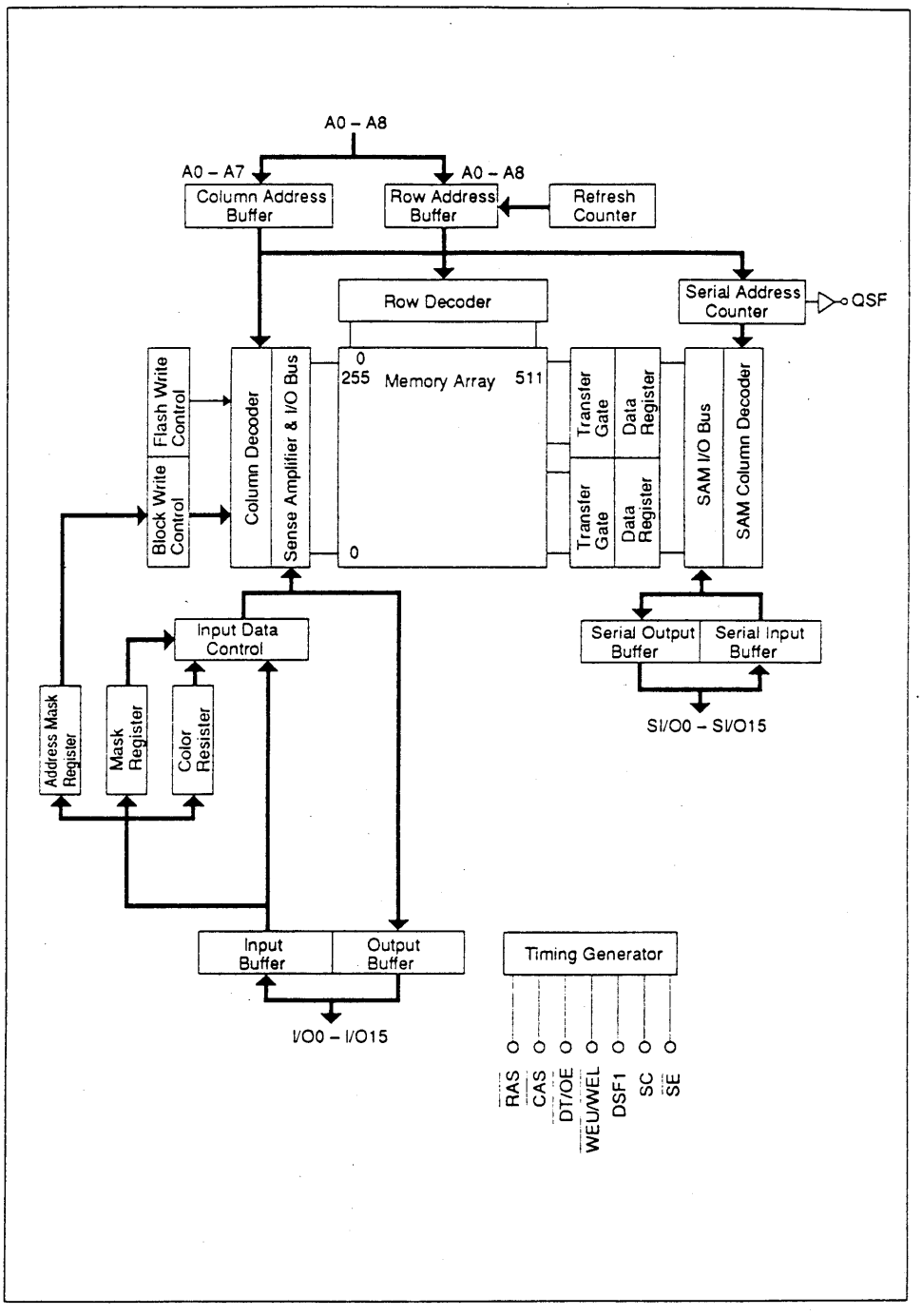


(Top view)

Pin Description

Pin name	Function
A0 – A8	Address inputs
I/O0 – I/O15	RAM port data inputs/outputs
SI/O0 – SI/O15	SAM port data inputs/outputs
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WEU}$	Upper byte write enable
$\overline{WEL}$	Lower byte write enable
$\overline{DT/OE}$	Data transfer/output enable
SC	Serial clock
$\overline{SE}$	SAM port enable
DSF1, DSF2	Special function input flag
QSF	Special function output flag
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



Pin Functions

$\overline{RAS}$ (input pin): $\overline{RAS}$ is a basic RAM signal. It is active in low level and standby in high level. Row address and signals as shown in table 1 are input at the falling edge of $\overline{RAS}$. The input level of these signals determine the operation cycle of the HM5316123.

Table 1. Operation Cycles of the HM5316123

Mnemonic Code	$\overline{RAS}$					$\overline{CAS}$		Address		I/On Input	
	$\overline{CAS}$	DT/$\overline{OE}$	$\overline{WE}$	DSF1	DSF2	DSF1	DSF2	$\overline{RAS}$	$\overline{CAS}$	$\overline{RAS}$	$\overline{CAS}$/$\overline{WE}$
CBRS	0	–	0	1	0	–	0	Stop	–	–	–
CBRR	0	–	1	0	0	–	0	–	–	–	–
CBRN	0	–	1	1	0	–	0	–	–	–	–
MWT	1	0	0	0	0	–	0	Row	TAP	WM	–
MSWT	1	0	0	1	0	–	0	Row	TAP	WM	–
RT	1	0	1	0	0	–	0	Row	TAP	–	–
SRT	1	0	1	1	0	–	0	Row	TAP	–	–
RWM	1	1	0	0	0	0	0	Row	Column	WM	Input data

Mnemonic Code	Write Mask	Pers W.M.	Register		No.of Bndry	Function
			WM	Color		
CBRS	–	–	–	–	Set	CBR refresh with stop resister set
CBRR	–	Reset	Reset	–	Reset	CBR refresh with register reset
CBRN	–	–	–	–	–	CBR refresh (no reset)
MWT	Yes	No Yes	Load/use Use	–	–	Masked write transfer (new/old mask)
MSWT	Yes	No Yes	Load/use Use	–	Use	Masked split write transfer (new/old mask)
RT	–	–	–	–	–	Read transfer
SRT	–	–	–	–	Use	Split read transfer
RWM	Yes	No Yes	Load/use Use	–	–	Read/write (new/old mask)

Table 1. Operation Cycles of the HM5316123 (cont)

Mnemonic	$\overline{RAS}$					$\overline{CAS}$		Address		I/On Input	
Code	$\overline{CAS}$	$\overline{DT/OE}$	$\overline{WE}$	DSF1	DSF2	DSF1	DSF2	$\overline{RAS}$	$\overline{CAS}$	$\overline{RAS}$	$\overline{CAS/WE}$
BWM	1	1	0	0	0	1	0	Row	Column	WM	Column Mask
RW (No)	1	1	1	0	0	0	0	Row	Column	–	Input data
BW (No)	1	1	1	0	0	1	0	Row	Column	–	Column Mask
FWM	1	1	0	1	0	–	0	Row	–	WM	–
LMR and Old Mask Set	1	1	1	1	0	0	0	(Row)	–	–	Mask Data
LCR	1	1	1	1	0	1	0	(Row)	–	–	Color
Option	0	0	0	0	0	–	0	Mode	–	Data	–

Mnemonic Code	Write Mask	Pers W.M.	Register WM	Register Color	No.of Bndry	Function
BWM	Yes	No Yes	Load/use Use	Use	–	Block write (new/old mask)
RW (No)	No	No	–	–	–	Read/write (no mask)
BW (No)	No	No	–	Use	–	Block write (no mask)
FWM	Yes	No Yes	Load/use Use	Use	–	Masked flash write (new/old mask)
LMR and Old Mask Set	–	Set	Load	–	–	Load mask register and old mask set
LCR	–	–	–	Load	–	Load color resister set
Option	–	–	–	–	–	–

Notes: 1. With CBRS, all SAM operations use stop register.
2. After LMR, RWM, BWM, FWM, MWT, and MSWT, use old mask which can be reset by CBRR.
3. DSF2 is fixed low in all operation. (for the addition of operation mode in future)

$\overline{CAS}$ (input pin): Column address and DSF1 signals are fetched into chip at the falling edge of $\overline{CAS}$, which determines the operation mode of the HM5316123. $\overline{CAS}$ controls output impedance of I/O in RAM.

A0 – A8 (input pins): Row address (AX0 – AX8) is determined by A0 – A8 level at the falling edge of $\overline{RAS}$. Column address (AY0 – AY7) is determined by A0 – A7 level at the falling edge of $\overline{CAS}$. In transfer cycles, row address is the address on the word line which transfers data with SAM data register, and column address is the SAM start address after transfer.

$\overline{WEU}$ and $\overline{WEL}$ (Input pins): $\overline{WEU}$ and $\overline{WEL}$ pins have two functions at the falling edge of $\overline{RAS}$ and after. When either $\overline{WEU}$ or $\overline{WEL}$ is low at the falling edge of $\overline{RAS}$, the HM5316123 turns to mask write mode. According to the I/O level at the time, write on each I/O can be masked. ($\overline{WEU}$ and $\overline{WEL}$ levels at the falling edge of $\overline{RAS}$ is don't care in read cycle.) When both $\overline{WEU}$ and $\overline{WEL}$ are high at the falling edge of $\overline{RAS}$, a no mask write cycle is executed. After that, $\overline{WEU}$ and $\overline{WEL}$ switch read/write cycles. Both $\overline{WEU}$ and $\overline{WEL}$ must be held high in a read cycle. In a transfer cycle, the direction of transfer is determined by $\overline{WEU}$ and $\overline{WEL}$ levels at the falling edge of $\overline{RAS}$. When either $\overline{WEU}$ or $\overline{WEL}$ is low, data is transferred from SAM to RAM (data is written into RAM), and when both $\overline{WEU}$ and $\overline{WEL}$ are high, data is transferred from RAM to SAM (data is read from RAM).

I/O0 – I/O15 (input/output pins): I/O pins function as mask data at the falling edge of $\overline{RAS}$ (in mask write mode). Data is written only to high I/O pins. Data on low I/O pins are masked and internal data are retained. After that, they function as inut/output pins as those of a standard DRAM. In block write cycle, they function as column mask data at the falling edges of $\overline{CAS}$, and $\overline{WEU}$ or $\overline{WEL}$.

$\overline{DT/OE}$ (input pin): $\overline{DT/OE}$ pin functions as $\overline{DT}$ (data transfer) pin at the falling edge of $\overline{RAS}$ and as $\overline{OE}$ (output enable) pin after that. When $\overline{DT}$ is low at the falling edge of $\overline{RAS}$, this cycle becomes a transfer cycle. When $\overline{DT}$ is high at the falling edge of $\overline{RAS}$, RAM and SAM operate independently.

SC (input pin): SC is a basic SAM clock. In a serial read cycle, data outputs from an SI/O pin synchronously with the rising edge of SC. In a serial write cycle, data on an SI/O pin at the rising edge of SC is fetched into the SAM data register.

$\overline{SE}$ (input pin): $\overline{SE}$ pin activates SAM. When $\overline{SE}$ is high, SI/O is in the high impedance state in serial read cycle and data on SI/O is not fetched into the SAM data register in serial write cycle. $\overline{SE}$ can be used as a mask for serial write because the internal pointer is incremented at the rising edge of SC.

SI/O0 – SI/O15 (input/output pins): SI/Os are input/output pins in SAM. Direction of input/output is determined by the previous transfer cycle. When it was a read transfer cycle, SI/O outputs data. When it was a masked write transfer cycle, SI/O inputs data.

DSF1 (input pin): DSF1 is a special function data input flag pin. It is set to high at the falling edge of $\overline{RAS}$ when new functions such as color register and mask register read/write, split transfer, and flash write, are used.

DSF2 (input pin): DSF2 is also a special function data input flag pin. This pin is fixed to low level in all operations of the HM5316123.

QSF (output pin): QSF outputs data of address A7 in SAM. QSF is switched from low to high by accessing address 127 in SAM and from high to low by accessing address 255 in SAM.

Operation of HM5316123

RAM Port Operation

RAM Read Cycle ($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high and DSF1 low at the falling edge of $\overline{RAS}$, DSF1 low at the falling edge of $\overline{CAS}$)

Row address is entered at the $\overline{RAS}$ falling edge and column address at the $\overline{CAS}$ falling edge to the device as in standard DRAM. Then, when $\overline{WEU}$ or $\overline{WEL}$ is high and $\overline{DT}/\overline{OE}$ is low while $\overline{CAS}$ is low, the selected address data outputs through I/O pin. At the falling edge of $\overline{RAS}$, $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ become high to distinguish RAM read cycle from transfer cycle and CBR refresh cycle. Address access time (t_{AA}) and $\overline{RAS}$ to column address delay time (t_{RAD}) specifications are added to enable fast page mode.

RAM Write Cycle (Eraly Write, Delayed Write, Read-Modify-Write)
($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high and DSF1 low at the falling edge of $\overline{RAS}$, DSF1 low at the falling edge of $\overline{CAS}$)

- No Mask Write Cycle ($\overline{WEU}$ and $\overline{WEL}$ high at the falling edge of $\overline{RAS}$)

When $\overline{CAS}$ is set low and either $\overline{WEU}$ or $\overline{WEL}$ is set low after $\overline{RAS}$ low, a write cycle is executed.
If either $\overline{WEU}$ or $\overline{WEL}$ is set low before the $\overline{CAS}$ falling edge, this cycle becomes an early write cycle and all I/O become in high impedance. All 16 data are latched on the falling edge of $\overline{CAS}$. If only one of $\overline{WEU}$ and $\overline{WEL}$ is low when $\overline{CAS}$ falls, the write will affect only those corresponding 8 bits. If the other of $\overline{WEU}$ and $\overline{WEL}$ falls at the same time in the cycle, the write will then occur for those 8 bits, with the latched data.
If both $\overline{WEU}$ and $\overline{WEL}$ are set low after the $\overline{CAS}$ falling edge, this cycle becomes a delayed write cycle and all 16 data are latched on the falling edge of $\overline{WEU}$ or $\overline{WEL}$. Byte write occures if only one of $\overline{WEU}$ or $\overline{WEL}$ falls during the cycle. I/O does not become high impedance in this cycle, so data should be entered with $\overline{OE}$ in high.
If both $\overline{WEU}$ and $\overline{WEL}$ are set low after t_{CWD} (min) and t_{AWD} (min) after the $\overline{CAS}$ falling edge, this cycle becomes a read-modify-write cycle and enables read/write at the same address in one cycle. In this cycle also, to avoid I/O contention, data should be input after reading data and driving $\overline{OE}$ high.

- Mask Write Mode ($\overline{WEU}$ or $\overline{WEL}$ low at the falling edge of $\overline{RAS}$)

If $\overline{WEU}$ or $\overline{WEL}$ is set low at the falling edge of $\overline{RAS}$, two modes of mask write cycle are capable.
1. In new mask mode, mask data is loaded from I/O pin and used. Whether or not an I/O is written depends on I/O level at the falling edge of $\overline{RAS}$. The data is written in high level I/Os, and the data is masked and retained in low level I/Os. This mask data is effective during the $\overline{RAS}$ cycle. So, in page mode cycles the mask data is retained during the page access.
2. If a load mask register cycle (LMR) has been performed, the mask data is not loaded from I/O pins and the mask data stored in mask registers persistently are used. This operation is known as persistent write mask, set by LMR cycle and reset by CBRR cycle.

Fast Page Mode Cycle ($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high and DSF1 low at the falling edge of $\overline{RAS}$)

High-speed page mode cycle reads/writes the data of the same row address at high speed by toggling $\overline{CAS}$ while $\overline{RAS}$ is low. Its cycle time is one third of the random read/write cycle. In this cycle, read, write and block write cycles can be mixed. Note that address access time (t_{AA}), $\overline{RAS}$ to column address delay time (t_{RAD}), and access time from $\overline{CAS}$ precharge (t_{ACP}) are added. In one $\overline{RAS}$ cycle, 256-word memory cells of the same row address can be accessed. It is necessary to specify access frequency within t_{RASP} max (100 μs).

Color Register Set/Read Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ high, $\overline{WEU}$ and $\overline{WEL}$ high and DSF1 high at the falling edge of $\overline{RAS}$)

In color register set cycle, color data is set to the internal color register used in flash write cycle or block write cycle. 16 bits of internal color register are provided at each I/O. This register is composed of static circuits, so once it is set, it retains the data until reset. Since color register set cycle is just as same as the usual write cycle, so read, early write and delayed write cycle can be executed. In this cycle, the HM5316123 refreshes the row address fetched at the falling edge of $\overline{RAS}$.

Mask Register Set/Read Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ high, $\overline{WEU}$ and $\overline{WEL}$ high, and DSF1 high at the falling edge of $\overline{RAS}$)

In mask register set cycle, mask data is set to the internal mask register used in mask write cycle, block write cycle, flash write cycle, masked write transfer, and masked split write transfer. 16 bits of internal mask register are provided at each I/O. This mask register is composed of static circuits, so once it is set, it retains the data until reset. Since mask register set cycle is just as same as the usual read and write cycle, so read, early and delayed write cycles can be executed.

Flash Write Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ high, $\overline{WEU}$ or $\overline{WEL}$ low, and DSF1 high at the falling edge of $\overline{RAS}$)

In a flash write cycle, a row of data (256 word x 16 bit) is cleared to 0 or 1 at each I/O according to the data of color register mentioned before. It is also necessary to mask I/O in this cycle. When $\overline{CAS}$ and $\overline{DT/OE}$ is set high, $\overline{WEU}$ or $\overline{WEL}$ is low, and DSF1 is high at the falling edge of $\overline{RAS}$, this cycle starts. Then, the row address to clear is given to row address. Mask data is as same as that of a RAM write cycle. Cycle time is the same as those of RAM read/write cycles, so all bits can be cleared in 1/256 of the usual cycle time. (See figure 1.)

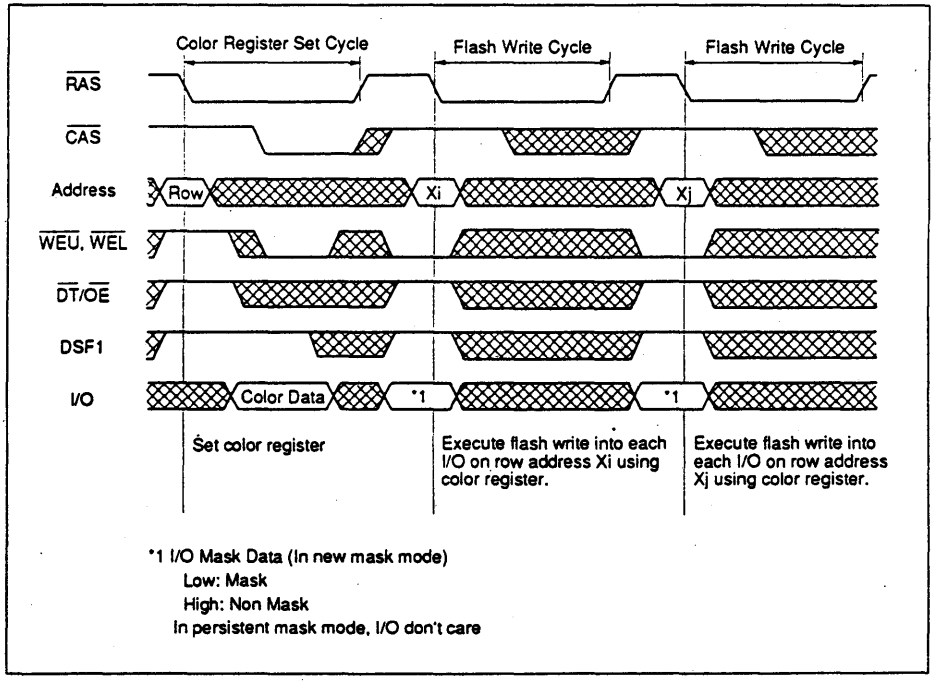


Figure 1 Use of Flash Write

Block Write Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ high and DSF1 low at the falling edge of $\overline{RAS}$, DSF1 high and $\overline{WEU}$ or $\overline{WEL}$ low at the falling edge of $\overline{CAS}$)

In a block write cycle, 4 columns of data (4 column x 16 bit) are cleared to 0 or 1 at each I/O according to the data of color register. Column addresses A0 and A1 are disregarded. The mask data on I/Os and the mask data on column addresses can be determined independently. I/O level at the falling edge of $\overline{CAS}$ determines the address to be cleared. (See Figure 2.) The block write cycle is as the same as the usual write cycle, so early and delayed write, read-modify-write, and page mode write cycle can be executed.

- No mask Mode Block Write Cycle ($\overline{WEU}$ and $\overline{WEL}$ high at the falling edge of $\overline{RAS}$)

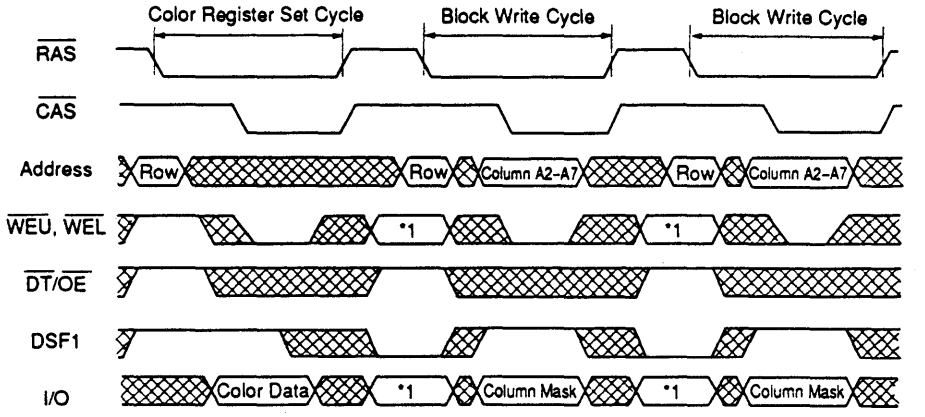
The data on 16 I/Os are all cleared when $\overline{WEU}$ and $\overline{WEL}$ are high at the falling edge of $\overline{RAS}$.

- Mask Block Write Cycle ($\overline{WEU}$ or $\overline{WEL}$ low at the falling edge of $\overline{RAS}$)

When either $\overline{WEU}$ or $\overline{WEL}$ is low at the falling edge of $\overline{RAS}$, the HM5316123 starts mask block write cycle to clear the data on an optional I/O. The mask data is the same as that of a RAM write cycle. High I/O is cleared, low I/O is not cleared and the internal data is retained. In new mask mode, the mask data is available in the $\overline{RAS}$ cycle. In persistent mask mode, I/O don't care about mask mode.

- Column Mask ($\overline{WEU}$ or $\overline{WEL}$ low at the falling edge of $\overline{CAS}$)

Column mask data is determined by 4I/Os (I/O0, I/O1, I/O2, I/O3) level at $\overline{CAS}$ low and $\overline{WEU}$ or $\overline{WEL}$ low edge. When upper byte column mask is performed by $\overline{WEL}$ high and $\overline{WEU}$ low, column mask data are determined by 4I/Os (I/O0, I/O1, I/O2, I/O3) and other I/Os (I/O4 to I/O15) don't care.



*1

WEU, WEL	Mode	I/O data/RAS
Either Low	New Mask Mode	Mask
	Persistent Mask Mode	Don't care (mask register used)
Both High	No mask	Don't care

I/O Mask Data (In new mask mode)
Low: Mask
High: Non Mask
In persistent mask mode, I/O don't care

Column Mask Data

I/O0	Column0 (A0 = 0, A1 = 0) Mask Data	Low: Mask
I/O1	Column1 (A0 = 1, A1 = 0) Mask Data	
I/O2	Column2 (A0 = 0, A1 = 1) Mask Data	High: Non Mask
I/O3	Column3 (A0 = 1, A1 = 1) Mask Data	

Figure 2 Use of Block Write

Transfer Operation

The HM5316123 provides the read transfer cycle, split read transfer cycle, masked write transfer cycle and masked split write transfer cycle as data transfer cycles. Theses transfer cycles are set by driving $\overline{CAS}$ high and $\overline{DT/OE}$ low at the falling edge of $\overline{RAS}$. They have following functions:
(1) Transfer data between row address and SAM data register
Read transfer cycle and split read transfer cycle: RAM to SAM
Masked write transfer cycle and masked split write transfer cycle: SAM to RAM
(2) Determine SI/O state (except for split read transfer cycle and masked split write transfer cycle)
Read transfer cycle: SI/O output
Masked write transfer cycle: SI/O input
(3) Determine first SAM address to access after transferring at column address (SAM start address).
SAM start address must be determined by read transfer cycle or masked write transfer cycle (split transfer cycle isn't available)before SAM access, after power on, and determined for each transfer cycle.
(4) Use the stopping columns (boundaries) in the serail shift register. If the stopping columns have been set, split transfer cycles use the stopping columns, but any boundaries cannot be set as the start address.
(5) Load/use mask data in masked write transfer cycle and masked split write transfer cycle.

Read Transfer Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ low, $\overline{WEU}$ and $\overline{WEL}$ high and DSF1 low at the falling edge of $\overline{RAS}$)

This cycle becomes read transfer cycle by driving $\overline{DT/OE}$ low, $\overline{WEU}$ and $\overline{WEL}$ high and DSF1 low at the falling edge of $\overline{RAS}$. The row address data (256 x 16 bits) determined by this cycle is transferred to SAM data register synchronously at the rising edge of $\overline{DT/OE}$. After the rising edge of $\overline{DT/OE}$, the new address data outputs from SAM start address determined by column address. In read transfer cycle, $\overline{DT/OE}$ must be risen to transfer data from RAM to SAM.
This cycle can access SAM even during transfer (real time read transfer). In this case, tie timing t_{SDD} (min) specified between the last SAM access before transfer and $\overline{DT/OE}$ rising edge and t_{SDH} (min) specified between the first SAM access and $\overline{DT/OE}$ rising edge must be satisfied. (See figure 3.)
When read transfer cycle is executed, SI/O becomes output state by first SAM access. Input must be set high impedance before t_{SZS} (min) of the first SAM access to avoid data contention.

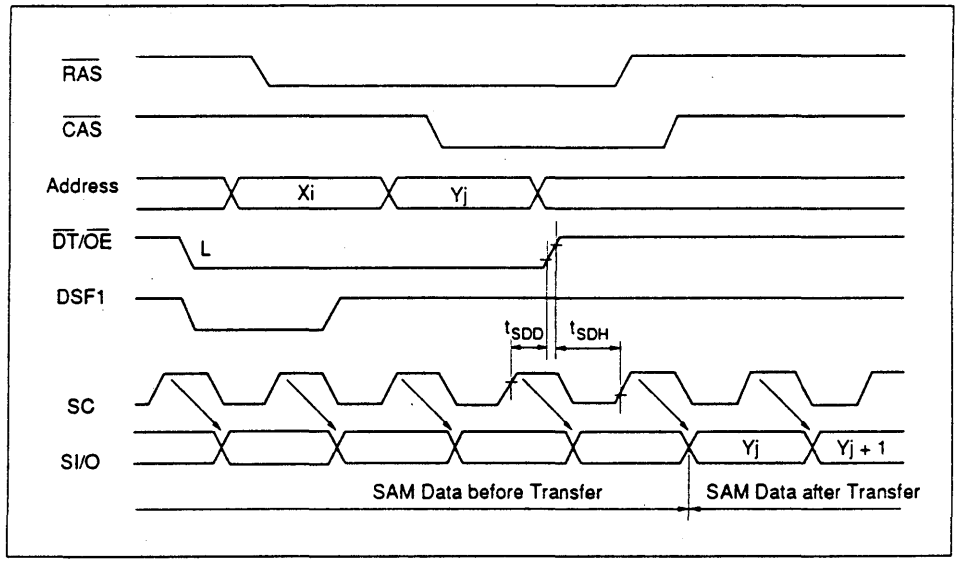


Figure 3 Real Time Read Transfer

Masked Write Transfer cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ low, $\overline{WEU}$ or $\overline{WEL}$ low, and DSF1 low at the falling edge of $\overline{RAS}$)

Masked write transfer cycle can transfer only selected I/O data in a row of data input by serial write cycle to RAM. Whether one I/O data is transferred or not depends on the corresponding I/O level (mask data) at the falling edge of $\overline{RAS}$. This mask transfer operation is the same as a mask write operation in RAM cycles, so the persistent mode can be supported. The row address of data transferred into RAM is determined by the address at the falling edge of $\overline{RAS}$. The column address is specified as the first address for serial write after terminating this cycle. Also in this cycle, SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. SAM access is inhibited during $\overline{RAS}$ low. In this period, SC must bot be risen. Data transferred to SAM by read transfer cycle or split read transfer cycle can be written to other addreses of RAM by write transfer cycle. However, the adddress to write data must be the same as that of the read transfer cycle or the split read transfer cycle (row address AX8)

Split Read Transfer Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ low, $\overline{WEU}$ and $\overline{WEL}$ high and DSF1 high at the falling edge of $\overline{RAS}$)

To execute a continuous serial read by real time read transfer, the HM5316123 must satisfy SC and $\overline{DT/OE}$ timings and requires an external circuit to detect SAM last address. Split read transfer cycle makes it possible to execute a continuous serial read without the above timing limitation.

The HM5316123 supports two types of split register operation. One is the normal split register operation to split the data register into two halves. The other is the boundary split register operation using stopping columns described later.

Figure 4 shows the block diagram for the normal split register operation. SAM data register (DR) consists of 2 split buffers, whose organizations are 128-word x 16-bit each. Let us suppose that data is read from upper data reagister DR1 (The row address AX8 is 0 and SAM address A7 is 1.). When split read transfer is executed setting row address AX8 to 0 and SAM start addresses A0 to A6, 128-word x 16-bit data are transferred from RAM to the lower data register DR0 (SAM address A7 is 0) automatically. After data are read from data register DR1, data start to be read from SAM start addresses of data register DR0. If the next split read transfer isn't executed while data are read from data register DR0, data start to be read from SAM start address 0 of DR1 after data are read from data register DR0. If split read transfer is executed setting row address AX8 to 1 and SAM start addresses A0 to A6 while data are read from data register DR1, 128-word x 16-bit data are transferred to data register DR2. After data are read from data register DR1, data start to be read from SAM start addresses of data register DR2. If the next split read transfer isn't executed while data is read from data register DR2, data start to be read from SAM start address 0 of data register DR1 after data are read from data register DR2. In split read data transfer, the SAM start address A7 is automatically set in the data register, which isn't used.

The data on SAM address A7, which will be accessed next, outputs to QSF, QSF is switched from low to high by accessing SAM last address 127 and from high to low by accessing address 255.

Split read transfer cycle is set when $\overline{CAS}$ is high, $\overline{DT/OE}$ is low, $\overline{WEU}$ and $\overline{WEL}$ is high and DSF1 is high at the falling edge of $\overline{RAS}$. The cycle can be executed asyncronously with SC. However, HM5316123 must be satisfied tSTS (min) timing specified between SC rising (Boundary address) and $\overline{RAS}$ falling. In split transfer cycle, the HM5316123 must satisfy t_{RST} (min), t_{CST} (min) and t_{AST} (min) timings specified between $\overline{RAS}$ or $\overline{CAS}$ falling and column address. (See figure 5.)

In split read transfer, SI/O isn't switched to output state. Therefore, read transfer must be executed to switch SI/O to output state when the previous transfer cycle is masked write transfer cycle or masked split write transfer cycle. SAM start address must be set in every split read transfer cycle.

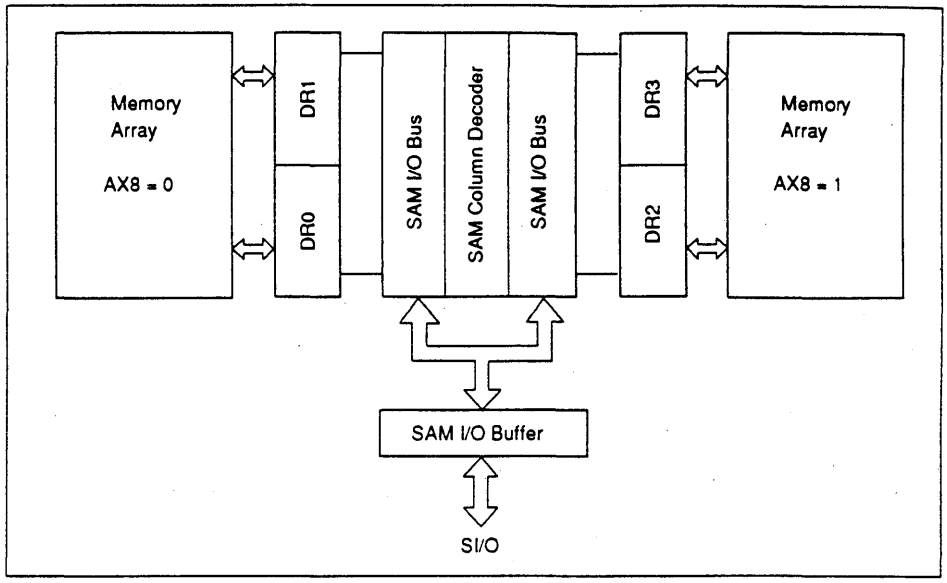


Figure 4 Block Diagram for Split Transfer

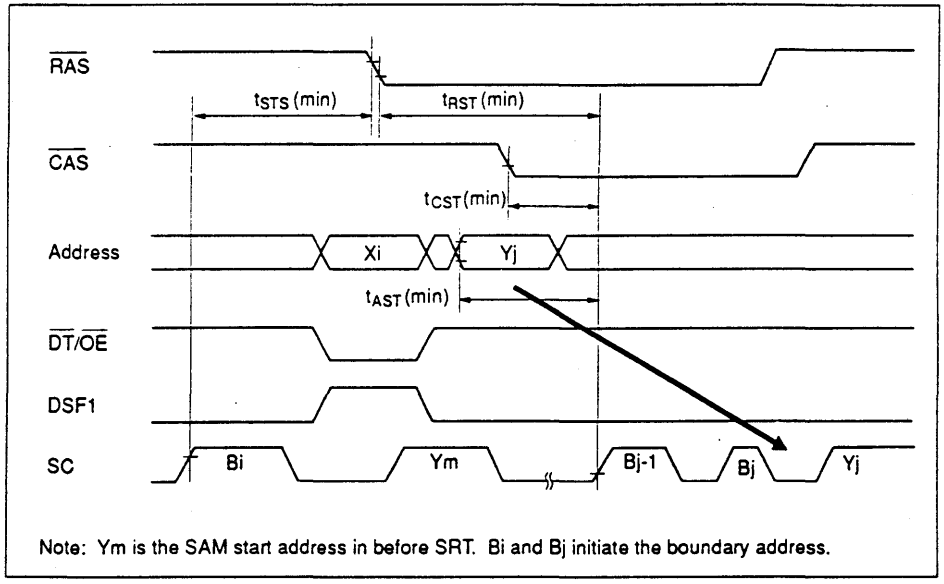


Figure 5 Limitation in Split Transfer

Masked Split Write Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WEU}$ or $\overline{WEL}$ low and DSF1 high at the falling edge of $\overline{RAS}$)

A continuous serial write cannot be executed because accessing SAM is inhibited during $\overline{RAS}$ low in write transfer. Masked split write transfer cycle makes it possible. In this cycle, t_{STS} (min), t_{RST} (min), t_{CST} (min) and t_{AST} (min) timings must be satisfied like split read transfer cycle. And it is impossible to switch SI/O to input state in this cycle. If SI/O is in output state, masked write transfer cycle should be executed to switch SI/O into input state. Data transferred to SAM by read transfer cycle or split read transfer cycle can be written to other addresses of RAM by masked split write transfer cycle. However, masked write transfer cycle must be executed before split write transfer cycle. And in this masked split write transfer cycle, the MSB of row address (AX8) to write data must be the same as that of the read transfer cycle or the split read transfer cycle.

Stopping Column in Split Transfer Cycle

The HM5316123 has the boundary split register operation using stopping columns. If a CBRS cycle has been performed, split transfer cycle performs the boundary operation. Figure 6 shows an example of boundary split register. (Boundary code is B6.)
First of all a read data transfer cycle is executed, and SAM start addresses A0 to A7 are set. The RAM data are transferred to the SAM, and SAM serial read starts from the start address (Y1) on the lower SAM. After that, a split read transfer cycle is executed, and the next start address (Y2) is set. The RAM data are transferred to the upper SAM. When the serial read arrive at the first boundary after the split read transfer cycle, the next read jumps to the start address (Y2) on the upper SAM (jump 1) and continues. Then the second split read transfer cycle is executed, and another start address (Y3) is set. The RAM data are transferred to the lower SAM. When the serial read arrive at the other boundary again, the next read jumps to the start address (Y3) on the lower SAM. In stopping column, split transfer is needed for jump operation between lower SAM and upper SAM.

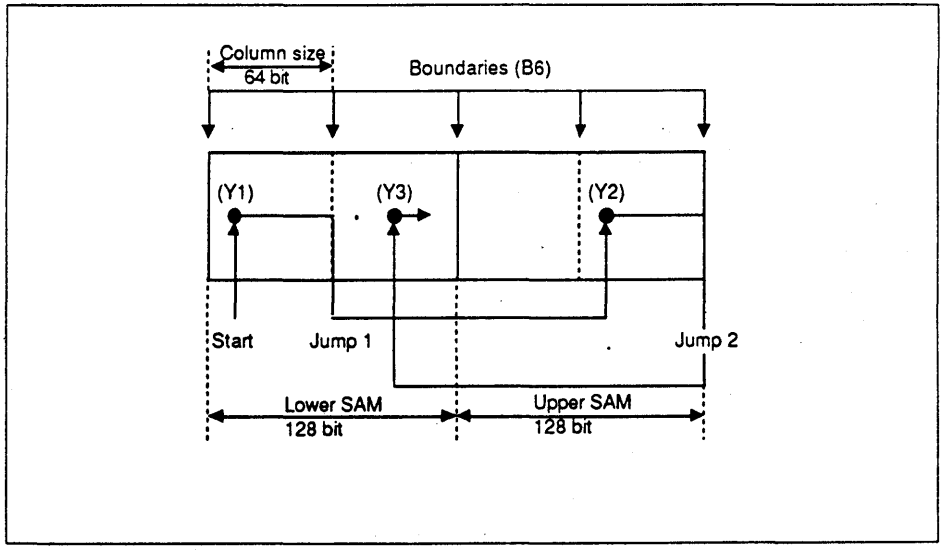


Figure 6 Example of Boundary Split Register

Stopping Column Set Cycle (CBRS)

This cycle becomes stopping column set cycle by driving $\overline{CAS}$ low, $\overline{WEU}$ or $\overline{WEL}$ low, DSF1 high at the falling edge of $\overline{RAS}$. Stopping column data (boundaries) are latched from address inputs on the falling edge of $\overline{RAS}$. To determine the boundary, A2 to A6 can be used and don't care A0, A1, and A7. In the HM5316123, 6 types of boundary (B2 to B7) can be set including the default case. (See stopping column boundary table.) If A2 to A5 are set to high and A6 is set to low, the boundaries (B6) are selected. Figure 6 shows the example. The stop address that is set by the CBRS is used from next split transfer cycle. Once a CBRS is executed, the stopping column operation mode continues until CBRR.

Stopping Column Boundary Table

		Stop Address				
Boundary code	Column size	A2	A3	A4	A5	A6
B2	4	0	*	*	*	*
B3	8	1	0	*	*	*
B4	16	1	1	0	*	*
B5	32	1	1	1	0	*
B6	64	1	1	1	1	0
B7	128	1	1	1	1	1

Notes: 1. A0, A1, and A7: don't care
2. *: don't care

Register Reset Cycle (CBRR)

This cycle becomes register reset cycle (CBRR) by driving $\overline{CAS}$ low, $\overline{WEU}$ and $\overline{WEL}$ high, and DSF1 low at the falling edge of $\overline{RAS}$. A CBRR can reset the persistent mask operation and stopping column operation, so the HM5316123 becomes the new mask operation and boundary code B7. When a CBRR is executed for stopping column operation reset and split transfer operation, it need to satisfy t_{STS} (min) and t_{RST} (min) between $\overline{RAS}$ falling and SC rising for correct SAM read/write operation.

No Reset CBR Cycle (CBRN)

This cycle becomes no reset CBR cycle (CBRN) by driving $\overline{CAS}$ low, $\overline{WE}$ high and DSF1 high at the falling edge of $\overline{RAS}$. The CBRN can only execute the refresh operation.

Byte Control ($\overline{WEU}$, $\overline{WEL}$)

In a write cycle, when $\overline{WEL}$ set low and $\overline{WEU}$ set high, I/O0 to I/O7 become write mode and I/O8 to I/O15 become no write mode, and when $\overline{WEL}$ set high and $\overline{WEU}$ set low, I/O0 to I/O7 become no write mode and I/O8 to I/O15 become write mode. The write cycle that byte control is capable are RAM write cycle, block write cycle, load write mask register cycle and load color register cycle. The byte control write cycle is capable to execute early write, delay write, read-modify-write and page mode. But write mask in new mask mode, flash write, transfer and refresh cycle can not execute byte control.

SAM Port Operation

Serial Read Cycle

SAM port is in read mode when the previous data transfer cycle is a read transfer cycle. Access is synchronized with SC rising, and SAM data is output from SI/O. When $\overline{SE}$ is set high, SI/O becomes high impedance, and the internal pointer is incremented by the SC rising. After indicating the last address (address 255), the internal pointer indicates address 0 at the next access.

Serial Write Cycle

If previous data transfer cycle is masked write transfer cycle, SAM port goes into write mode. In this cycle, SI/O data is fetched into data register at the SC rising edge like in the serial read cycle. If $\overline{SE}$ is high, SI/O data isn't fetched into data register. The internal pointer is incremented by the SC rising, so $\overline{SE}$ high can be used as mask data for SAM. After indicating the last address (address 255), the internal pointer indicates address 0 at the next access.

Refresh

RAM Refresh

RAM, which is composed of dynamic circuits, requires refresh cycle to retain data. Refresh is executed by accessing all 512 row addresses within 8 ms. There are three refresh cycles: (1) $\overline{RAS}$-only refresh cycle, (2) $\overline{CAS}$-before-$\overline{RAS}$ (CBRN, CBRS, and CBRR) refresh cycle, and (3) Hidden refresh cycle. Besides them, the cycles which activate $\overline{RAS}$, such as read/write cycles or transfer cycles, can also refresh the row address. Therefore, no refresh cycle is required when all row addresses are accessed within 8 ms.

(1) $\overline{RAS}$-Only Refresh Cycle: $\overline{RAS}$-only refresh cycle is executed by activating only the $\overline{RAS}$ cycle with $\overline{CAS}$ fixed to high after inputting the row address (= refresh address) from external circuits. To distinguish this cycle from a data transfer cycle, $\overline{DT}/\overline{OE}$ must be high at the falling edge of $\overline{RAS}$.

(2) CBR Refresh Cycle: CBR refresh cycle (CBRN, CBRS and CBRR) are set by activating $\overline{CAS}$ before $\overline{RAS}$. In this cycle, the refresh address need not to be input through external circuits because it is input through an internal refresh counter. In this cycle, output is in high impedance and power dissipation is lowered because $\overline{CAS}$ circuits don't operate.

(3) Hidden Refresh Cycle: Hidden refresh cycle executes CBR refresh with the data output by reactivating $\overline{RAS}$ when $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ keep low in normal RAM read cycles.

SAM Refresh

SAM parts (data register, shift resister and selector), organized as fully static circuitry, require no refresh.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	−0.5 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{CC}	4.5	5.0	5.5	V	1
Input high voltage	V_{IH}	2.4	—	6.5	V	1
Input low voltage	V_{IL}	−0.5*2	—	0.8	V	1

Notes: 1. All voltage referenced to V_{SS}
2. −3.0 V for pulse width ≤ 10 ns.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

		HM5316123 -7		-8		-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**
Operating current	I_{CC1}	—	120	—	110	—	100	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min; SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC7}	—	195	—	175	—	160	mA	$\overline{SE}$ = V_{IL}, SC cycling; t_{SCC} = min
Block write current	I_{CC1BW}	—	125	—	115	—	100	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min; SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC7BW}	—	200	—	180	—	160	mA	$\overline{SE}$ = V_{IL}, SC cycling; t_{SCC} = min
Standby current	I_{CC2}	—	7	—	7	—	7	mA	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}; SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC8}	—	85	—	75	—	70	mA	$\overline{SE}$ = V_{IL}, SC cycling; t_{SCC} = min
$\overline{RAS}$-only refresh current	I_{CC3}	—	115	—	105	—	90	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IH}; SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC9}	—	185	—	165	—	150	mA	t_{RC} = min; $\overline{SE}$ = V_{IL}, SC cycling; t_{SCC} = min
Fast page mode current *3	I_{CC4}	—	125	—	120	—	115	mA	$\overline{CAS}$ cycling; $\overline{RAS}$ = V_{IL}; SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC10}	—	200	—	185	—	175	mA	t_{PC} = min; $\overline{SE}$ = V_{IL}, SC cycling; t_{SCC} = min
Fast page mode block write current *3	I_{CC4BW}	—	145	—	135	—	130	mA	$\overline{CAS}$ cycling; $\overline{RAS}$ = V_{IL}; SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC10BW}	—	220	—	205	—	195	mA	t_{PC} = min; $\overline{SE}$ = V_{IL}, SC cycling; t_{SCC} = min
$\overline{CAS}$-before $\overline{RAS}$ refresh current	I_{CC5}	—	85	—	75	—	65	mA	$\overline{RAS}$ cycling; t_{RC} = min; SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC11}	—	155	—	140	—	125	mA	$\overline{SE}$ = V_{IL}, SC cycling; t_{SCC} = min
Data transfer current	I_{CC6}	—	130	—	120	—	110	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min; SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC12}	—	205	—	185	—	165	mA	$\overline{SE}$ = V_{IL}, SC cycling; t_{SCC} = min
Input leakage current	I_{LI}	−10	10	−10	10	−10	10	µA	
Output leakage current	I_{LO}	−10	10	−10	10	−10	10	µA	
Output high voltage	V_{OH}	2.4	—	2.4	—	2.4	—	V	I_{OH} = −1 mA
Output low voltage	V_{OL}	—	0.4	—	0.4	—	0.4	V	I_{OL} = 2.1 mA

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed once while $\overline{RAS}$ is low and $\overline{CAS}$ is high.
3. Address can be changed once in 1 page cycle (t_{PC}).

Capacitance (Ta = 25°C, V_{CC} = 5 V±10 %, f = 1 MHz, Bias: Clock, I/O = V_{CC}, address=V_{SS})

Parameter	Symbol	Typ	Max	Unit	Note
Input capacitance (Address)	C_{I1}	—	5	pF	1
Input capacitance (Clocks)	C_{I2}	—	5	pF	1
Output capacitance (I/O, SI/O, QSF)	$C_{I/O}$	—	7	pF	1

Notes: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V) *1, *16

Test Conditions

- Input rise and fall times: 5ns
- Input pulse levels: V_{SS} to 3.0 V
- Input timing reference levels: 0.8 V, 2.4 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: RAM 1TTL+CL(50PF)
  SAM, QSF 1TTL+CL(30PF)
  (Including scope and jig)

Common Parameter

		HM5316123 -7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Random read or write cycle time	t_{RC}	130	—	150	—	180	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	50	—	60	—	70	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10000	80	10000	100	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	—	20	—	25	—	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	12	—	15	—	15	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	20	75	ns	2
$\overline{RAS}$ hold time referenced to $\overline{CAS}$	t_{RSH}	20	—	20	—	25	—	ns	
$\overline{CAS}$ hold time referenced to $\overline{RAS}$	t_{CSH}	70	—	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	10	—	ns	

Common Parameter (cont)

Parameter	Symbol	HM5316123 -7 Min	-7 Max	-8 Min	-8 Max	-10 Min	-10 Max	Unit	Notes
Transition time (rise to fall)	t_T	3	50	3	50	3	50	ns	3
Refresh period	t_{REF}	—	8	—	8	—	8	ms	
$\overline{DT}$ to $\overline{RAS}$ setup time	t_{DTS}	0	—	0	—	0	—	ns	
$\overline{DT}$ to $\overline{RAS}$ hold time	t_{DTH}	10	—	10	—	10	—	ns	
DSF1 to $\overline{RAS}$ setup time	t_{FSR}	0	—	0	—	0	—	ns	
DSF1 to $\overline{RAS}$ hold time	t_{RFH}	10	—	10	—	10	—	ns	
DSF1 to $\overline{CAS}$ setup time	t_{FSC}	0	—	0	—	0	—	ns	
DSF1 to $\overline{CAS}$ hold time	t_{CFH}	12	—	15	—	15	—	ns	
Data-in to $\overline{CAS}$ delay time	t_{DZC}	0	—	0	—	0	—	ns	4
Data-in to $\overline{OE}$ delay time	t_{DZO}	0	—	0	—	0	—	ns	4
Output buffer turn-off delay referenced to $\overline{CAS}$	t_{OFF1}	—	15	—	20	—	20	ns	5
Output buffer turn-off delay referenced to $\overline{OE}$	t_{OFF2}	—	15	—	20	—	20	ns	5

Read Cycle (RAM), Page Mode Read Cycle

		HM5316123 -7		-8		-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Access time from $\overline{RAS}$	t_{RAC}	—	70	—	80	—	100	ns	6, 7
Access time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	25	ns	7, 8
Access time from $\overline{OE}$	t_{OAC}	—	20	—	20	—	25	ns	7
Address access time	t_{AA}	—	35	—	40	—	45	ns	7, 9
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	0	—	ns	10
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0	—	5	—	10	—	ns	10
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	15	55	ns	2
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	—	40	—	45	—	ns	
Column address to $\overline{CAS}$ lead time	t_{CAL}	35	—	40	—	45	—	ns	
Page mode cycle time	t_{PC}	45	—	50	—	55	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	7	—	10	—	10	—	ns	
Access time from $\overline{CAS}$ precharge	t_{ACP}	—	40	—	45	—	50	ns	
Page mode $\overline{RAS}$ pulse width	t_{RASP}	70	100000	80	100000	100	100000	ns	

Write Cycle (RAM), Page Mode Write Cycle, Color Register Set Cycle

		HM5316123 -7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	11
Write command hold time	t_{WCH}	12	—	15	—	15	—	ns	
Write command pulse width	t_{WP}	12	—	15	—	15	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	—	20	—	20	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	—	20	—	20	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	12
Data-in hold time	t_{DH}	12	—	15	—	15	—	ns	12
$\overline{WE}$ to $\overline{RAS}$ setup time	t_{WS}	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ hold time	t_{WH}	10	—	10	—	10	—	ns	
Mask data to $\overline{RAS}$ setup time	t_{MS}	0	—	0	—	0	—	ns	
Mask data to $\overline{RAS}$ hold time	t_{MH}	10	—	10	—	10	—	ns	
$\overline{OE}$ hold time referenced to $\overline{WE}$	t_{OEH}	15	—	20	—	20	—	ns	
Page mode cycle time	t_{PC}	45	—	50	—	55	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	7	—	10	—	10	—	ns	
$\overline{CAS}$ to data-in delay time	t_{CDD}	15	—	20	—	20	—	ns	13
Page mode $\overline{RAS}$ pulse width	t_{RASP}	70	100000	80	100000	100	100000	ns	

Read-Modify-Write Cycle

		HM5316123 -7		-8		-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Read-modify-write cycle time	t_{RWC}	180	—	200	—	230	—	ns	
$\overline{RAS}$ pulse width (read-modify-write cycle)	t_{RWS}	120	10000	130	10000	150	10000	ns	
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	40	—	45	—	50	—	ns	14
Column address to $\overline{WE}$ delay time	t_{AWD}	60	—	65	—	70	—	ns	14
$\overline{OE}$ to data-in delay time	t_{ODD}	15	—	20	—	20	—	ns	12
Access time from $\overline{RAS}$	t_{RAC}	—	70	—	80	—	100	ns	6, 7
Access time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	25	ns	7, 8
Access time from $\overline{OE}$	t_{OAC}	—	20	—	20	—	25	ns	7
Address access time	t_{AA}	—	35	—	40	—	45	ns	7, 9
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	15	55	ns	
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	—	20	—	20	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	—	20	—	20	—	ns	
Write command pulse width	t_{WP}	12	—	15	—	15	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	12
Data-in hold time	t_{DH}	12	—	15	—	15	—	ns	12
$\overline{OE}$ hold time referenced to $\overline{WE}$	t_{OEH}	15	—	20	—	20	—	ns	

Refresh Cycle

		HM5316123 -7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10	—	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	—	10	—	10	—	ns	

Flash Write Cycle, Block Write Cycle, and Register Read Cycle

		HM5316123 -7		8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{CAS}$ to data-in delay time	t_{CDD}	15	—	20	—	20	—	ns	13
$\overline{OE}$ to data-in delay time	t_{ODD}	15	—	20	—	20	—	ns	13

CBR Refresh with Register Reset

		HM5316123 -7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Split transfer setup time	t_{STS}	20	—	20	—	25	—	ns	
Split transfer hold time referenced to $\overline{RAS}$	t_{RST}	70	—	80	—	100	—	ns	

Read Transfer Cycle

		HM5316123 -7		-8		-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
$\overline{DT}$ hold time referenced to $\overline{RAS}$	t_{RDH}	60	10000	65	10000	80	10000	ns	
$\overline{DT}$ hold time referenced to $\overline{CAS}$	t_{CDH}	20	—	20	—	25	—	ns	
$\overline{DT}$ hold time referenced to column address	t_{ADH}	25	—	30	—	30	—	ns	
$\overline{DT}$ precharge time	t_{DTP}	20	—	20	—	30	—	ns	
$\overline{DT}$ to $\overline{RAS}$ delay time	t_{DRD}	60	—	70	—	80	—	ns	
SC to $\overline{RAS}$ setup time	t_{SRS}	15	—	20	—	30	—	ns	
1st SC to $\overline{RAS}$ hold time	t_{SRH}	70	—	80	—	100	—	ns	
1st SC to $\overline{CAS}$ hold time	t_{SCH}	25	—	25	—	25	—	ns	
1st SC to column address hold time	t_{SAH}	40	—	45	—	50	—	ns	
Last SC to $\overline{DT}$ delay time	t_{SDD}	5	—	5	—	5	—	ns	
1st SC to $\overline{DT}$ hold time	t_{SDH}	10	—	13	—	15	—	ns	
$\overline{DT}$ to QSF delay time	t_{DQD}	—	30	—	35	—	35	ns	15
QSF hold time referenced to $\overline{DT}$	t_{DQH}	5	—	5	—	5	—	ns	
Serial data-in to 1st SC delay time	t_{SZS}	0	—	0	—	0	—	ns	
Serial clock cycle time	t_{SCC}	25	—	28	—	30	—	ns	
SC pulse width	t_{SC}	5	—	10	—	10	—	ns	
SC precharge time	t_{SCP}	10	—	10	—	10	—	ns	
SC access time	t_{SCA}	—	20	—	23	—	25	ns	15
Serial data-out hold time	t_{SOH}	5	—	5	—	5	—	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	15	—	15	—	ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	15	55	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	—	40	—	45	—	ns	
$\overline{RAS}$ to QSF delay time	t_{RQD}	—	70	—	75	—	85	ns	15
$\overline{CAS}$ to QSF delay time	t_{CQD}	—	35	—	35	—	35	ns	15

Read Transfer Cycle (cont)

Parameter	Symbol	HM5316123 -7 Min	-7 Max	-8 Min	-8 Max	-10 Min	-10 Max	Unit	Notes
QSF hold time referenced to $\overline{RAS}$	t_{RQH}	20	—	20	—	25	—	ns	
QSF hold time referenced to $\overline{CAS}$	t_{CQH}	5	—	5	—	5	—	ns	

Masked Write Transfer Cycle

Parameter	Symbol	HM5316123 -7 Min	-7 Max	-8 Min	-8 Max	-10 Min	-10 Max	Unit	Notes
SC setup time referenced to $\overline{RAS}$	t_{SRS}	15	—	20	—	30	—	ns	
$\overline{RAS}$ to SC delay time	t_{SRD}	20	—	25	—	25	—	ns	
Serial output buffer turn-off time referenced to $\overline{RAS}$	t_{SRZ}	10	30	10	35	10	50	ns	
$\overline{RAS}$ to serial data-in delay time	t_{SID}	30	—	35	—	50	—	ns	
$\overline{RAS}$ to QSF delay time	t_{RQD}	—	70	—	75	—	85	ns	15
$\overline{CAS}$ to QSF delay time	t_{CQD}	—	35	—	35	—	35	ns	15
QSF hold time referenced to $\overline{RAS}$	t_{RQH}	20	—	20	—	25	—	ns	
QSF hold time referenced to $\overline{CAS}$	t_{CQH}	5	—	5	—	5	—	ns	
Serial clock cycle time	t_{SCC}	25	—	28	—	30	—	ns	
SC pulse width	t_{SC}	5	—	10	—	10	—	ns	
SC precharge time	t_{SCP}	10	—	10	—	10	—	ns	
SC access time	t_{SCA}	—	20	—	23	—	25	ns	15
Serial data-out hold time	t_{SOH}	5	—	5	—	5	—	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	15	—	15	—	ns	

Split Read Transfer Cycle, Masked Split Write Transfer Cycle

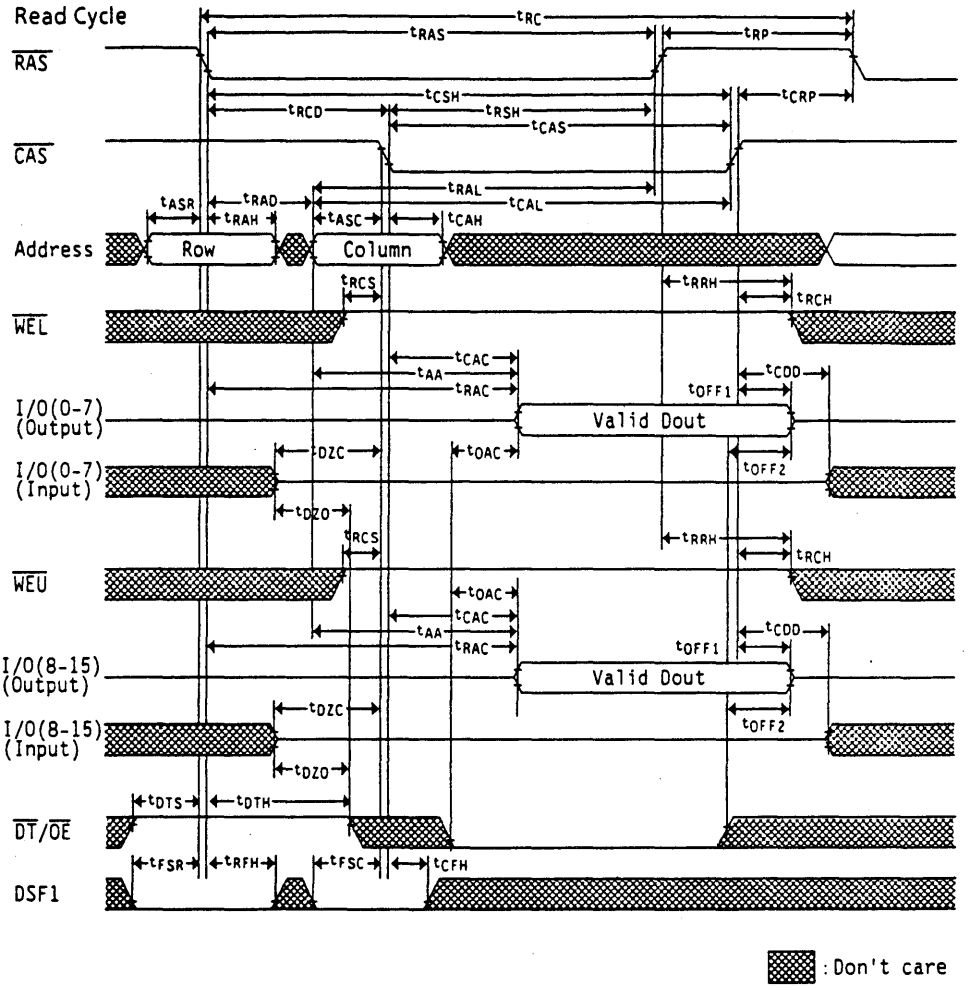
		HM5316123 -7		-8		-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Split transfer setup time	t_{STS}	20	—	20	—	25	—	ns	
Split transfer hold time referenced to $\overline{RAS}$	t_{RST}	70	—	80	—	100	—	ns	
Split transfer hold time referenced to $\overline{CAS}$	t_{CST}	20	—	20	—	25	—	ns	
Split transfer hold time referenced to column address	t_{AST}	35	—	40	—	45	—	ns	
SC to QSF delay time	t_{SQD}	—	30	—	30	—	30	ns	15
QSF hold time referenced to SC	t_{SQH}	5	—	5	—	5	—	ns	
Serial clock cycle time	t_{SCC}	25	—	28	—	30	—	ns	
SC pulse width	t_{SC}	5	—	10	—	10	—	ns	
SC precharge time	t_{SCP}	10	—	10	—	10	—	ns	
SC access time	t_{SCA}	—	20	—	23	—	25	ns	15
Serial data-out hold time	t_{SOH}	5	—	5	—	5	—	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	15	—	15	—	ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	15	55	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	—	40	—	45	—	ns	

Serial Read Cycle, Serial Write Cycle

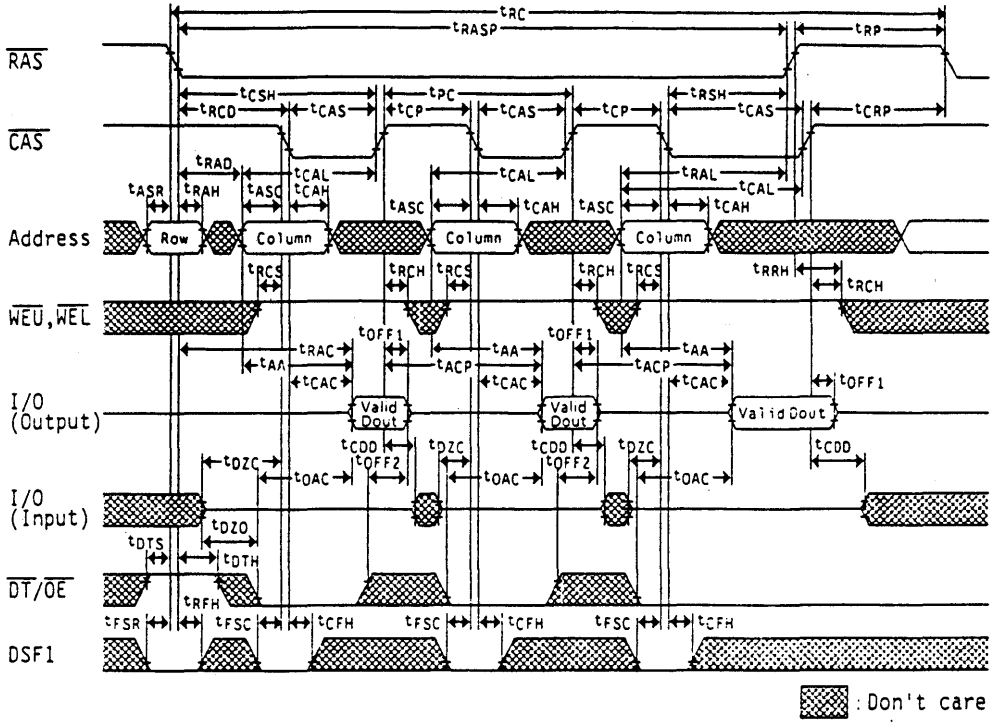
		HM5316123 -7		-8		-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Serial clock cycle time	t_{SCC}	25	—	28	—	30	—	ns	
SC pulse width	t_{SC}	5	—	10	—	10	—	ns	
SC precharge width	t_{SCP}	10	—	10	—	10	—	ns	
Access time from SC	t_{SCA}	—	20	—	23	—	25	ns	15
Access time from $\overline{SE}$	t_{SEA}	—	17	—	20	—	25	ns	15
Serial data-out hold time	t_{SOH}	5	—	5	—	5	—	ns	
Serial output buffer turn-off time referenced to $\overline{SE}$	t_{SHZ}	—	15	—	20	—	20	ns	5,17
$\overline{SE}$ to serial output in low-Z	t_{SLZ}	0	—	0	—	0	—	ns	5,17
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	15	—	15	—	ns	
Serial write enable setup time	t_{SWS}	0	—	0	—	0	—	ns	
Serial wrtie enable hold time	t_{SWH}	15	—	15	—	15	—	ns	
Serial write disable setup time	t_{SWIS}	0	—	0	—	0	—	ns	
Serial write disable hold time	t_{SWIH}	15	—	15	—	15	—	ns	

Notes:
1. AC measurements assume t_T = 5 ns.
2. When $t_{RCD} > t_{RCD}$ (max) and $t_{RAD} > t_{RAD}$ (max), access time is specified by t_{CAC} or t_{AA}.
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition time t_T is measured between V_{IH} and V_{IL}.
4. Data input must be floating before output buffer is turned on. In read cycle, read-modify-write cycle and delayed write cycle, either t_{DZC} (min) or t_{DZO} (min) must be satisfied.
5. t_{OFF1} (max), t_{OFF2} (max), t_{SHZ} (max) and t_{SLZ} (min) are defined as the time at which the output acheives the open circuit condition (V_{OH} – 100 mV, V_{OL} + 100 mV). This parameter is sampled and not 100% tested.
6. Assume that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
7. Measured with a load circuit equivalent to 1 TTL loads and 50 pF.
8. When $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max), access time is specified by t_{CAC}.
9. When $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max), access time is specified by t_{AA}.
10. If either t_{RCH} or t_{RRH} is satisfied, operation is guaranteed.
11. When $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle, and I/O pins remain in an open circuit (high impedance) condition.
12. These parameters are specified by the later falling edge of $\overline{CAS}$ or $\overline{WEU}$ and $\overline{WEL}$.
13. Either t_{CDD} (min) or t_{ODD} (min) must be satisfied because output buffer must be turned off by $\overline{CAS}$ or $\overline{OE}$ prior to applying data to the device when output buffer is on.
14. When $t_{AWD} \geq t_{AWD}$ (min) and $t_{CWD} \geq t_{CWD}$ (min) in read-modify-write cycle, the data of the selected address outputs to an I/O pin and input data is written into the selected address. t_{ODD} (min) must be satisfied because output buffer must be turned off by $\overline{OE}$ prior to applying data to the device.
15. Measured with a load circuit equivalent to 1 TTL loads and 30 pF.
16. After power-up, pause for 100 µs or more and execute at least 8 initialization cycle (normal memory cycle or refresh cycle), then start operation. Hitachi recommends that least 8 initialization cycle is the CBRR for internal register reset. This CBRR need not t_{STS} and t_{RST}.
17. When t_{SHZ} and t_{SLZ} are measured in the same V_{CC} and Ta condition and tr and tf of $\overline{SE}$ are less than 5 ns, $t_{SHZ} \leq t_{SLZ}$ +5 ns. This parameter is sampled and not 100% tested.
18. When both $\overline{WEU}$ and $\overline{WEL}$ go low at the same time, all 16-bits data are written into the device, $\overline{WEU}$ and $\overline{WEL}$ cannot be staggered within the same write cycles.
19. After power-up, QSF output may be High-Z, so 1 sc cycle is needed to be Low-Z it.
20. DSF2 pin is open pin, but Hitachi recommends it is fixed low in all operation for the addition mode in future.

■ Timing Waveforms



Fast Page Mode Read Cycle



Write Cycle

The write cycle state table as shown below is applied to early write, delayed write, page mode write, and read-modify write.

Write Cycle State Table

MNEU	Cycle	$\overline{RAS}$ DSF1 W1	$\overline{CAS}$ DSF1 W2	$\overline{RAS}$ $\overline{WEU}$, $\overline{WEL}$ W3	$\overline{RAS}$ I/O W4	$\overline{CAS}$ I/O W5
RWM	Write mask (new/old) Write DQs to I/Os	0	0	0	Write mask*1	Valid data
BWM	Write mask (new/old) Block write	0	1	0	Write mask*2	Column mask*2
RW	Normal write (no mask)	0	0	1	Don't care*1	Valid data
BW	Block write (no mask)	0	1	1	Don't care*2	Column mask*2
LMR*4	Load write mask resister	1	0	1	Don't care	Write mask data*3
LCR*4	Load color resister	1	1	1	Don't care	Color data

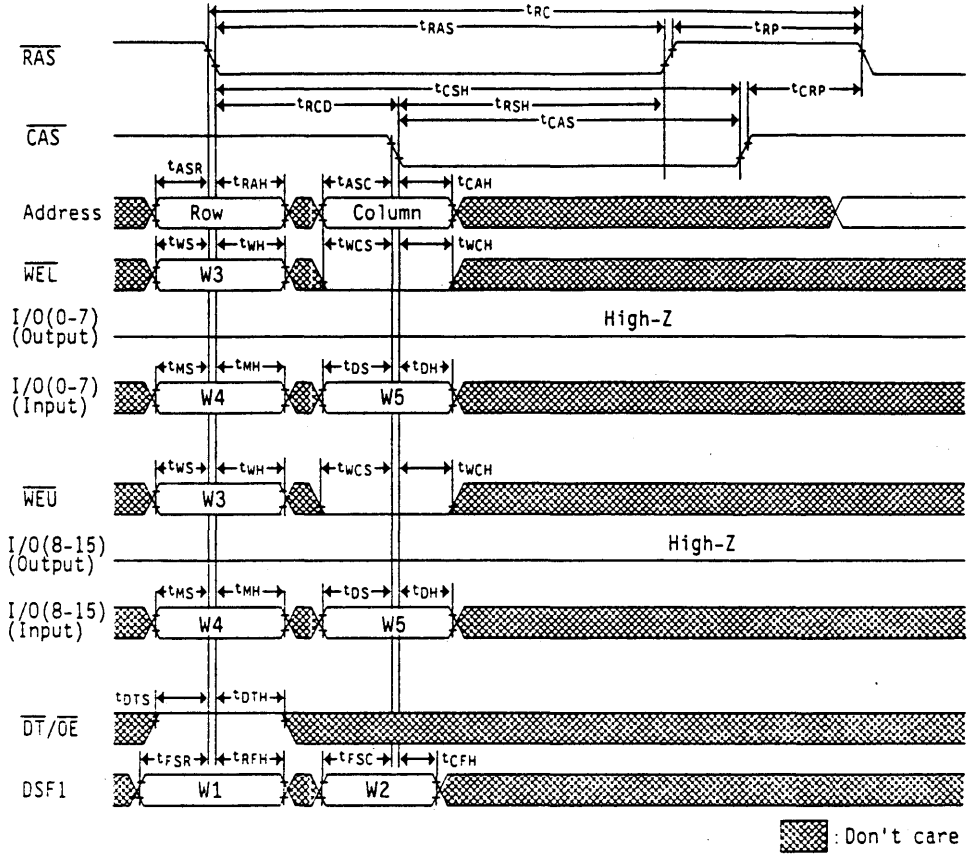
Notes: 1.

$\overline{WEU}$, $\overline{WEL}$	Mode	I/O data/$\overline{RAS}$
Either Low	New Mask Mode	Mask
	Persistent Mask Mode	Don't care (mask register used)
Both High	No mask	Don't care

I/O Mask Data (In new mask mode)
Low: Mask
High: Non Mask
In persistent mask mode, I/O don't care

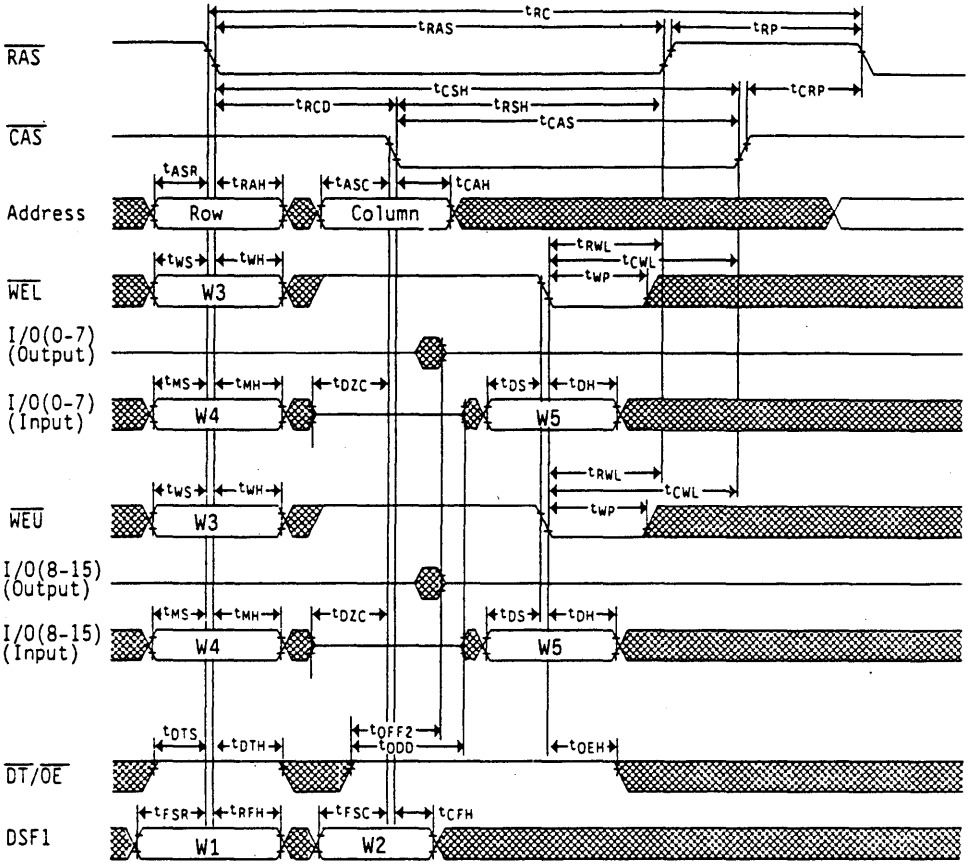
2. Reference Figure 2 Use of Block Write.
3. I/O Write Mask Data
   Low: Mask
   High: Non Mask
4. Column Address: Don't care

Early Write Cycle



W1 to W5: See Write Cycle State Table for the logic states.

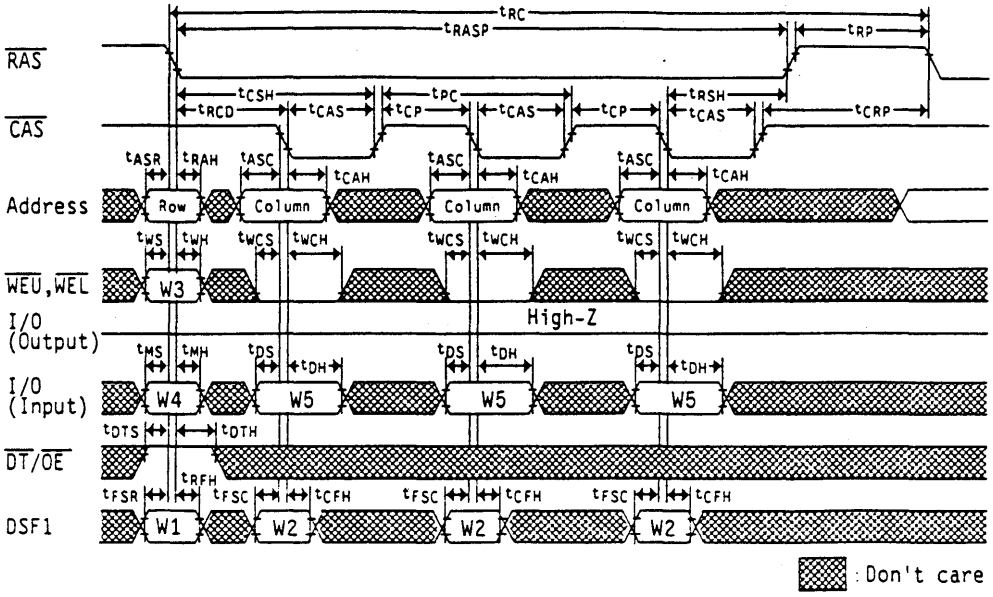
Delayed Write Cycle



: Don't care

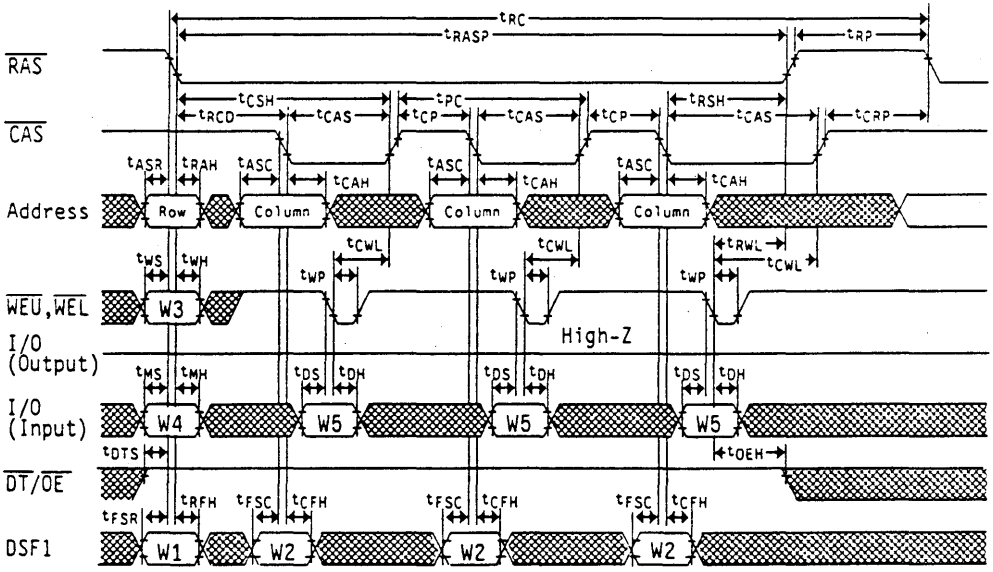
W1 to W5: See Write Cycle State Table for the logic states.

Fast Page Mode Write Cycle (Early Write)



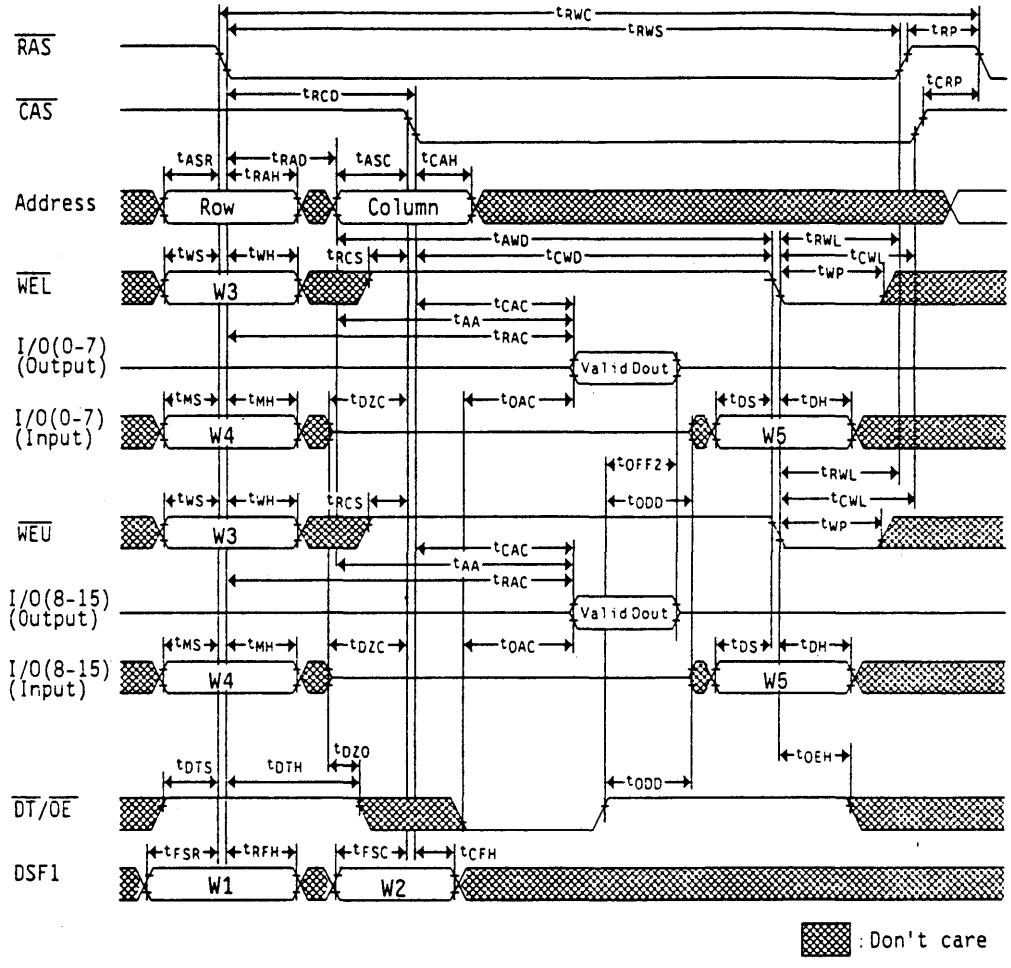
W1 to W5: See Write Cycle State Table for the logic states.

Fast Page Mode Write Cycle (Delayed Write)



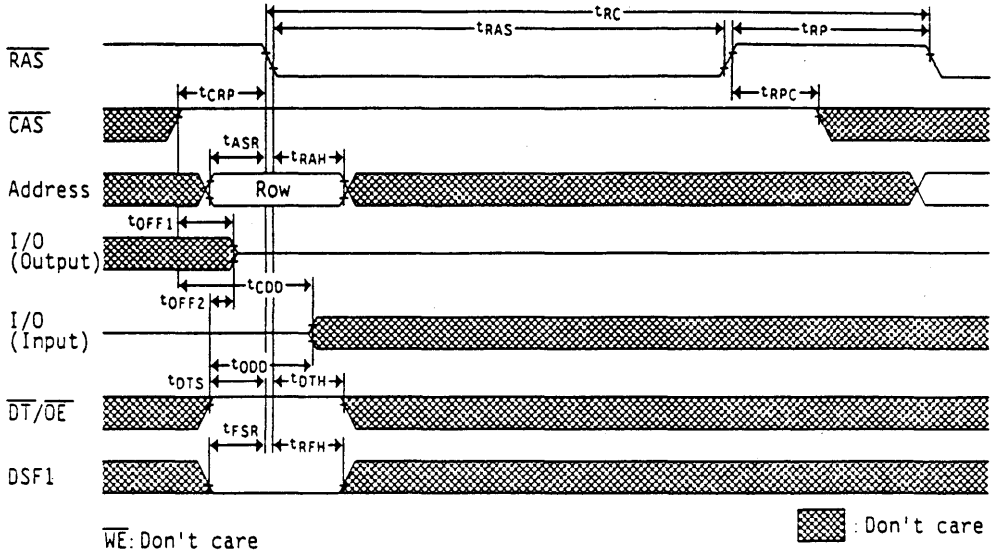
W1 to W5: See Write Cycle State Table for the locgic states.

Read- Modify-Write Cycle



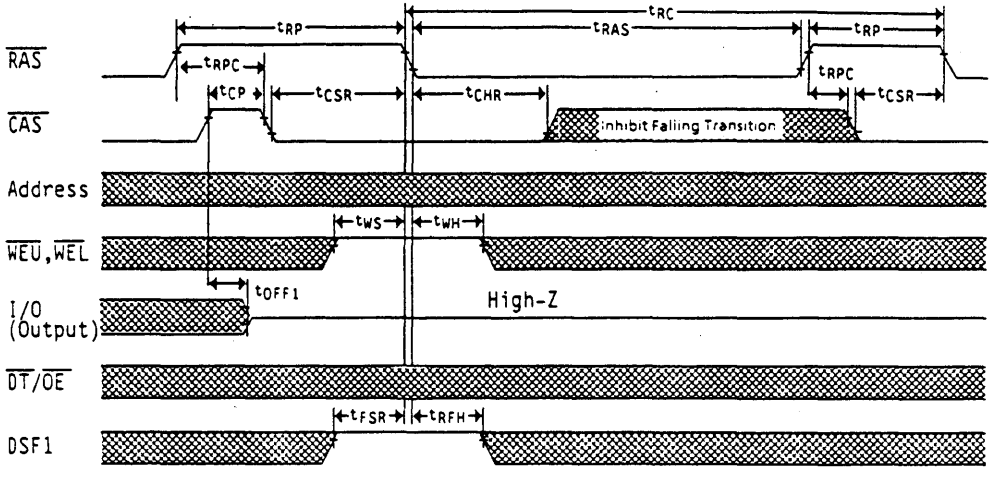
W1 to W5: See Write Cycle State Table for the logic states.

- $\overline{RAS}$-Only Refresh Cycle



WE: Don't care

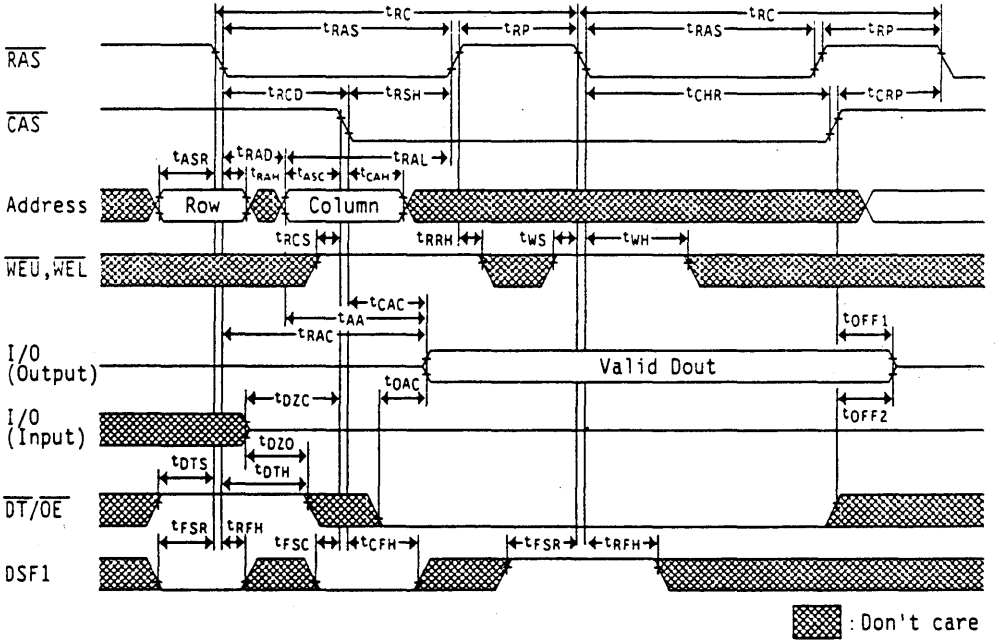
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle (CBRN)



Note: SC : Don't care

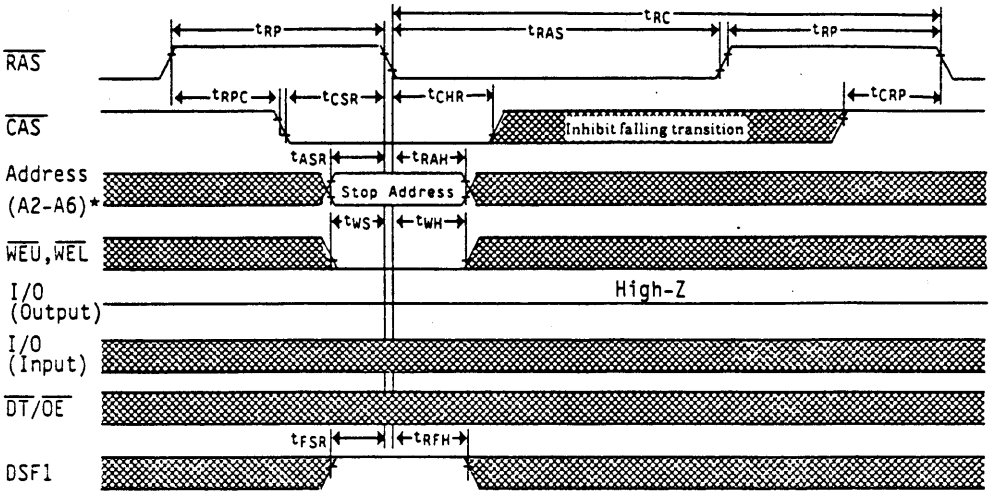
: Don't care

Hidden Refresh Cycle



: Don't care

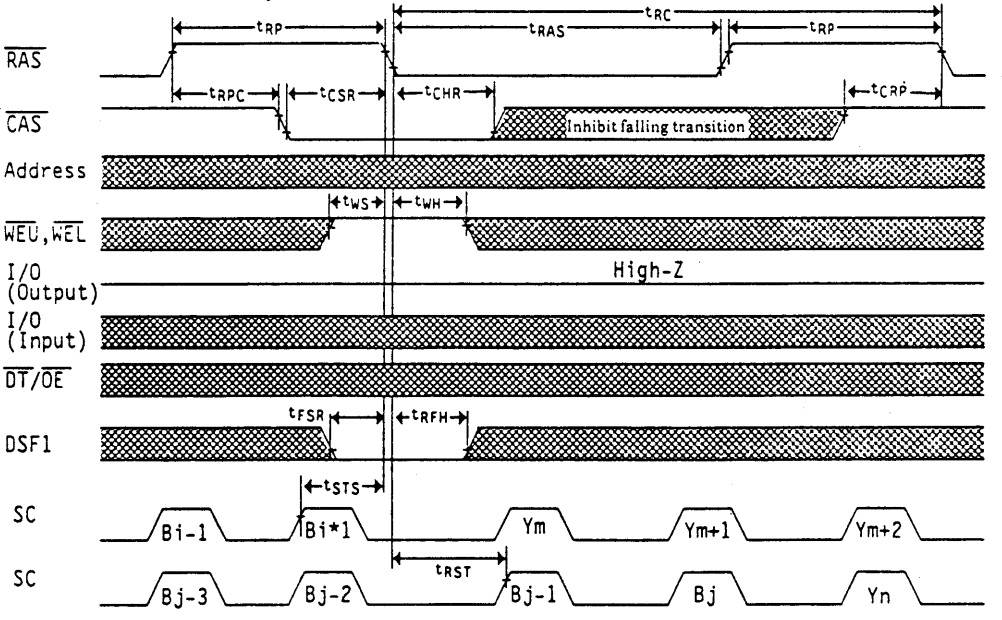
$\overline{CAS}$-Before-$\overline{RAS}$ Set Cycle (CBRS)



Note: A0, A1, A7: Don't care
SC : Don't care

: Don't care

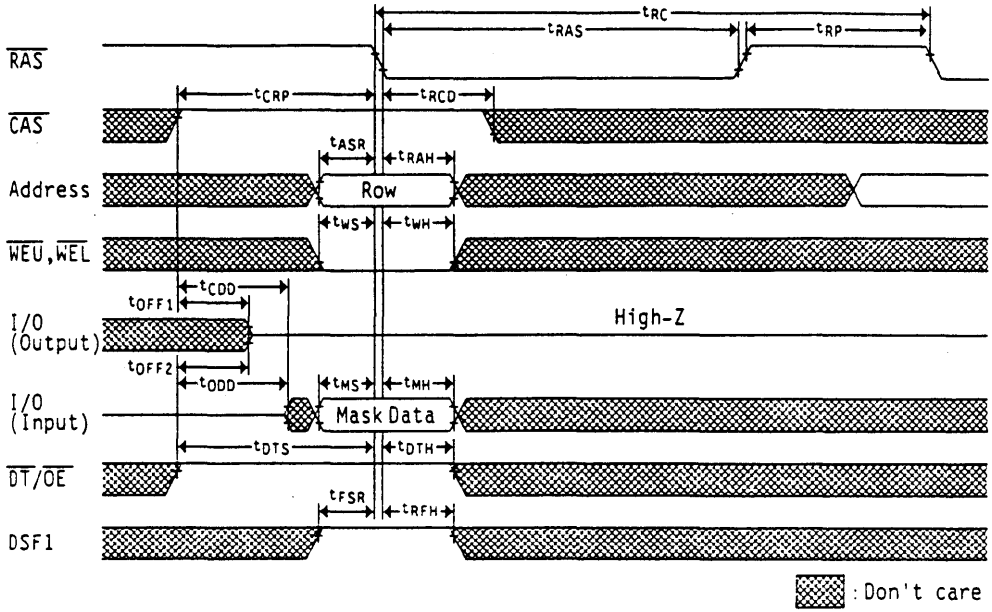
$\overline{CAS}$-Before-$\overline{RAS}$ Reset Cycle (CBRR)



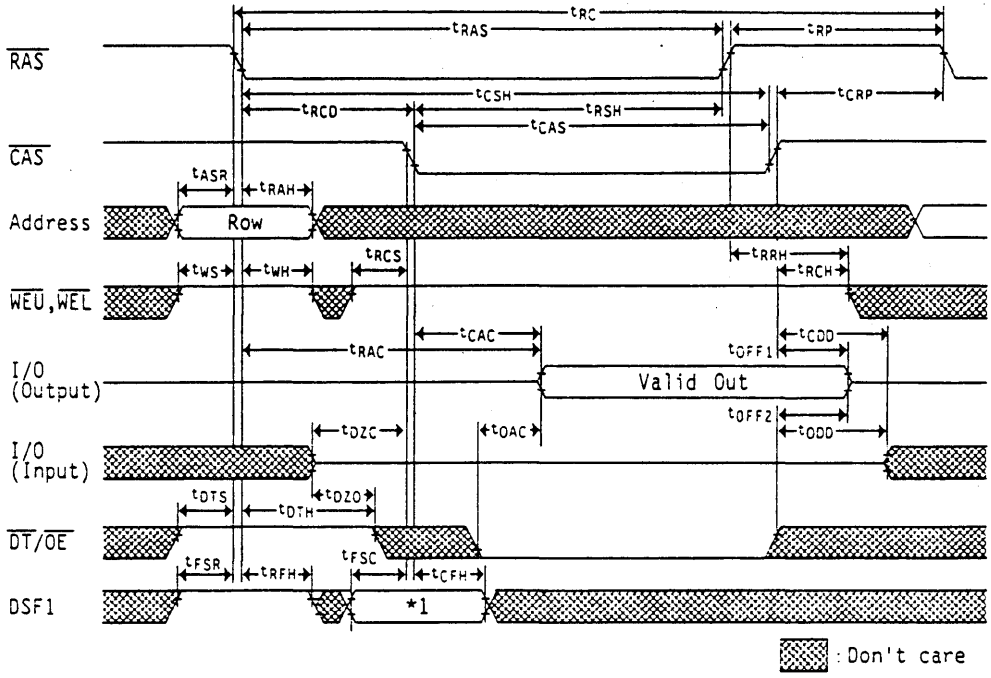
Note: 1. Bi, Bj initiate the boundary addresses.
2. Ym, Yn are the SAM start address in before SRT/MSWT.

: Don't care

Flash Write Cycle



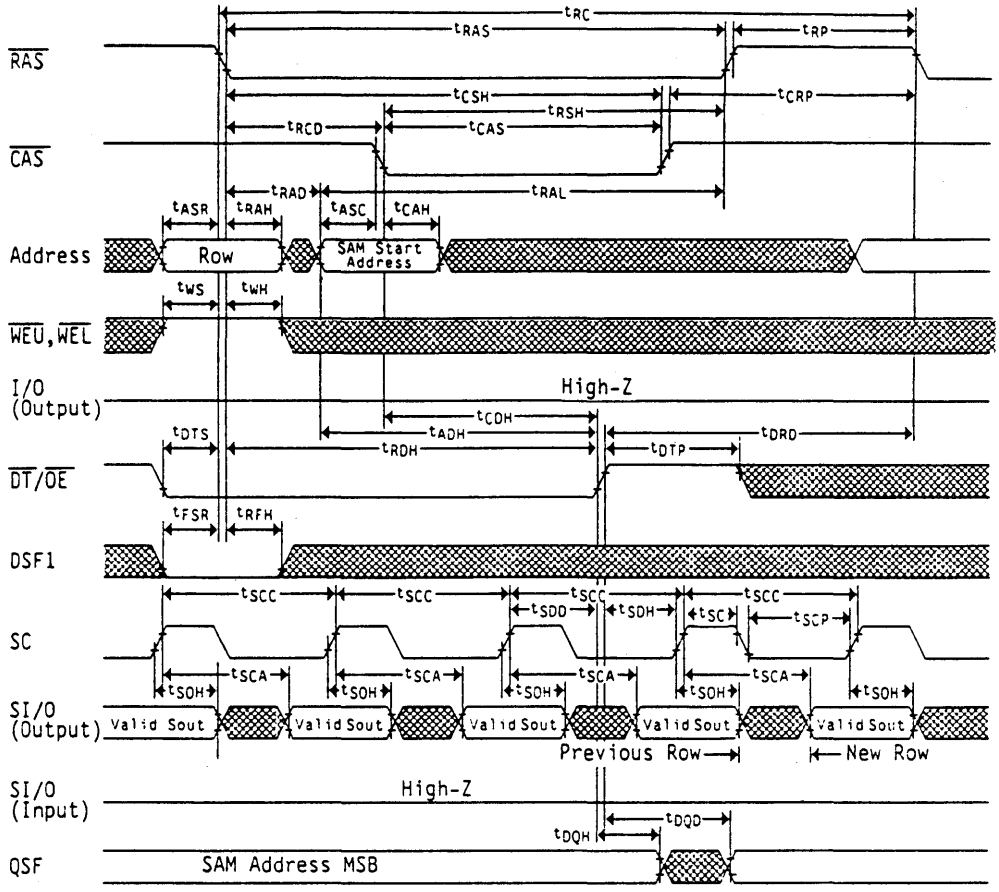
Register Read Cycle (Mask data, Color data)



Note: 1. State of DSF1 at falling edge of $\overline{CAS}$

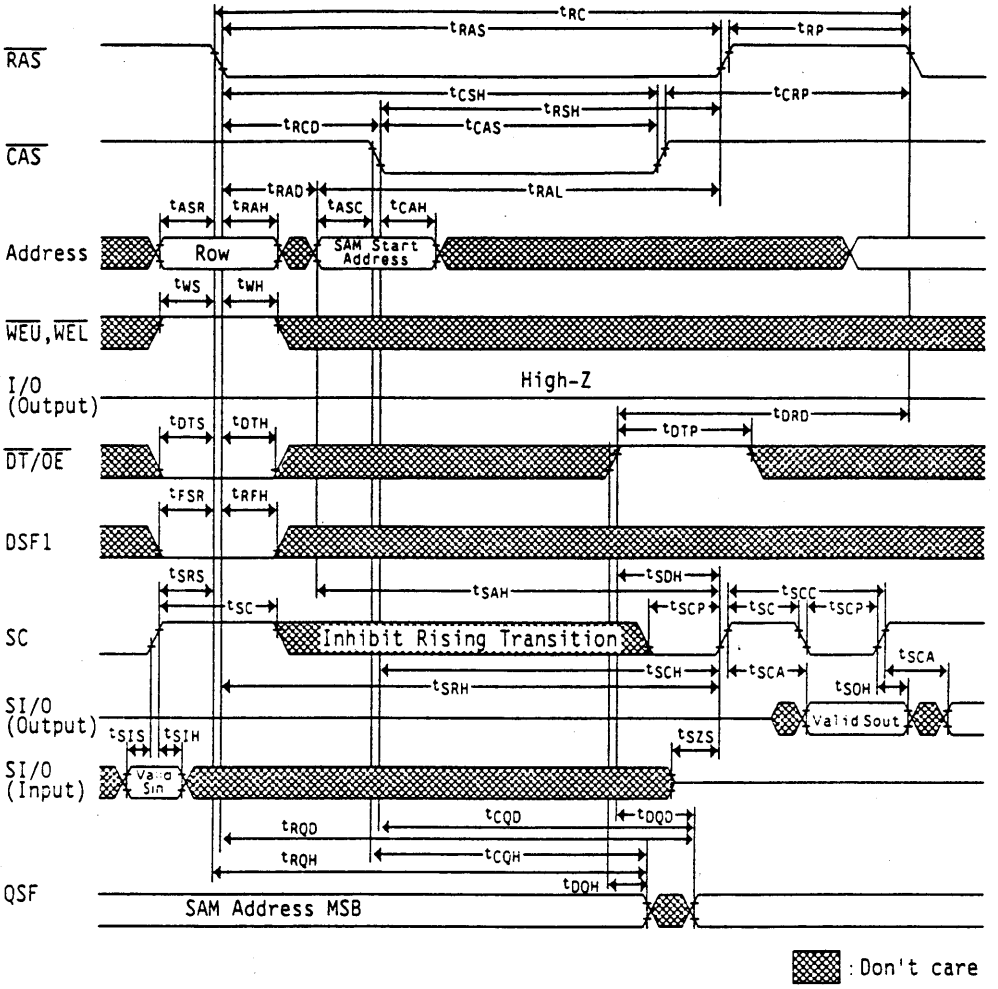
State	0	1
Accessed Data	Mask Data (LMR)	Color Data (LCR)

Read Transfer Cycle-1

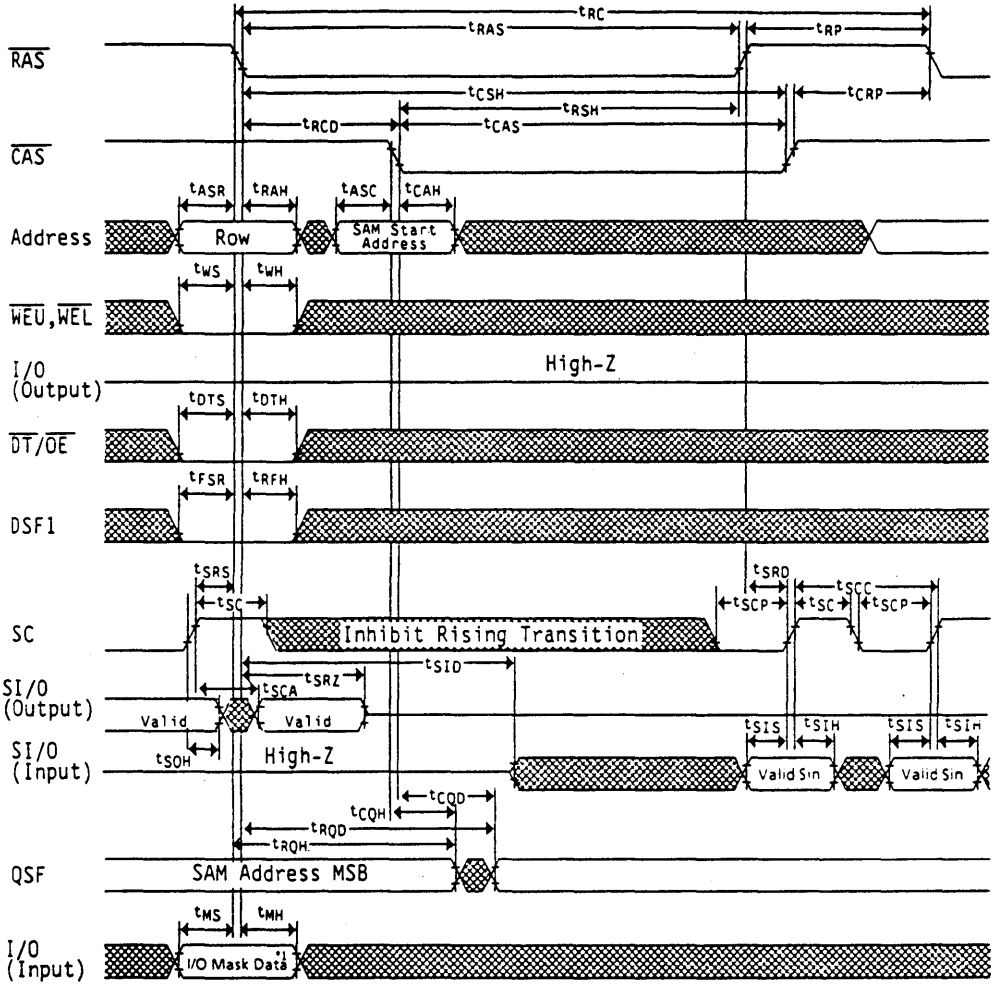


: Don't care

Read Transfer Cycle – 2



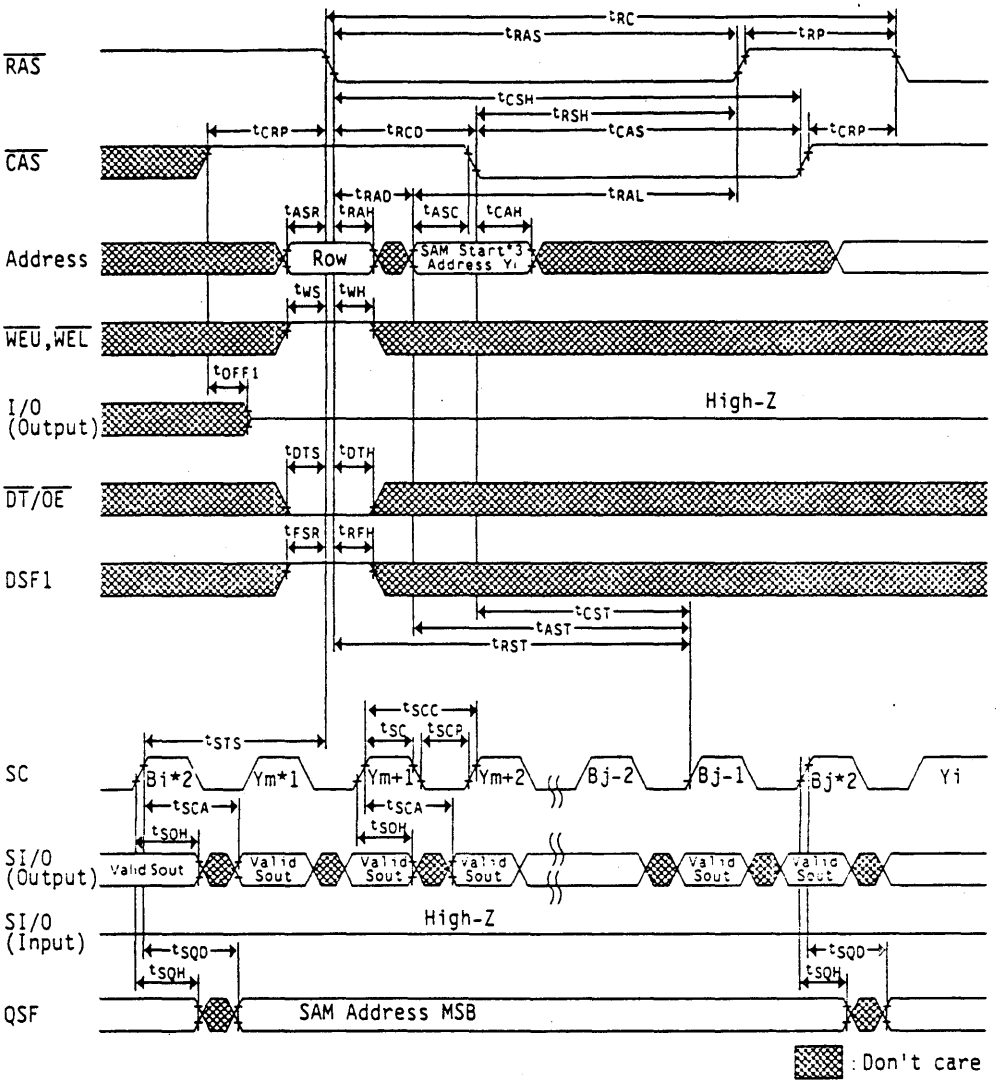
Masked Write Transfer Cycle



Note: 1. I/O Mask Data(In new mask mode)
Low: Mask
High: Non Mask
I/O: don't care in persistent mask mode

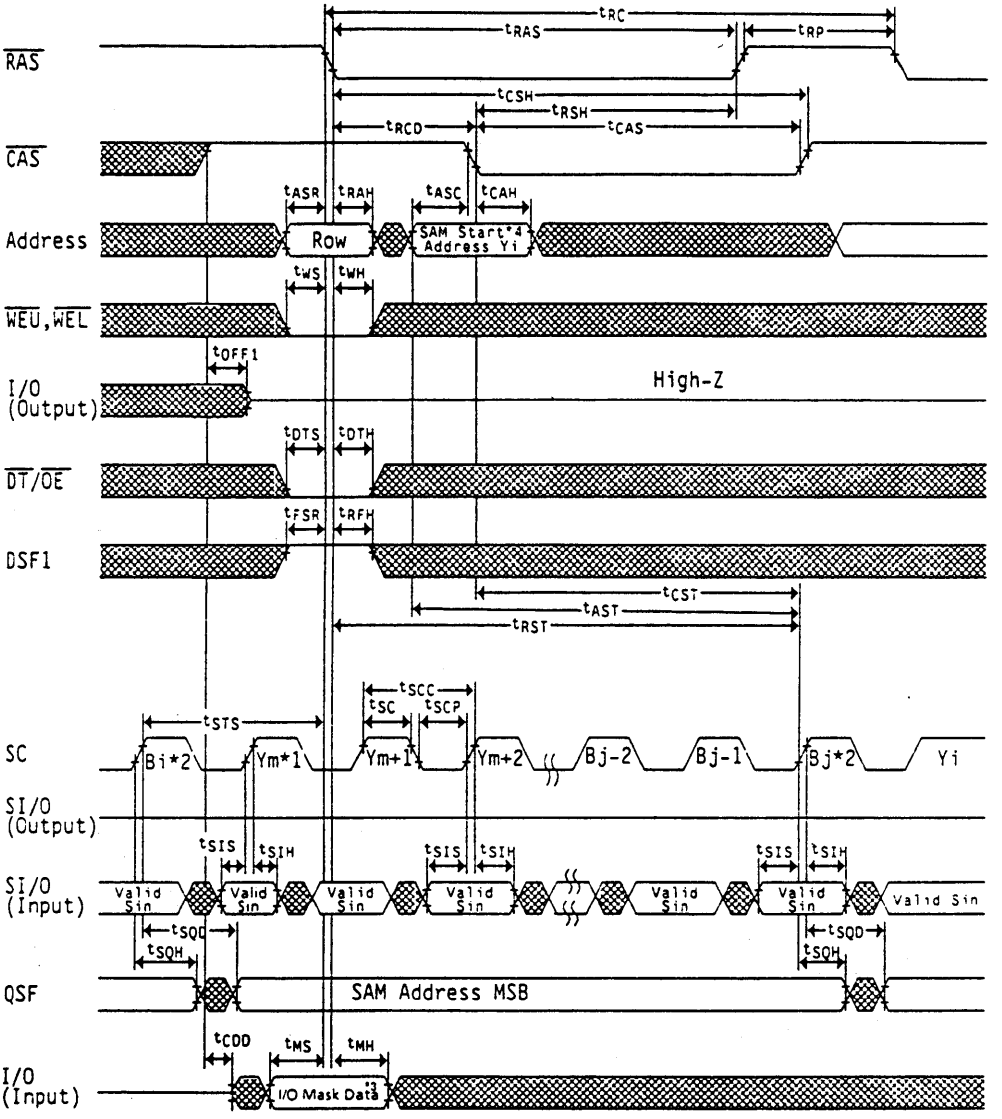
: Don't care

Split Read Transfer Cycle



Notes: 1. Ym is the SAM start address in before SRT.
2. Bi, Bj initiate the boundary address.
3. A8: Don't care
SAM start address can't set on the boundary address.

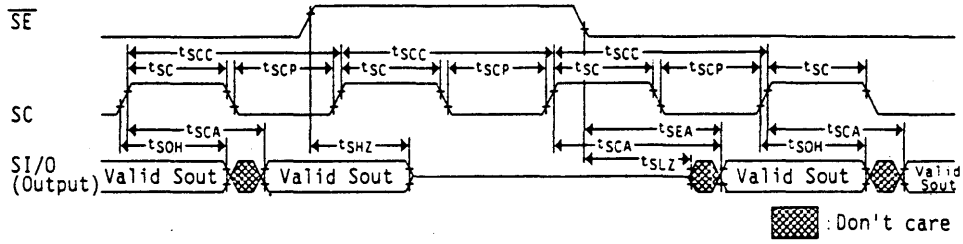
Masked Split Write Transfer Cycle



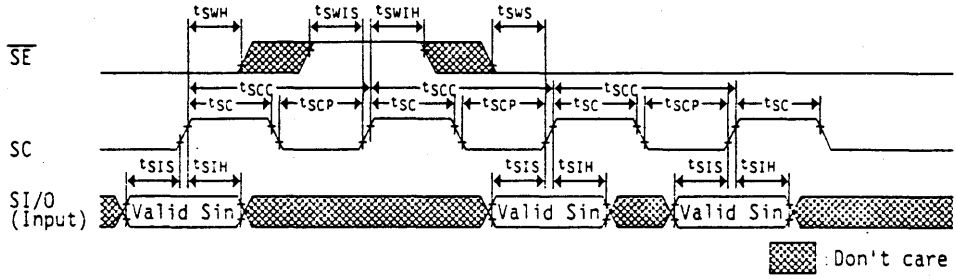
Notes: 1. Ym is the SAM start address in before MSWT.
2. Bi, Bj initiate the boundary address.
3. I/O Mask Data(In new mask mode)
Low: Mask
Hogh: Non Mask
I/O: Don't care in persistent mask mode
4. A8: Don't care
SAM start address can't set on the boundary address.

: Don't care

Serial Read Cycle

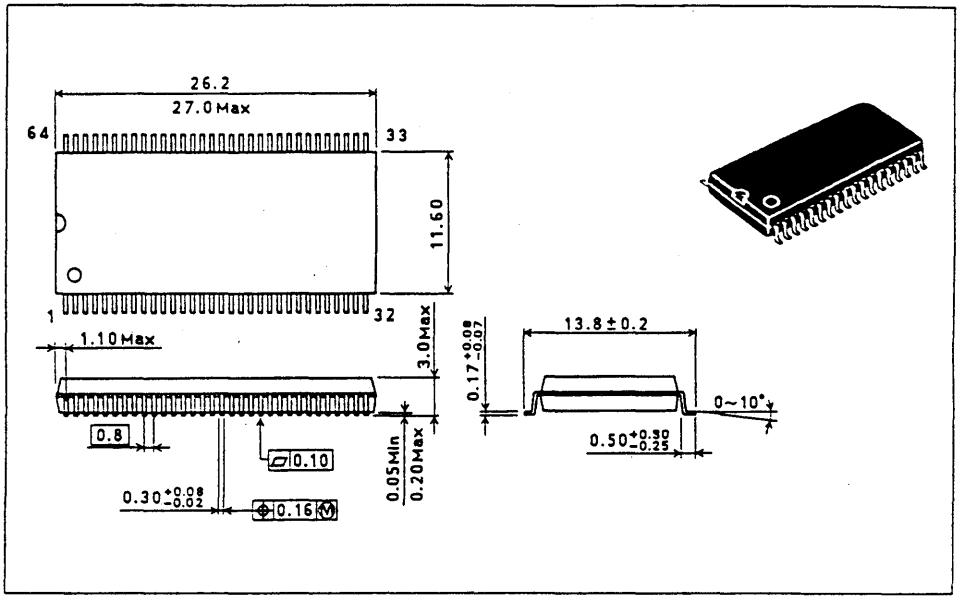


Sereal Write Cycle



Package Dimensions

HM5316123 Series (FP-64DS) Unit: mm



Section 3

Frame Memory

ADE-203-012C (Z)

HM530281
331,776-Word × 8-Bit Frame Memory

HITACHI

Rev. 3
Feb. 1994

The HM530281 memory products provide completely asynchronous I/O and operate at the high speed of 50 MHz. 0.8 µm CMOS process is used in their fabrication.

The HM530281 memory products provide reset, jump, and line increment/hold pointer control functions that can be used in synchronization with independent clocks on each of the I/O ports. Memory can be accessed immediately without any waiting period after the execution of these functions.

In addition to the FIFO function, the 281 products support an address structure that is compatible with HDTV, NTSC, and PAL standards, and can be used in a wide range of applications, such as noise reducers, TBC (time-based correction), inter-frame YC separation, and special function modes (e.g., multi-freeze, P-in-P) in the digital TV, VCR, and video camera application.

They are also appropriate for use as inter-system speed conversion buffer memories in communication systems, as cache memories of HDD and MOD and as frame buffer of VGA.

Features

(1) HM530281

- Organization: 331,776 words × 8 bits
- Completely asynchronous operation of the serial read port and write port
  - — Internal generation of read and write addresses
  - — Internal memory operation control provided on-chip
- High speed read/write cycle time: 50 MHz
- Reset functions
  - — Independent execution for read and write ports
  - — Can be executed with arbitrary timing
  - — Allow immediate access after execution (read/write) (for the jump function, when the address setup is complete)
  - — Jump address specifiable in 32-word units
- Built-in self-refresh eliminates the need for external refresh control.
- Power supply voltage: V_{CC} = 5.0 V ±10%
- 2 dimensial Address
- 32 word unit address jump
- Line increment/hold Address pointer control function
- Window scan function
- Can handle HDTV, NTSC, and PAL standards
  - — Line length: Up to 1152 bits (arbitrary line lengths can also be handled by using the line reset function.)
  - — Line count: Up to 324 lines

Hitachi semiconductor

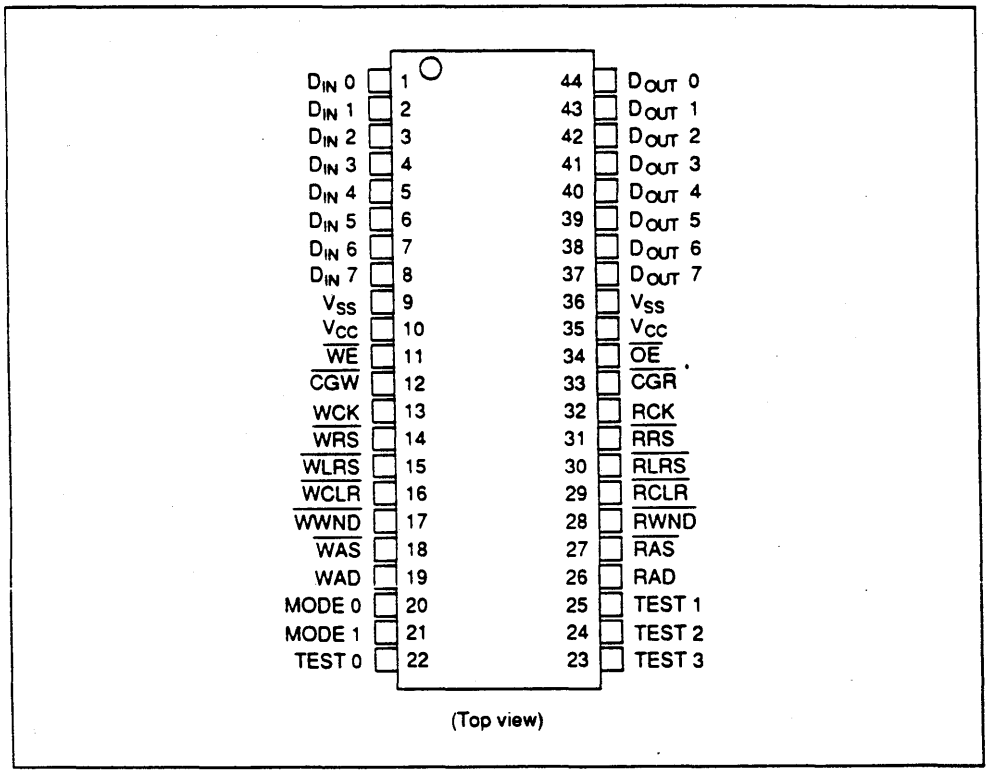
Ordering Information

Product Number	Cycle Time	Memory Organization	Package
HM530281 TT-20	20 ns	331,776 words x 8 bits*1	44-pin TSOP
-25	25 ns	1152 dots x 288 lines x 8 bits*2	
-34	34 ns	1024 dots x 324 lines x 8 bits	
-45	45 ns		

Selectable following two kinds of addressing mode by mode pins.

Notes: 1. 1 dimensional addressing mode
2. 2 dimensional addressing mode

Pin Arrangement

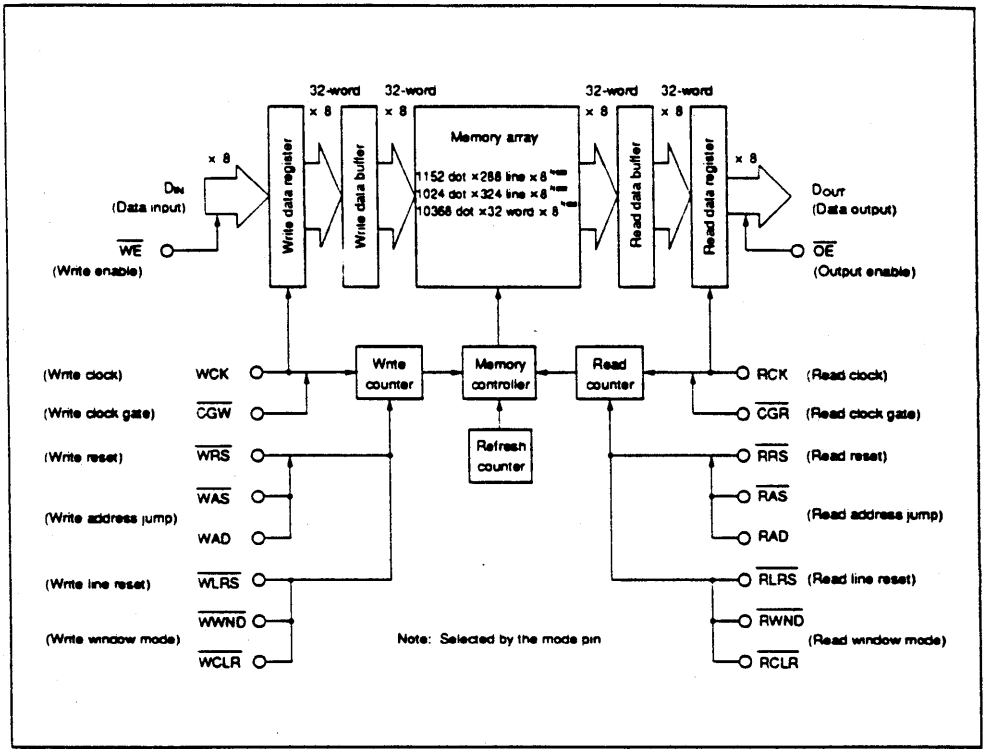


(Top view)

Pin Functions

Symbol	Pin Functions	
	2 Dim.add.	1 Dim.add.
$D_{IN}0$ to $D_{IN}7$	Data input	Data input
$D_{OUT}0$ to $D_{OUT}7$	Data output	Data output
WCK	Write clock	Write clock
RCK	Read clock	Read clock
$\overline{WRS}$	Write reset	Write reset
$\overline{RRS}$	Read reset	Read reset
$\overline{WE}$	Write enable	Write enable
$\overline{OE}$	Output enable	Output enable
$\overline{CGW}$	Write clock gate	Write clock gate
$\overline{CGR}$	Read clock gate	Read clock gate
$\overline{WAS}$	Write address set	Write address set
WAD	Write address	Write address
$\overline{RAS}$	Read address set	Read address set
$\overline{RAD}$	Read address	Read address
$\overline{WLRS}$	Write line reset	Vcc or GND
$\overline{RLRS}$	Read line reset	Vcc or GND
$\overline{WWND}$	Write window mode	Vcc or GND
$\overline{RWND}$	Read window mode	Vcc or GND
$\overline{WCLR}$	Write clear	Vcc or GND
$\overline{RCLR}$	Read clear	Vcc or GND
MODE 0 to 1	Mode selection input	Mode selection input
V_{CC}	Power supply	Power supply
V_{SS}	Ground	Ground
TEST0 to TEST3	Connect to ground	Connect to ground

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Pin voltage[Note]	V_T	−1.0 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	−55 to +125	°C
Storage temperature (when biased)	T_{bias}	−10 to +85	°C

Note: The permissible values with respect to V_{SS}.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Power supply voltage	V_{CC}	4.5	5	5.5	V
	V_{SS}	0	0	0	V
Input voltages	V_{IH}	2.7	—	6.5	V
	V_{IL}	−0.5[Note]	—	0.6	V

Note: When the pulse width is under 10 ns, V_{IL} min = −3.0 V.

DC Characteristics (V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

		HM530281-20			HM530281-25			HM530281-34			HM530281-45				Test
Item	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit	Conditions
Operating power supply voltage	I_{CCA}	—	110	135	—	90	120	—	70	95	—	55	75	mA	I_{OUT} = 0, t_{WCC} = t_{RCC} = Min
Standby power supply voltage	I_{CCS}	—	15	25	—	15	25	—	15	25	—	15	25	mA	
Input leakage current	I_{LI}	−10	—	10	−10	—	10	−10	—	10	−10	—	10	mA	V_{CC} = 5.5 V, V_{IN} = V_{SS} to V_{CC}
Output leakage current	I_{LO}	−10	—	10	−10	—	10	−10	—	10	−10	—	10	mA	$\overline{OE}$ = V_{IN} V_{OUT} = V_{SS} to V_{CC}
Output voltages	V_{OL}	—	—	0.4	—	—	0.4	—	—	0.4	—	—	0.4	V	I_{OL} = 2.1 mA
	V_{OH}	2.4	—	—	2.4	—	—	2.4	—	—	2.4	—	—	V	I_{OH} = −1.0 mA

Capacitances

Item	Symbol	Typ	Max	Units	Test Conditions
Input capacitance	C_{IN}	—	5	pF	V_{IN} = 0 V
Output capacitance	C_{OUT}	—	7	pF	V_{OUT} = 0 V

Note: These parameters are sampled values, not values measured for all units.

AC Characteristics

Test Conditions

Input pulse level: V_{SS} to 3.0 V
Input rise/fall times: 3 ns
I/O timing reference level: 1.5 V
Output load: 1 TTL + 50 pF (including jig and scope capacitances)

		HM530281-20		HM530281-25		HM530281-34		HM530281-45		
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Write clock cycle time	t_{WCC}	20	—	25	—	34	—	45	—	ns
Write clock pulse width (high)	t_{WC}	8	—	10	—	12	—	15	—	ns
Write clock pulse width (low)	t_{WCP}	8	—	10	—	12	—	15	—	ns
$\overline{WRS}$ setup time	t_{WRS}	8	—	8	—	10	—	10	—	ns
$\overline{WRS}$ hold time	t_{WRH}	7	—	8	—	10	—	10	—	ns
Data input setup time	t_{DS}	5	—	5	—	5	—	5	—	ns
Data input hold time	t_{DH}	6	—	6	—	6	—	6	—	ns
$\overline{CGW}$ setup time	t_{WGS}	7	—	8	—	10	—	10	—	ns
$\overline{CGW}$ hold time	t_{WGH}	7	—	8	—	10	—	15	—	ns
$\overline{WE}$ setup time	t_{WES}	5	—	5	—	5	—	5	—	ns
$\overline{WE}$ hold time	t_{WEH}	6	—	6	—	6	—	6	—	ns
Read clock cycle time	t_{RCC}	20	—	25	—	34	—	45	—	ns
Read clock pulse width (high)	t_{RC}	8	—	10	—	12	—	15	—	ns
Read clock pulse width (low)	t_{RCP}	8	—	10	—	12	—	15	—	ns
$\overline{RRS}$ setup time	t_{RRS}	7	—	8	—	10	—	10	—	ns
$\overline{RRS}$ hold time	t_{RRH}	7	—	8	—	10	—	10	—	ns
Access time from RCK	t_{RAC}	—	18	—	23	—	25	—	35	ns
Output hold time	t_{OH}	6	—	6	—	6	—	6	—	ns

AC Characteristics (cont)

		HM530281-20		HM530281-25		HM530281-34		HM530281-45		
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Output enable time	t_{OLZ}	0	—	0	—	0	—	0	—	ns
Output enable access time	t_{OAC}	—	18	—	20	—	25	—	25	ns
Output disable time	t_{OHZ}	0	15	0	18	0	20	0	20	ns
$\overline{CGR}$ setup time	t_{RGS}	7	—	8	—	10	—	10	—	ns
$\overline{CGR}$ hold time	t_{RGH}	7	—	8	—	10	—	10	—	ns
$\overline{WAS}$ setup time	t_{WSS}	7	—	8	—	10	—	10	—	ns
$\overline{WAS}$ hold time	t_{WSH}	7	—	8	—	10	—	10	—	ns
$\overline{RAS}$ setup time	t_{RSS}	7	—	8	—	10	—	10	—	ns
$\overline{RAS}$ hold time	t_{RSH}	7	—	8	—	10	—	10	—	ns
Write address input setup time	t_{WAS}	5	—	5	—	5	—	5	—	ns
Write address input hold time	t_{WAH}	6	—	6	—	6	—	6	—	ns
Read address input setup time	t_{RAS}	5	—	5	—	5	—	5	—	ns
Read address input hold time	t_{RAH}	6	—	6	—	6	—	6	—	ns
$\overline{WLRS}$ setup time	t_{WLS}	7	—	8	—	10	—	10	—	ns
$\overline{WLRS}$ hold time	t_{WLH}	7	—	8	—	10	—	10	—	ns
$\overline{RLRS}$ setup time	t_{RLS}	7	—	8	—	10	—	10	—	ns
$\overline{RLRS}$ hold time	t_{RLH}	7	—	8	—	10	—	10	—	ns
$\overline{WCLR}$ setup time	t_{WCLS}	7	—	8	—	10	—	10	—	ns
$\overline{WCLR}$ hold time	t_{WCLH}	7	—	8	—	10	—	10	—	ns
$\overline{RCLR}$ setup time	t_{RCLS}	7	—	8	—	10	—	10	—	ns
$\overline{RCLR}$ hold time	t_{RCLH}	7	—	8	—	10	—	10	—	ns
$\overline{WWND}$ setup time	t_{WWDS}	7	—	8	—	10	—	10	—	ns
$\overline{WWND}$ hold time	t_{WWDH}	7	—	8	—	10	—	10	—	ns
$\overline{RWND}$ setup time	t_{RWDS}	7	—	8	—	10	—	10	—	ns
$\overline{RWND}$ hold time	t_{RWDH}	7	—	8	—	10	—	10	—	ns

Input and Output Pin Functions

$D_{IN}0$ to $D_{IN}7$ (data input) Input

The D_{IN} pins input 8 bits of data. Data is input on the rising edge of the cycle of WCK that follows a low level on both $\overline{CGW}$ and $\overline{WE}$.

$D_{OUT}0$ to $D_{OUT}7$ (data output) Output

The D_{OUT} pins output 8 bits of data. Data output is synchronized with the RCK clock, and the access time is specified from the rising edge of the RCK cycle.

WCK (write clock) Input

WCK is the write clock input pin. The input of write data is synchronized with this clock.

Write data is input on the rising edge of the cycle of WCK that follows a low level on both $\overline{CGW}$ and $\overline{WE}$, and when $\overline{CGW}$ is low, the internal write address pointer is incremented at the same time.

Input of the write jump address is also synchronized with this clock. The 14 or 15 bits of the write jump address are read in sequentially from the WCK cycle that set $\overline{WAS}$ low, irrespective of write data acquisition.

RCK (read clock) Input

RCK is the read clock input pin. Read data is output in synchronization with this clock when both $\overline{CGR}$ and $\overline{OE}$ are low, and when $\overline{CGR}$ is low, the internal read address pointer is incremented at the same time.

Input of the read jump address is also synchronized with this clock. The read jump address is read in sequentially starting at the RCK cycle in which $\overline{RAS}$ was set low, independently of read data output.

$\overline{WRS}$ (write address pointer reset) Input

$\overline{WRS}$ is a reset signal input that resets the write address pointer to 0 when $\overline{WAS}$ and $\overline{WLRS}$ are high, resets to the head of the line currently being written when $\overline{WAS}$ is high and $\overline{WLRS}$ is low, and jumps to the preset write jump address when $\overline{WAS}$ is low.[Note]

Only the falling edge of this reset input is detected, and, on the first WCK cycle following that falling edge, a write cycle to the set address is started immediately.

Note: The reset destination in window scan mode changes as follows:

Reset to 0 → Reset to the window start.
Reset to line start → Reset to the point at the left edge of the window for the line.

$\overline{RRS}$ (read address pointer reset) Input

$\overline{RRS}$ is a reset signal input that resets the read address pointer to 0 when $\overline{RAS}$ and $\overline{RLRS}$ are high, resets to the start of the line currently being read when $\overline{RAS}$ is high and $\overline{RLRS}$ is low, and jumps to the read jump address when $\overline{RAS}$ is low.[Note]

Only the falling edge of this reset input is detected, and, on the first RCK cycle following that falling edge, a read cycle at the set address is started immediately.

Note: The reset destination in window scan mode changes as follows:

Reset to 0 → Reset to the window start.
Reset to line start → Reset to the point at the left edge of the window for the line.

$\overline{WE}$ (write enable) Input

$\overline{WE}$ is an input signal that controls the enabling/disabling of the data input pins. When $\overline{WE}$ is low, input data is acquired on the WCK cycle, and when $\overline{WE}$ is high, data input is disabled and the previous memory data is maintained.

Note that the write address pointer is incremented by the WCK write clock without regard for the level of $\overline{WE}$.

$\overline{OE}$ (output enable) Input

$\overline{OE}$ is an input signal that enables/disables the data output pins. When $\overline{OE}$ is low, data output is enabled, and when high, data output is disabled and the output pins go to the high impedance state.

Note that the read address pointer is incremented by the RCK read clock without regard for the level of $\overline{OE}$. Therefore, data can be jumped over during read simply by disabling output with $\overline{OE}$.

$\overline{CGW}$(clock gate for write) Input

$\overline{CGW}$ is an input signal that enables/disables incrementing of the internal write address pointer. When $\overline{CGW}$ is low, the write address pointer is incremented in synchronization with the WCK write clock, and when high, incrementing is stopped. Therefore time axis compression can be easily implemented without stopping the write clock by using $\overline{CGW}$.

$\overline{CGR}$(clock gate for read) Input

$\overline{CGR}$ is an input signal that enables/disables incrementing of the internal read address pointer. When $\overline{CGR}$ is low, the read address pointer is incremented in synchronization with the RCK read clock, and when high, incrementing is stopped. Therefore time axis expansion can be easily implemented without stopping the read clock by using $\overline{CGR}$.

$\overline{WAS}$ (write address set and jump) Input

$\overline{WAS}$ is an input signal that initiates write jump address input when $\overline{WRS}$ is high and jumps to the previously input write jump address when $\overline{WRS}$ is low. The falling edge of this input signal is detected, and either a write jump address input is initiated or a jump to the previously input write jump address is executed on the first WCK cycle following the fall of $\overline{WAS}$.

WAD (write jump address) Input

WAD is the input pin for the write jump address. The 14/15 bits of the write jump address are read in sequentially from the high order bit, starting at the WCK cycle (when $\overline{WRS}$ was high) in which $\overline{WAS}$ was set low.Note

$\overline{RAS}$ (read address set and jump) Input

$\overline{RAS}$ is an input signal that initiates read jump address input when $\overline{RRS}$ is high and jumps to the previously input read jump address when $\overline{RRS}$ is low. The falling edge of this input signal is detected, and either the read jump address input is initiated or the jump to the previously input read jump address is executed on the first RCK cycle following the fall of $\overline{RAS}$.

RAD (read jump address) Input

RAD is the input pin for the read jump address. The 14/15 bits of the write jump address are read in sequentially from the high order bit, starting at the RCK cycle (when $\overline{RRS}$ was high) in which $\overline{RAS}$ was set low.Note

Note:

Addressing Mode	Address Structure	Input Address
1 dim. add. (FIFO)	0 to 10,367 blocks	Address bits A_{13} to A_0
2 dim.add. (1)	32 horizontal blocks by 324 vertical lines	Line address bits V_8 to V_0, horizontal address bits H_4 to H_0
2 dim.add. (2)	36 horizontal blocks by 288 vertical lines	Line address bits V_8 to V_0, horizontal address bits H_5 to H_0

Note: For 2 dim. add., read jump and read window starting point setup are available only for the read jump address of which horizontal address is "0".

$\overline{WLRS}$ (write line reset) Input (in 2 dimensional addressing mode)

$\overline{WLRS}$ is an input pin for resetting the write address pointer to the start of the line from an arbitrary dot for each line.Note Only the falling edge of this signal is detected, and, on the first WCK cycle following that falling edge, the write address pointer is set to the head of the next line when $\overline{WRS}$ is high, and to head of the current line when $\overline{WRS}$ is low.Note

Note: When window scan mode is set, the reset is to the point at the left edge of the window for the line.

$\overline{\text{RLRS}}$ (read line reset) Input (in 2 dimensional addressing mode)

$\overline{\text{RLRS}}$ is an input pin for resetting the read address pointer to the start of the line from an arbitrary dot for each line.Note Only the falling edge of this signal is detected, and, on the first $\overline{\text{RCK}}$ cycle following that falling edge, the write address pointer is set to the head of the next line when $\overline{\text{RRS}}$ is high, and to head of the current line when $\overline{\text{RRS}}$ is low.Note

Note: When window scan mode is set, the reset is to the point at the left edge of the window for the line.

$\overline{\text{WWND}}$ (write window scan) Input (in 2 dimensional addressing mode)

$\overline{\text{WWND}}$ is an input signal that specifies the use of the window scan function. When executing a write jump with $\overline{\text{WRS}}$ and $\overline{\text{WAS}}$ low, if $\overline{\text{WWND}}$ is set low at the same time, a scan of the window region that takes that write jump address as its starting point will begin (see note below).

$\overline{\text{RWND}}$ (read window scan) Input (in 2 dimensional addressing mode)

$\overline{\text{RWND}}$ is an input signal that specifies the use of the window scan function. When executing a read jump with $\overline{\text{RRS}}$ and $\overline{\text{RAS}}$ low, if $\overline{\text{RWND}}$ is set low at the same time, a scan of the window region that takes that read jump address as its starting point will begin.Note

Note: When window scan is set, the horizontal address of the pointer reset destination when increment/hold is executed will be the left edge of the window. Also, when a write/read reset is executed, the pointer will be reset to the starting point of the window. Thus it is possible to scan arbitrary window regions within the screen independently for read and write by using these line reset and reset functions.

Starting point of read window is confined to the address of which horizontal address is '0'.

$\overline{\text{WCLR}}$ (write clear) Input

$\overline{\text{WCLR}}$ is an input signal that, independently of the levels on $\overline{\text{WRS}}$, $\overline{\text{WAS}}$, $\overline{\text{WLRS}}$ and $\overline{\text{WWND}}$, resets the write address pointer to 0 and clears the window scan function. This function is executed immediately in the WCK cycle in which $\overline{\text{WCLR}}$ was set low. This clear operation should also be performed after applying power to the HM530281.

$\overline{\text{RCLR}}$ (read clear) Input

$\overline{\text{RCLR}}$ is an input signal that, independently of the levels on $\overline{\text{RRS}}$, $\overline{\text{RAS}}$, $\overline{\text{RLRS}}$ and $\overline{\text{RWND}}$, resets the read address pointer to 0 and clears the window scan function. This function is executed immediately in the RCK cycle in which $\overline{\text{RCLR}}$ was set low. This clear operation should also be performed after applying power to the HM530281.

Memory Structure

The memory is organized as 331,776 words of 8 bits each, and these words can be accessed sequentially, since the address pointer can be incremented by inputting a clock signal. Addresses are allocated corresponding to 32 word blocks.

The mode pins switch between the three addressing modes shown below.

Mode 0	Mode 1	Addressing Mode	Address Structure	Capacity
0	0	1 dim. add. (FIFO)	0 to 10,367 blocks	331,776 words
1	0	2 dim. add. (1)	32 horizontal blocks by 324 vertical lines	1024 dots by 324 lines
0	1	2 dim. add. (2)	36 horizontal blocks by 288 vertical lines	1152 dots by 288 lines

In 1 dimensional addressing mode, blocks 0 to 10367 are accessed cyclically.
In the 2 dimensional addressing modes, the line head can be reset at an arbitrary dot on each line.

Operations

Write

- Write operation
  When the $\overline{WE}$ and $\overline{CGW}$ inputs are low, 8 bits of write data are input in synchronization with the WCK clock. The input data is read in to the word indicated by the address pointer on the next rising edge of the WCK cycle. This allows read data and write data to be handled with the same clock, and cascade connections to be easily implemented.

- Write reset operations
  When $\overline{CGR}$ is 'L', by setting $\overline{WRS}$ low, the write address pointer can be set immediately on that WCK cycle to the address 0 block head.

  This operation can be executed independently of the input level of $\overline{WE}$. (See 'Notes on usage 6' on the operation when $\overline{CGW}$ = 'H')

- Write address pointer increment operations
  The write address pointer is incremented in synchronization with WCK when $\overline{CGW}$ is low.

  It is possible to apply a write mask in WCK clock units by setting the $\overline{WE}$ input high. In this case, the previous memory data will be retained. The write address pointer increment function can be stopped by setting the $\overline{CGW}$ input high. This allows time axis compression to be implemented easily. (See 'Notes on usage 3 and 4' for interval specifications of write system reset operations)Note

Note: The write system reset operation stands for write reset, write window reset, write line reset, write jump and write clear.

Read

- Read operation
  8 bits of read data are output in synchronization with the RCK clock when the $\overline{OE}$ and $\overline{CGR}$ inputs are low. The access time is stipulated from the rising edge of the RCK clock.

- Read reset operations
  When $\overline{CGR}$ is 'L', by setting $\overline{RRS}$ low, the read address pointer can be set immediately on that RCK cycle to address 0 and data will then be output.

  This operation can be performed independently of the input level of $\overline{OE}$. (See 'Notes on usage 5' on the operation when $\overline{CGR}$ = 'H')

- Read address pointer increment operations
  The read address pointer is incremented in synchronization with RCK when $\overline{CGR}$ is low.

  Data outputs go to the high impedance state when the $\overline{OE}$ input is set high. The read address pointer increment function can be stopped by setting the $\overline{CGR}$ input high. This allows time axis expansion to be implemented easily. (See 'Notes on usage 2' for interval specifications of read system reset operations)Note

Note: The read system reset operation stands for read reset, read jump, read window reset, read line reset and read clear.

$\overline{WE}$ and $\overline{CGW}$ Input Level, Write Address Pointer, and Data Input State Relationship

WCK Rising Edge		Internal Write	
$\overline{CGW}$	$\overline{WE}$	Address Pointer	Data Input
L	L	Incremented	Enable
L	H	Stopped	Disable (memory data is retained)
H	—		

Data is input when the $\overline{WE}$ input is low.

Relation Between the $\overline{OE}$ and $\overline{CGR}$ Input Levels and the Read Address Pointer and Data Output States.

RCK Rising Edge		Internal Read	
$\overline{CGR}$	$\overline{OE}$	Address Pointer	Data Output
L	L	Incremented	Output
L	H		High impedance
H	L	Stopped	Output data held
H	H		High impedance

Data is output when the $\overline{OE}$ input is low.

Line Reset (independent functions for read and write, in 2 dimensional addressing modes)

When the 281 series products are used in 2 dimensional addressing modes, the line length can be set to be either 1024 dots (2 dimensional (1)) or 1152 dots (2 dimensional (2)). In these modes, after accessing the data at the last dot (address) on each line, address pointer incrementing is stopped. Access is restarted at either the first dot at the head of the next line or at the first dot at the head of the current line by executing either a line increment or a line hold, respectively. Also, since these line reset operations can be executed at any arbitrary point in the middle of a line, an arbitrary line length (of between 64 dots and the actual line length) can be realized.

- Line increment operation
  In case clock gate signal ($\overline{CGW}$, $\overline{CGR}$) is 'L', the read and write line increment operations are executed by setting $\overline{RLRS}$ low and $\overline{RRS}$ high, and setting $\overline{WLRS}$ low and $\overline{WRS}$ high respectively. When these operations are executed, the next access goes immediately to the starting dot of the next line.

- Line hold operation
  In case clock gate signal ($\overline{CGW}$, $\overline{CGR}$) is 'L', the read and write line hold operations are executed by setting $\overline{RLRS}$ and $\overline{RRS}$ low, and setting $\overline{WLRS}$ and $\overline{WRS}$ low respectively. When these operations are executed, the next access goes immediately to the starting dot of the current line. Note that the read line hold operation is invalid on the first line following a 0 reset or jump. In this case, the same effect can be achieved by re-executing the reset or jump operation (resetting only the H address to 0).

  If the reset interval specifications are met (see Notes on Usage 1 to 3), the line reset[Note] operation can be performed on an arbitrary RCK/WCK clock cycle without regard for the levels of the $\overline{OE}$, $\overline{WE}$, and inputs. (See Notes on usage 6, 7 for the operation when clock gate signal ($\overline{CGW}$, $\overline{CGR}$) is 'H'.)

Note: The line reset operation stands for write line hold, write line increment, read line hold and read line increment.

Jump (independent functions for read and write)

It is possible to set the address pointer to the start address of an arbitrary block in 32 word units.[Note] After initializing a jump address setup for read and/or write, after 64 WCK or 64 RCK cycles, it is possible to execute a jump to that address (random access in 32 word by 8 bit units) independently for read and write.

Note: As for the read jump, in 2-dim add, read jump address is confined to the address of which horizontal address is '0'.

- Jump to the line end block is inhibited. (See 'Notes on usage 5' for jump operation to '0' address)

- Jump address setup
  The read and write jump addresses are serially input independently from the RAD and WAD pins in synchronization with the RCK and WCK clock inputs respectively. Address input start is enabled by setting the $\overline{RAS}$ and/or $\overline{WAS}$ inputs low for read and write respectively, and 14/15 bits of jump address are input sequentially starting with that cycle.[Note] Note that the read and write operations can continue independently of this address input operation.

- Jump address setup is executed regardless of the input level of $\overline{WE}$, $\overline{CGW}$ and $\overline{OE}$, $\overline{CGR}$.

Note:

Addressing Mode	Address Structure	Input Address
1 dim. add. (FIFO)	0 to 10,367 blocks	Address bit A_{13} to A_0
2 dim. add (1)	32 horizontal blocks by 324 vertical lines	Line address bits V_8 to V_0, horizontal address bits H_4 to H_0
2 dim. add. (2)	36 horizontal blocks by 288 vertical lines	Line address bits V_8 to V_0, horizontal address bits H_5 to H_0

Following the start of address input, it is possible to mask the input of address bits below an arbitrary bit position by returning $\overline{RAS}$ or $\overline{WAS}$ to the high level at the desired bit position. This can be convenient in applications that need to jump a fixed interval, since the low order bits of the address will be fixed. When all 14 bits of an address are to be input, be sure to hold $\overline{RAS}$ and $\overline{WAS}$ low for the full 14-clock period.

- Jump operation
  In case clock gate signal is 'L', the jump operation is executed by setting $\overline{RRS}$ and $\overline{RAS}$ low for read, and by setting $\overline{WRS}$ and $\overline{WAS}$ low for write, and the address set is accessed immediately from that RCK or WCK cycle. Note that as long as the interval specifications listed in Notes on Usage 1 to 4 are met, the jump operation can be executed on any RCK or WCK cycle without regard for the values of $\overline{OE}$ on read, and $\overline{WE}$ on write. (See 'Notes on usage 5 and 6' on the operation when clock gate signal ($\overline{CGW}$, $\overline{CGR}$) is 'L')

Window Scan (independent functions for read and write)

The window scan function can be used with either the 2 dimensional (1) or (2) addressing modes, and is a function which scans a rectangular region with an arbitrary starting point[Note]. The jump address setup function (see Jump address setup above) is used to specify the starting point

Note: Starting point of read window is confined to the address of which horizontal address is '0'.

- Initiating window scan
  When clock gate signal is 'L', the window scan function is started by setting $\overline{WWIND}$ to low for write or $\overline{RWIND}$ low for read, and executing a read or write jump operation (see Jump operation above). Window scan will start immediately from that cycle.

- Window scan operation
  When clock gate signal is 'L', one of the window scan functions described below will be executed independently for read and write.[Note]

  Also note that as long as the interval conditions listed in Notes on Usage 1 to 3 are met, these operations can be executed at arbitrary dots without regard for the address block organization.

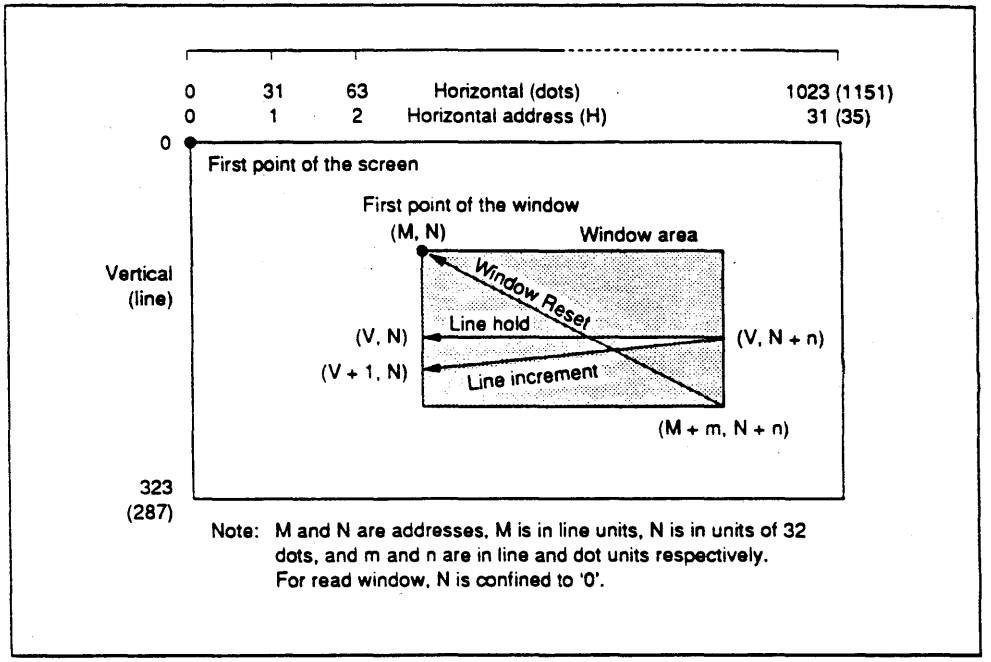
Operation	Address Pointer Control
Reset	Reset to the first dot at the start of the window.
Line increment	Reset to the first dot at the left edge of the window on the next line.
Line hold	Reset to the first dot at the left edge of the window on the current line.

Note: For a starting point, minimum window size can be scanned, is 64 dots × 1 line.

- Clearing window scan
  The window scan function is turned off either by executing a reset or jump with $\overline{RWIND}$ (for read) or $\overline{WWIND}$ (for write) set high, or by executing the clear operation described in section Clear below.

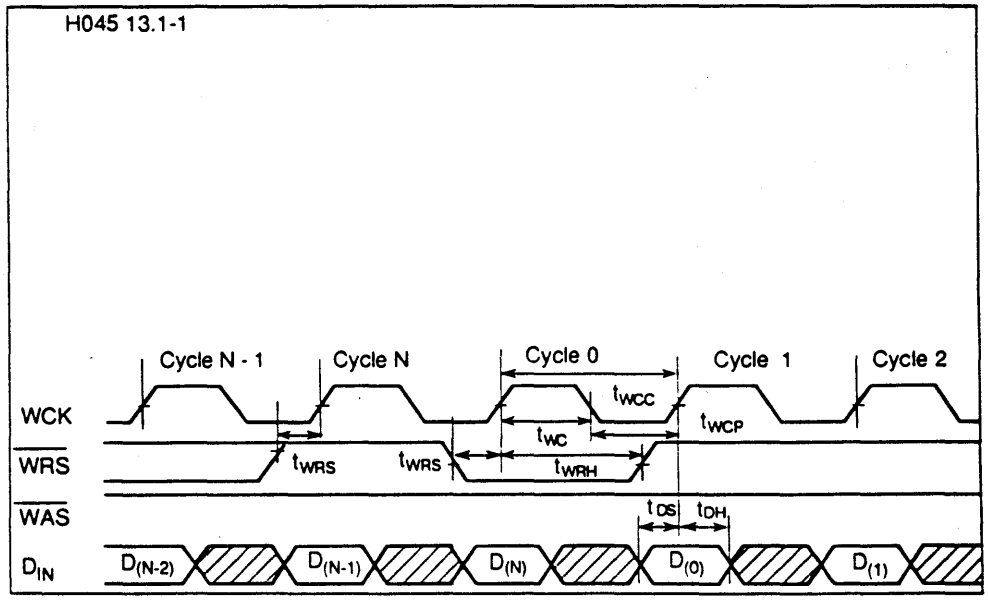
- Both setting and clearing window scan mode are executed independently of $\overline{OE}$ and $\overline{WE}$. (See 'Notes on usage 1 and 2' for the operation when clock gate signal ($\overline{CGW}$, $\overline{CGR}$) is 'H')

- Overview of the window scan operation



Note: M and N are addresses, M is in line units, N is in units of 32 dots, and m and n are in line and dot units respectively. For read window, N is confined to '0'.

- Starting and clearing window scan



Clear (independent functions for read and write)

The clear function both resets the address pointer to 0 without regard for the value on $\overline{WRS}$, $\overline{WAS}$, $\overline{WLRS}$, $\overline{WWND}$, $\overline{RRS}$, $\overline{RAS}$, $\overline{RLRS}$ and $\overline{RWND}$. If window mode is set, this clears window mode.

- Clear Operation

  When clock gate signal ($\overline{CGW}$ or $\overline{CGR}$) is 'L', the clear operation can be executed by setting the $\overline{RCLR}$ pin low for read (read clear) and the $\overline{WCLR}$ pin low for write (write clear). The data input following a write clear is valid data. If the interval conditions listed in Notes on Usage 1 to 3 are met by the operations including the clear operation, then the data preceding the clear operation will also be valid data.

Access of New and Previous Data

- New data access (follow-up read out of data currently being written)
  Written data of 32 word block can be read out 128 WCK cycles after it was written. However, it is necessary to execute the read jump address setup operation outside the time period between 32 WCK cycles before write to that address is started and 32 WCK cycles after write to that address is completed.

  — It is also possible to read out the new data of 32 word block when jumping to an address at least 128 WCK clock cycles after write to that address was finished. Note that in this case, there is more than enough time for the read jump address setup operation even if it is begun 32 or more clock cycles after the completion of the write operation.

  — It is possible to read out the new data of less than 32 word block when 128 WCK clock after write system reset was input.

At least 96 WCK clock are necessory between completion 32 word block data input and starting previous address of 32 word block data output. Generary this mean, 160 WCK clock separation between write and read Address pointer.

- Previous data access (reading out data prior to that of the current write operation)
  The previous data can be read out up to 32 WCK clock cycles after the write operation.

  Therefore, these memories can be used to provide delay times of between 160 and 331,808 (331,776 + 32) clock cycles.

Power On

Wait at least 100 µs after power-on to begin operation. At this time the write and read address pointers are undefined.

The following operation should be executed.

- $\overline{CGW}$ and $\overline{CGR}$ should be hold low.
- Reset cycle when 1 dimensional addressing mode.
- Clear cycle when 2 dimensional addressing mode.
- Dummy cycle of over 64 WCK and 64 RCK clock cycle.

Then, initiate the desired operating mode by providing the signal input combination given by the truth tables below.

Function Table[Note]

1 Dimensional Addressing Modes

- Write

WCK Rising Edge

$\overline{WRS}$	$\overline{WAS}$	Operation	
H	H	Normal state	In the normal state, the write address pointer is incremented in synchronization with WCK.
L	H	Reset	The write address pointer is reset to 0.
L	L	Jump	Jump to the address A to which the write address pointer is set.
H	L	Address setup	The write jump address is input.

- Read

RCK Rising Edge

$\overline{RRS}$	$\overline{RAS}$	Operation	
H	H	Normal state	In the normal state, the read address pointer is incremented in synchronization with RCK.
L	H	Reset	The read address pointer is reset to 0.
L	L	Jump	Jump to the address A to which the read address pointer is set.
H	L	Address setup	The read jump address is input.

Note: Description of operations of function table is based on the operation on condition $\overline{CGW}$, $\overline{WE}$ and $\overline{CGR}$, $\overline{OE}$ is 'L'.

2 Dimensional Addressing Modes (when window scan is not used)

- Write*1

Levels at the Rise of WCK						Operation		
$\overline{WRS}$	$\overline{WAS}$	$\overline{WLRS}$	$\overline{WWND}$	$\overline{WCLR}$		Write Address Pointer Control	Write Jump Address	Notes
H	H	H	H	H	Normal state	Incremented in synchronization with WCK	—	*2
L	H	H	H	H	Reset	Reset to (0, 0)	—	
L	L	H	H	H	Jump	Jump to the set address A	—	
H	L	H	H	H	Address set	—	Set	
H	H	L	H	H	Line increment	Reset to the first bit of the next line	—	*2
L	H	L	H	H	Line hold	Reset to the first bit of the current line	—	*2
—	—	—	—	L	Clear	Reset to (0, 0)	—	

(—: Don't care)

Notes: 1. Hold the $\overline{WWND}$ pin high when window mode is not used.
2. The write address pointer is incremented up to the last dot on the current line, and then stopped. Writing is started immediately from the first dot on the next line by execution of the line increment operation. Also, writing is started immediately from the first dot on the current line by execution of the line hold operation.

- Read*1

Levels at the Rise of RCK						Operation		
$\overline{RRS}$	$\overline{RAS}$	$\overline{RLRS}$	$\overline{RWND}$	$\overline{RCLR}$		Read Address Pointer Control	Read Jump Address	Notes
H	H	H	H	H	Normal state	Incremented in synchronization with RCK	—	*2
L	H	H	H	H	Reset	Reset to (0, 0)		
L	L	H	H	H	Jump	Jump to the set address A	—	
H	L	H	H	H	Address set	—	Set	
H	H	L	H	H	Line increment	Reset to the first bit of the next line	—	*2
L	H	L	H	H	Line hold	Reset to the first bit of the current line	—	*2
—	—	—	—	L	Clear	Reset to (0, 0)	—	

(—: Don't care)

Notes: 1. Hold the $\overline{RWND}$ pin high when window mode is not used.
2. The read address pointer is incremented up to the last dot on the current line, and then stopped. Reading is started immediately from the first dot on the next line by execution of the line increment operation. Also, reading is started immediately from the first dot on the current line by execution of the line hold operation.

2 Dimensional Addressing Modes (when window scan is used)

- Write

Levels at the Rise of WCK					Operation				
						Write Address Pointer Control				
WRS	WAS	WLRS	WWND	WCLR		Window Mode Off	Window Mode On	Write Jump Address	Window Mode after Execution	Notes
L	H	H	H	H	Reset	Reset to (0, 0)		—	Off	
H	H	H	—	H	Normal state	Incremented in synchronization with WCK		—	—	*1
H	H	L	—	H	Line increment	To the first bit of the next line	To the left edge of the window on the next line	—	—	
L	H	L	—	H	Line hold	To the first bit of the current line	To the left edge of the window on the current line	—	—	
H	L	H	—	H	Address set	—		Set	—	
L	L	H	H	H	Jump	Jump to the set address A		—	Off	
L	L	H	L	H	Window jump	Jump to the set address A		—	On	*2
L	H	H	L	H	Window Reset	Reset to the window origin point A		—	—	
—	—	—	—	L	Clear	Reset to (0, 0)		—	Off	

(—: Don't care)

Notes: 1. The write address pointer is incremented up to the last address on the line, and then stopped. Writing is started immediately from the first dot on the next line or the left edge of the window by execution of the line increment operation.

2. It is possible to move directly from an old window to a new window in window mode by setting up a new jump address and executing a window setup jump operation.
However, the new jump address should be input after access to the last line of the old window.

- Read

Levels at the Rise of RCK					Operation	Read Address Pointer Control		Read Jump Address	Window Mode after Execution	Notes
$\overline{RRS}$	$\overline{RAS}$	$\overline{RLRS}$	$\overline{RWND}$	$\overline{RCLR}$		Window Mode Off	Window Mode On			
L	H	H	H	H	Reset	Reset to (0, 0)		—	Off	
H	H	H	—	H	Normal state	Incremented in synchronization with RCK		—	—	*1
H	H	L	—	H	Line increment	To the first bit of the next line	To the left edge of the window on the next line	—	—	
L	H	L	—	H	Line hold	To the first bit of the current line	To the left edge of the window on the current line	—	—	
H	L	H	—	H	Address set	—		Set	—	
L	L	H	H	H	Jump	Jump to the set address A		—	Off	
L	L	H	L	H	Window jump	Jump to the set address A		—	On	*2
L	H	H	L	H	Window Reset	Reset to the window origin point A		—	—	
—	—	—	—	L	Clear	Reset to (0, 0)		—	Off	

(—:Don't care)

Notes: 1. The read address pointer is incremented up to the last address on the line, and then stopped. Reading is started immediately from the first dot on the next line or the left edge of the window by execution of the line increment operation.
2. It is possible to move directly from an old window to a new window in window mode by setting up a new jump address and executing a window setup jump operation.
However, the new jump address should be input after access to the last line of the old window.
3. When window scan mode is used any case after power on, $\overline{WWND}$ and $\overline{WRS}$ or $\overline{RWND}$ and $\overline{RRS}$ pins are should be input same signal.

Notes on Usage

1. Read system resets (read reset, read jump, read window reset, read line reset and read clear) and the read address setup operation cannot be executed for consecutive RCK clock cycles. Similarly, write system resets (write reset, write jump, write window reset, write line reset and write clear) and the write jump address setup operation cannot be execution for consecutive WCK clock cycles.
2. Read system reset operations and read jump address set operations must be performed at times separated by at least 64 RCK clock cycles. (There is no need to use only 32 word addressing units, and these operations can be performed on any clock cycle.)
3. Write system reset operations must be performed at times separated by at least 64 WCK clock cycles. During setting write jump address, write system reset operations cannot be executed.

4. It is possible to input the write system reset in the middle of 32 word unit addressing. In this case, not only must the condition of note 2 be met, but furthermore, pairs of write system resets for units of less than 32 words must be separated by at least 160 WCK clock cycles. When the write system reset is executed at less than 32 words, the data up to the point to which the address pointer has advanced will be written, and the remaining data will retain the old values. (Note that after the completion of a write of less than 32 words, a write reset is required to write the data for the last address into the memory array.)
5. Location 0 and line end cannot be specified as a jump address. Use a reset to access location 0.
6. Any number of read system resets can be input when $\overline{CGR}$ is high, but the only first reset is effective. This read system reset operation is executed at the rising edge of the RCK just after $\overline{CGR}$ is set to low.
7. When $\overline{CGW}$ is high, write system can reset be input only once. In this case, this write system reset is executed at the rising edge of the WCK just after $\overline{CGW}$ is set to low.

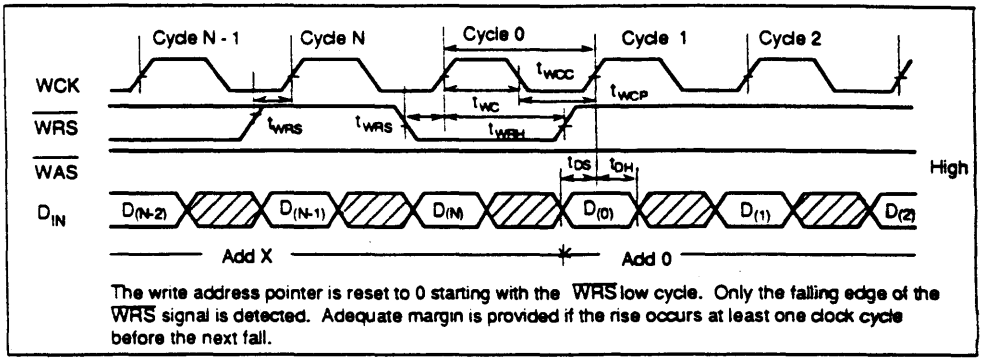
Supplement

If the read system reset interval (at least 64 RCK clock cycles) of note 1, or the write system reset interval for less than 32 word units (and at least 160 WCK clock cycles) are not provided (see note 3), it is possible for the 32 words of data of the first address after the reset to be invalid, or for the first write of less than 32 words following the write reset to fail to occur. However, even in this case, address pointer control will correctly, and valid data will be output for the second and following addresses. (However, in this case the condition of note 2 and the 32 clock or longer read system reset/read jump address interval must be provided.)

Timing Charts

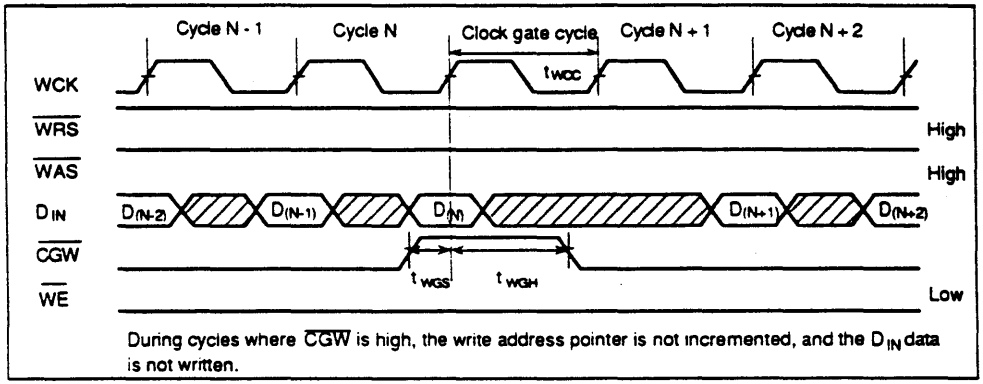
Write Cycle

- Write address reset



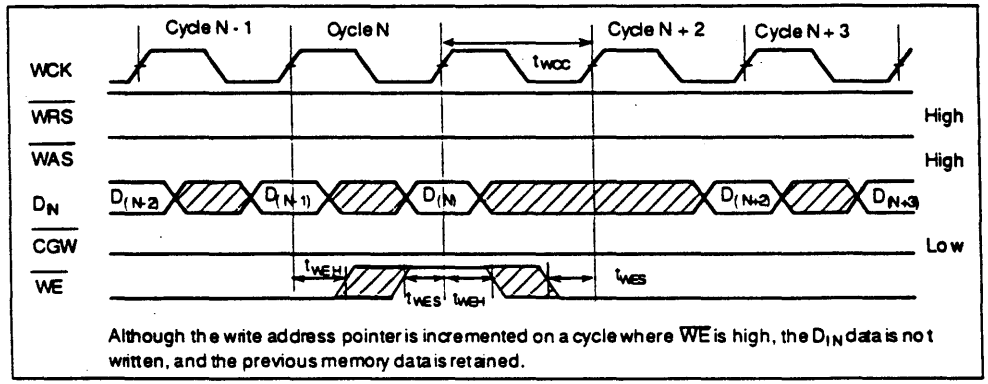
The write address pointer is reset to 0 starting with the $\overline{WRS}$ low cycle. Only the falling edge of the $\overline{WRS}$ signal is detected. Adequate margin is provided if the rise occurs at least one clock cycle before the next fall.

- Write clock gate



During cycles where $\overline{CGW}$ is high, the write address pointer is not incremented, and the D_{IN} data is not written.

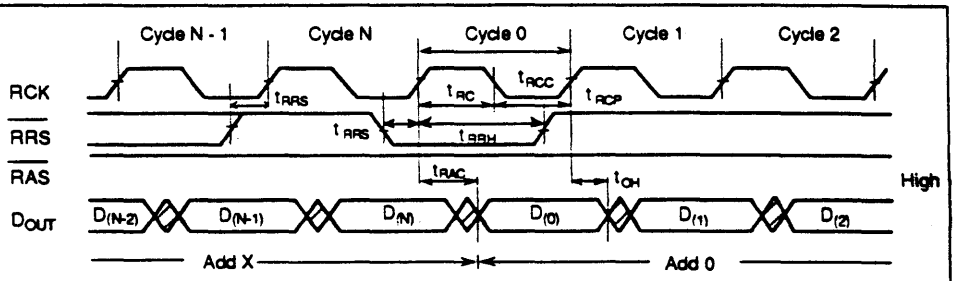
- Write enable



Although the write address pointer is incremented on a cycle where $\overline{WE}$ is high, the D_{IN} data is not written, and the previous memory data is retained.

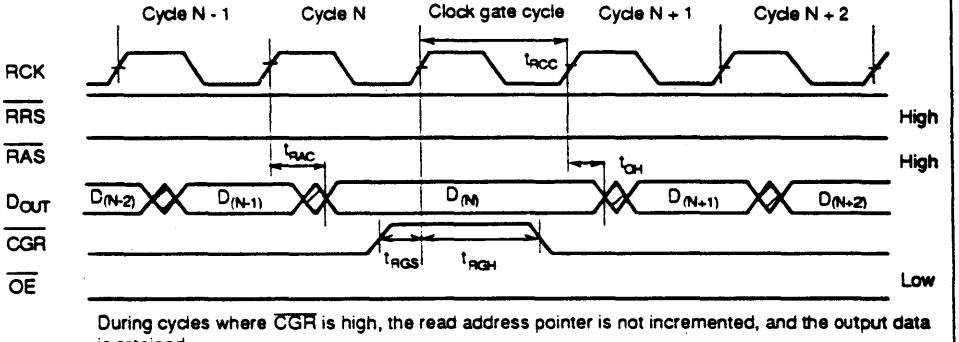
Read Cycle

- Read address reset



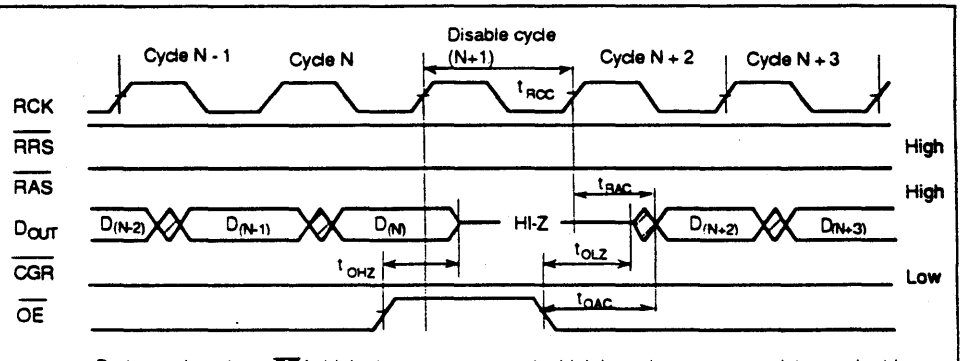
The read address pointer is reset to 0 from the cycle where $\overline{RRS}$ was low.
Only the falling edge of the $\overline{RRS}$ signal is detected. Adequate margin is provided if the rise occurs at least one clock cycle before the next fall.

- Read clock gate



During cycles where $\overline{CGR}$ is high, the read address pointer is not incremented, and the output data is retained.

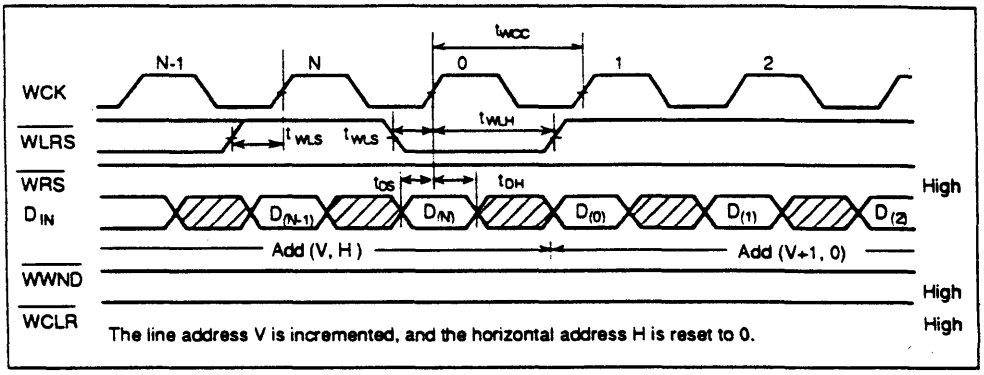
- Output enable



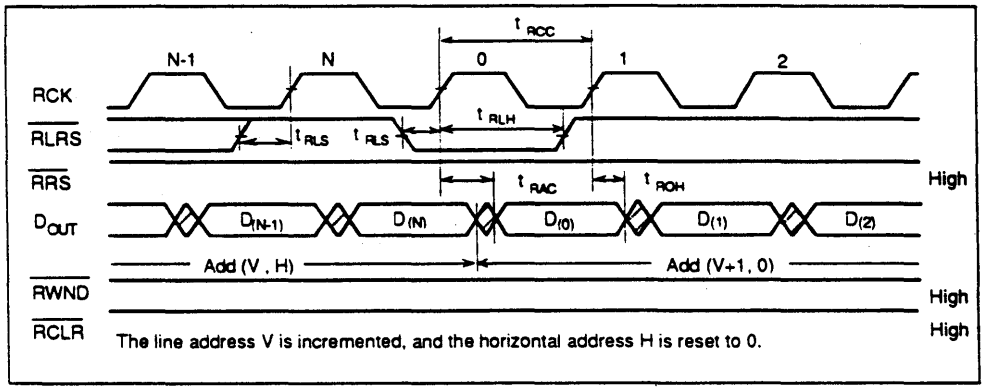
During cycles where $\overline{OE}$ is high, the output goes to the high impedance state, and the read address pointer is incremented.

Line Reset

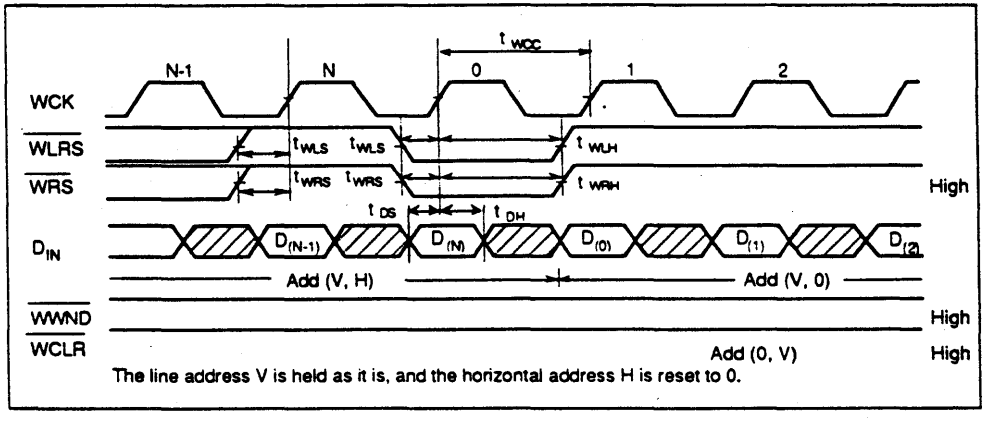
- Write line increment



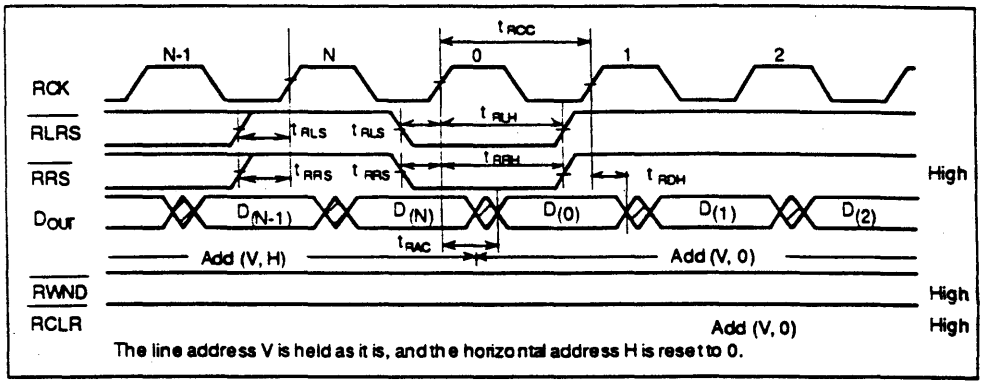
- Read line increment



- Write line hold



- Read line hold

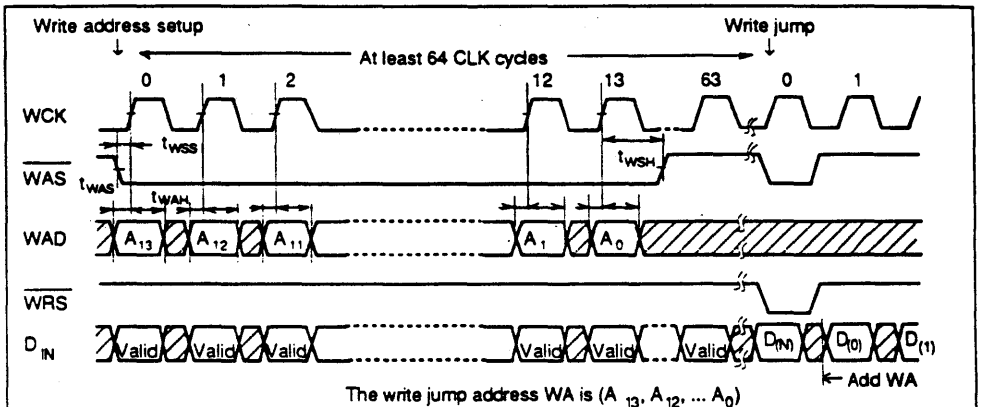


The line address V is held as it is, and the horizontal address H is reset to 0.

Jump Address Setup

1 Dimensional Addressing Mode

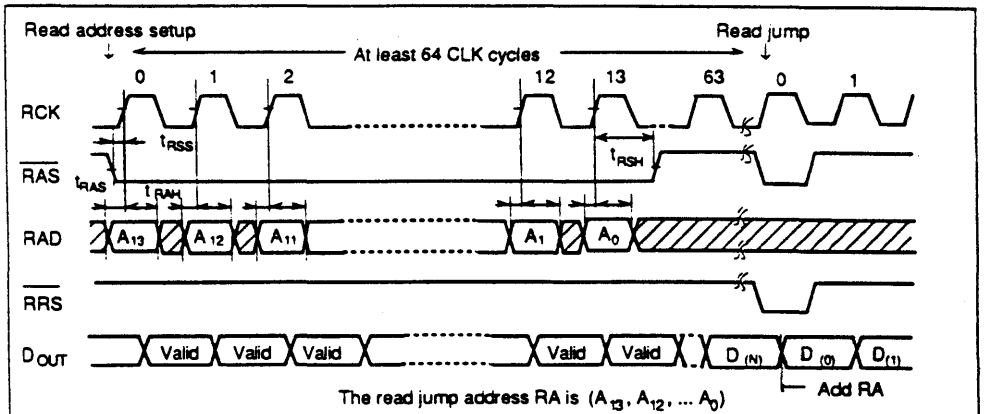
- Write address setup



The write jump address WA is (A_{13}, A_{12}, ... A_0)

After 64 cycles have passed following the start of write address setup, a jump to the set address can be performed at any time.

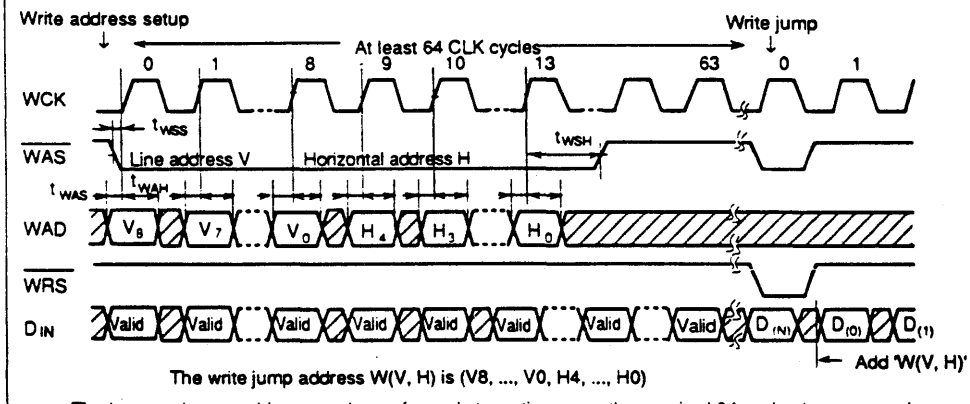
- Read address setup



After 64 cycles have passed following the start of read address setup, a jump to the set address can be performed at any time.
Read and write address setup can be performed asynchronously.

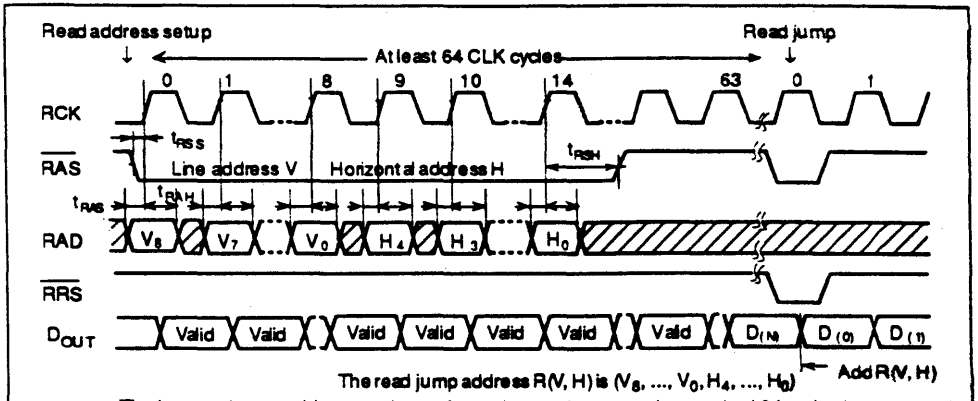
2 Dimensional Addressing Mode 1

- Write address setup (2 dimensional addressing: 324 line × 1024 dot mode)



The jump to the set address can be performed at any time once the required 64 cycles have passed following the start of write address setup.
Jump to line end block is inhibited.

- Read address setup (2 dimensional addressing: 324 line × 1024 dot mode)

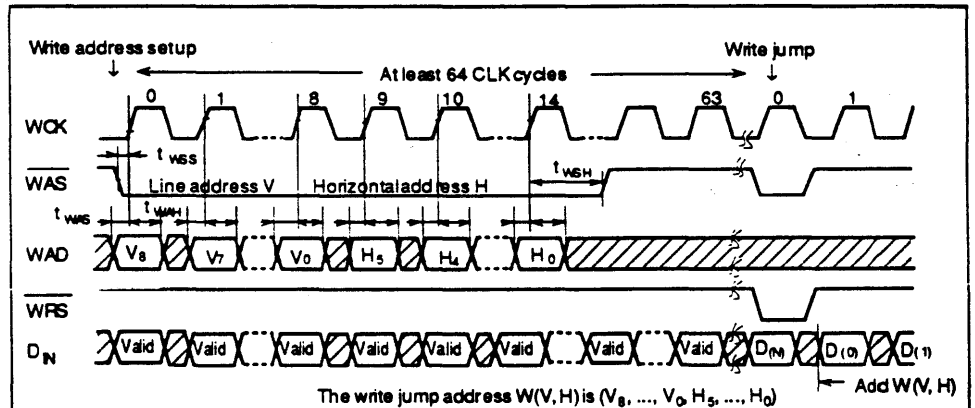


The read jump address R(V, H) is (V_8, ..., V_0, H_4, ..., H_0)

The jump to the set address can be performed at any time once the required 64 cycles have passed following the start of read address setup.
Read and write address setup can be performed asynchronously.
Horizontal address should be '0' for read jump in 2 dim. add.
Jump to line end address is inhibited.

2 Dimensional Addressing Mode 2

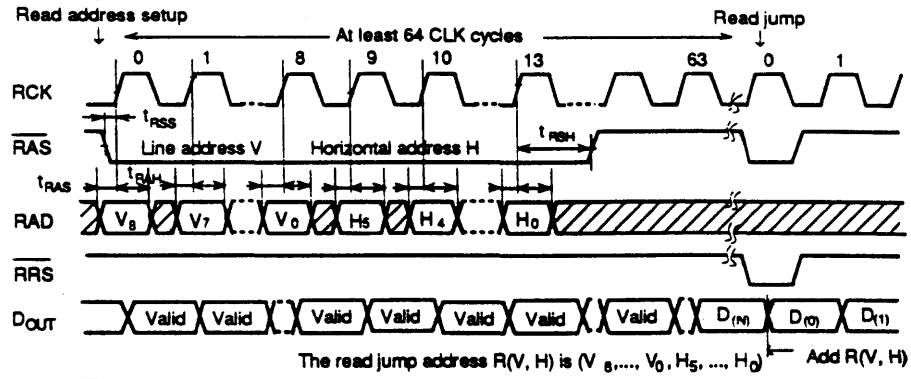
- Write address setup (2 dimensional addressing: 288 line × 1152 dot mode)



The write jump address W(V, H) is (V_8, ..., V_0, H_5, ..., H_0)

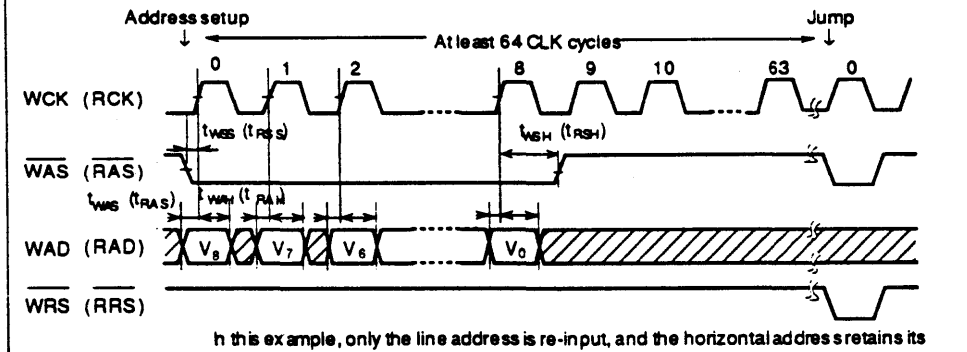
The jump to the set address can be performed at any time once the required 64 cycles have passed following the start of write address setup.
Jump to line end address is inhibited.

- Read address setup (2 dimensional addressing: 288 line × 1152 dot mode)



The jump to the set address can be performed at any time once the required 64 cycles have passed following the start of read address setup.
Read and write address setup can be performed asynchronously.
Horizontal address should be '0' for read jump in 2 dim. add.
Jump to line end address is inhibited.

- Address input mask

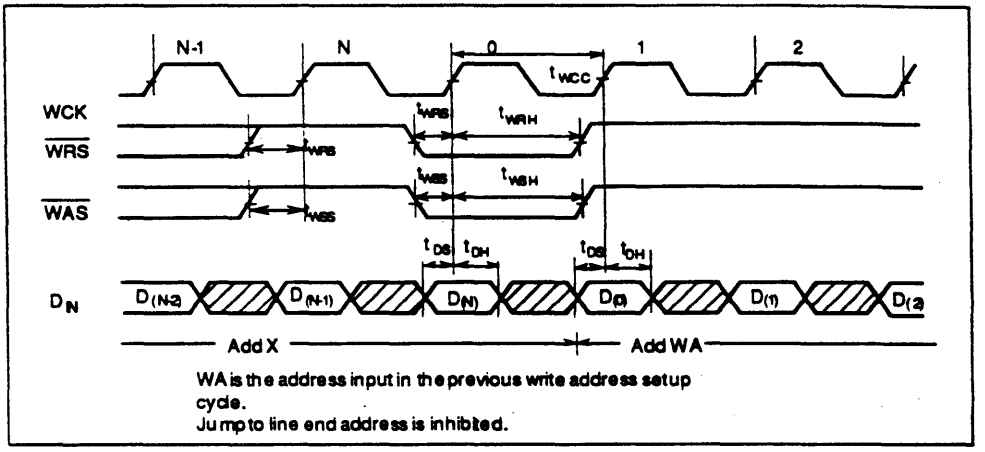


h this example, only the line address is re-input, and the horizontal address retains its previously set value.

After the start of read or write jump address setup, if $\overline{RAS}$ or $\overline{WAS}$ respectively is returned to the high level at an arbitrary bit position, the address bits input thereafter are masked, and the corresponding bits retain their previous values.

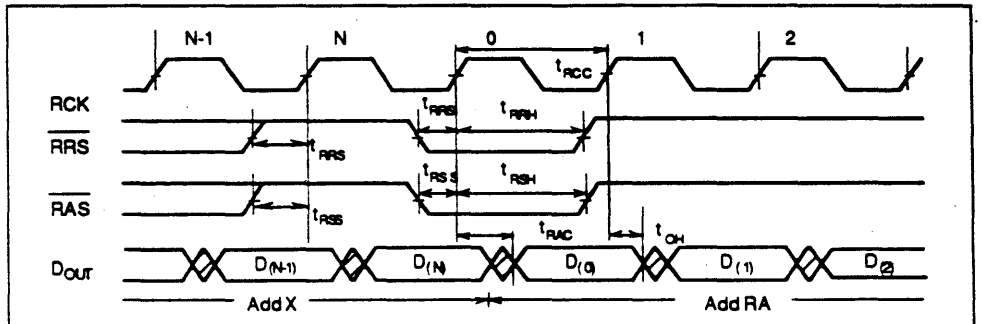
Jump

- Write jump



WA is the address input in the previous write address setup cycle.
Jump to line end address is inhibited.

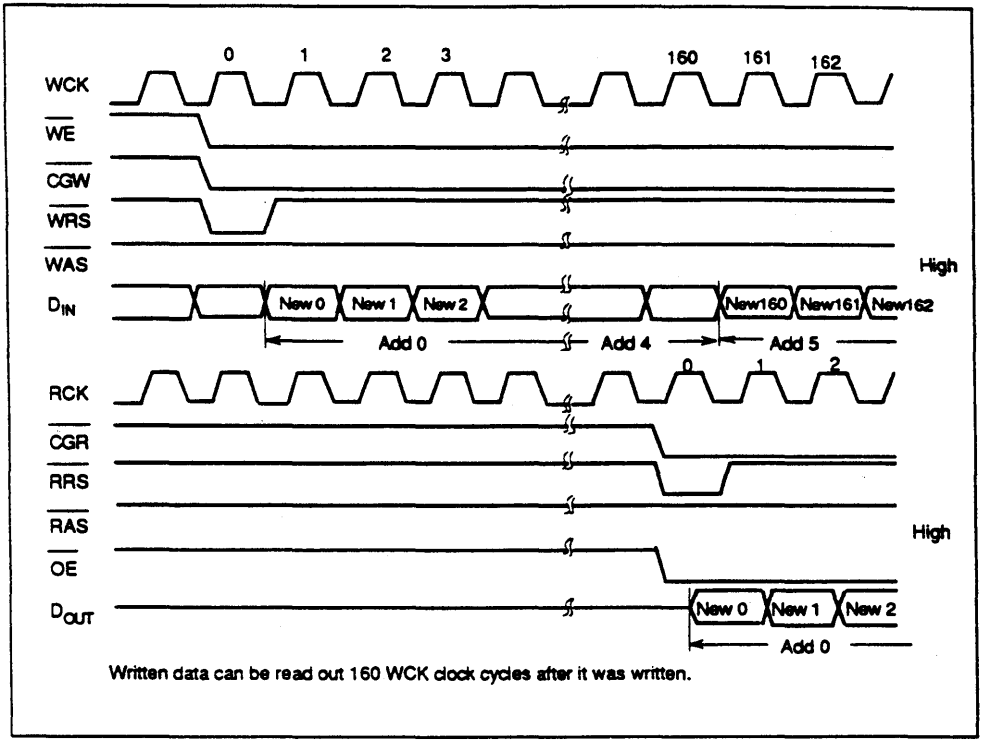
- Read jump



RA is the address input in the previous read address setup cycle.
Read jump is available for the jump address of which horizontal address is '0'.
Jump to line end address is inhibited.

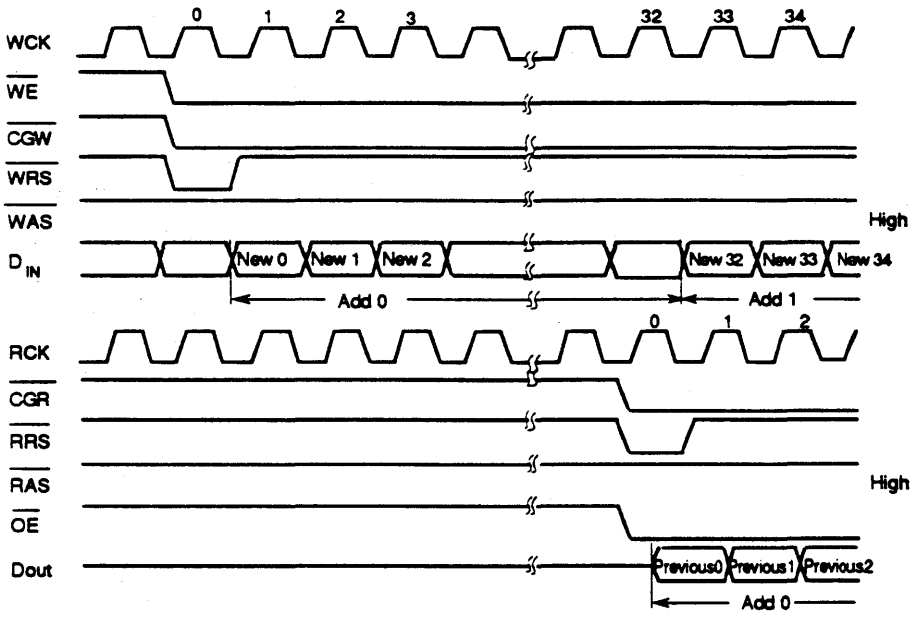
New/Previous Data Access

- New data access (address reset)



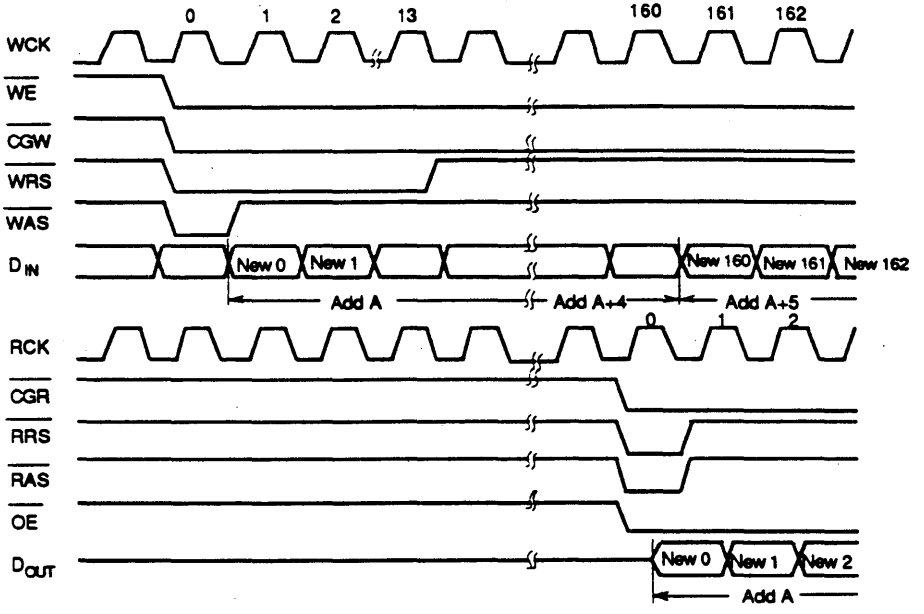
Written data can be read out 160 WCK clock cycles after it was written.

- Previous data access (address reset)



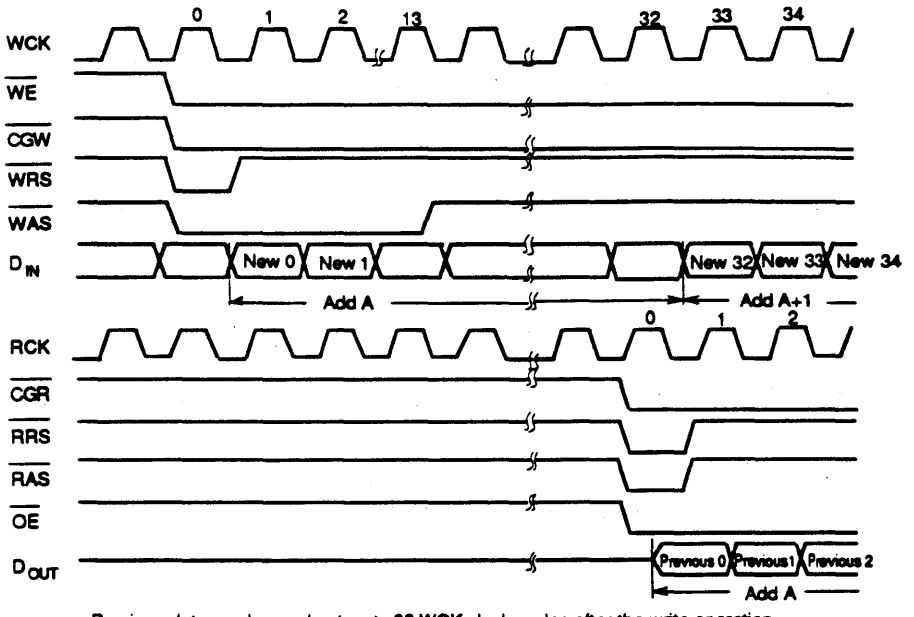
Previous data can be read out up to 32 WCK clock cycles after the write operation.

- New data access (address jump)
  (example where the read and write jump addresses are to the same location)



Written data can be read out 160 WCK clock cycles after it was written. However, it is necessary to execute the read jump address setup operation outside the time period between 32 WCK cycles before the start of write to that address and 32 WCK cycles after the completion of write to that address.

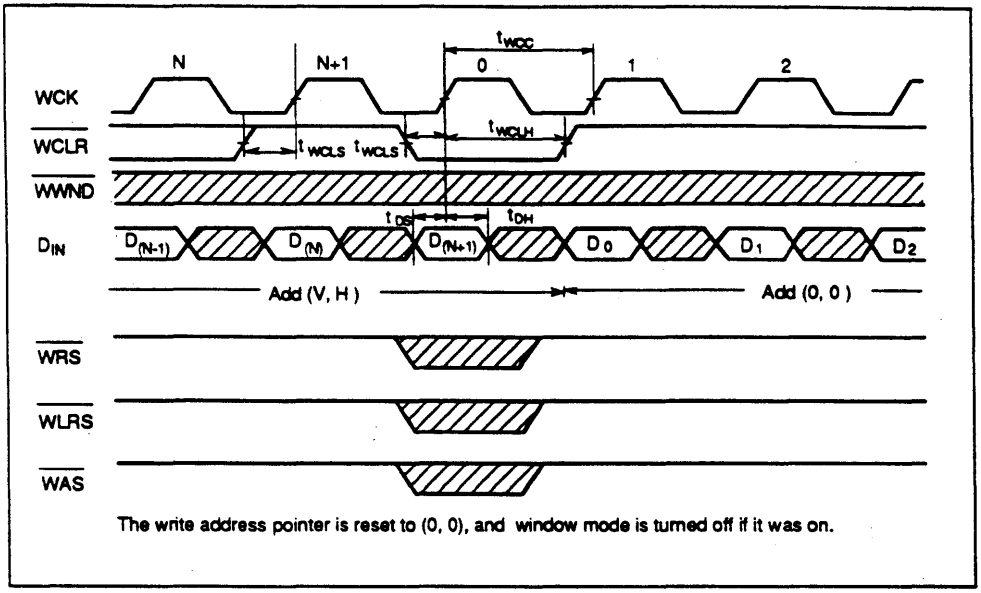
- Previous data access (address jump)
  (example when the read and write jump addresses are to the same location)



Previous data can be read out up to 32 WCK clock cycles after the write operation.

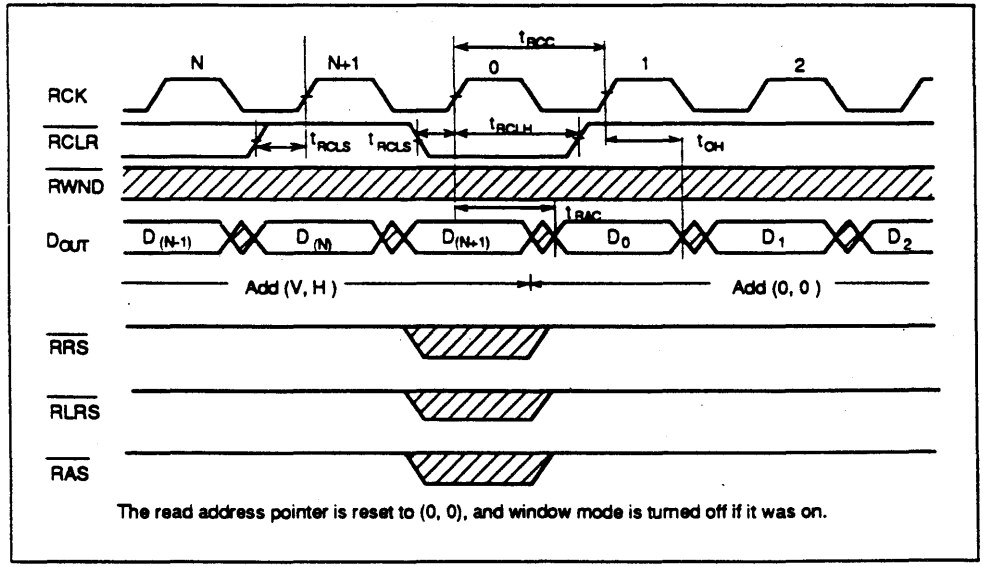
Clear

- Write clear



The write address pointer is reset to (0, 0), and window mode is turned off if it was on.

- Read clear



The read address pointer is reset to (0, 0), and window mode is turned off if it was on.

Window Scan Function

Combined Window Scan Example

In window scan mode, the destination address of a jump will be the first point in the window region, and line reset and reset operate as follows.

Line increment: Resets to the left edge of the window on the next line.

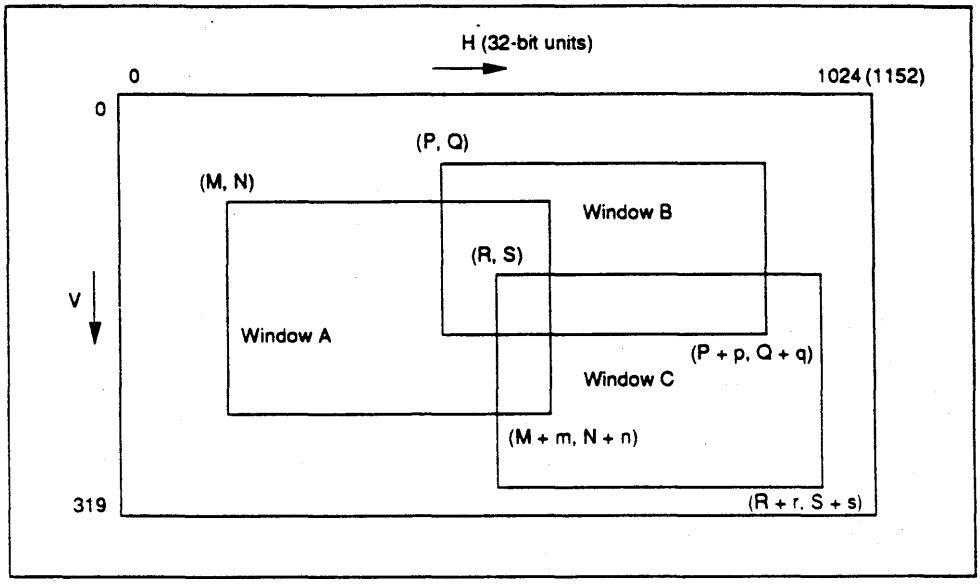
Line hold: Resets to the left edge of the window on the same line.

Reset: Resets to the first point in the window.

In this mode, addresses are generated automatically internally, so this function is useful in applications that need to scan a window region.

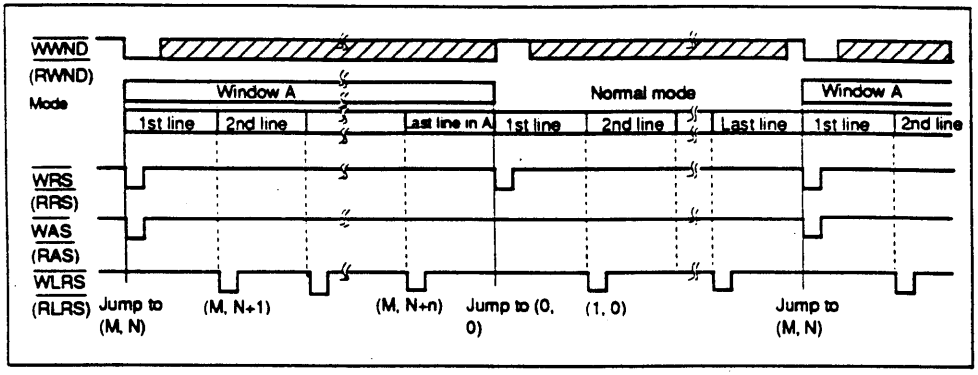
Also, completely independent window regions can be scanned by the read and write systems.

Representative application examples are presented below.

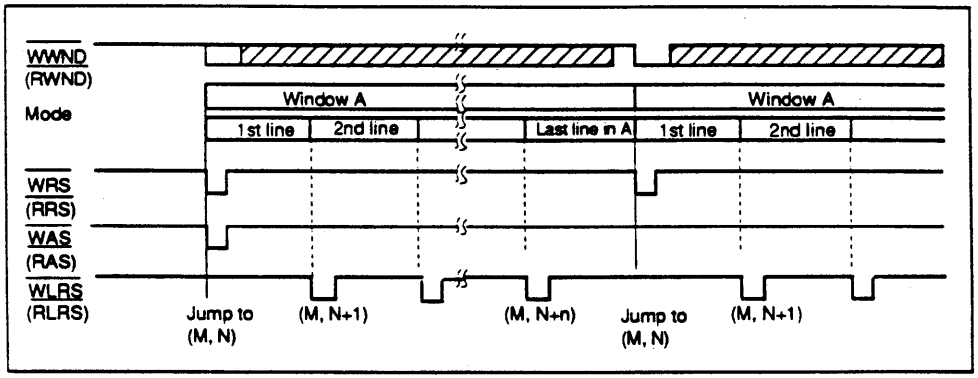


Note: Horizontal address should be '0' for read window jump.

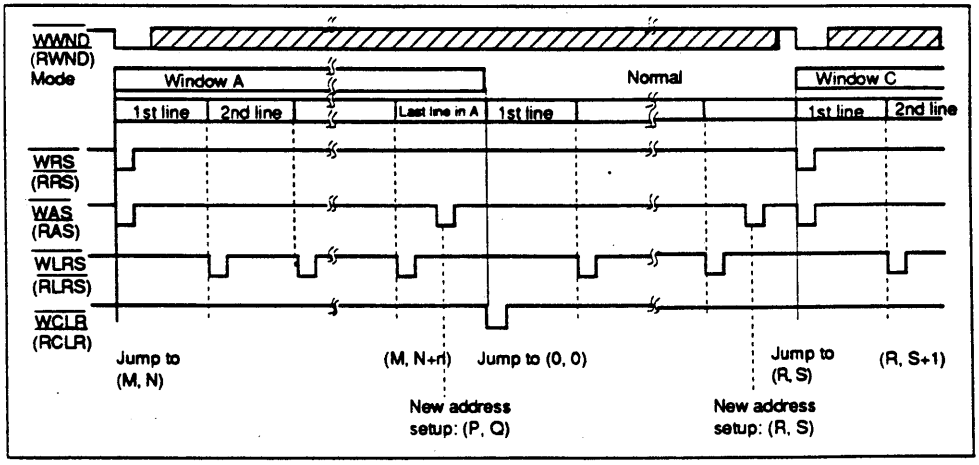
Case 1: Switching Between Normal and Window A Scan



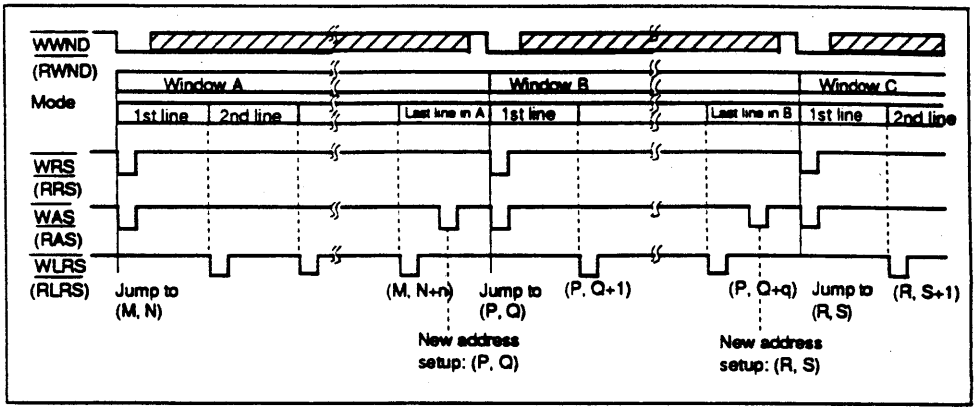
Case 2: Repeatedly Scanning Window A



Case 3: Switching from Window A Scan to Normal Scan to Window C Scan



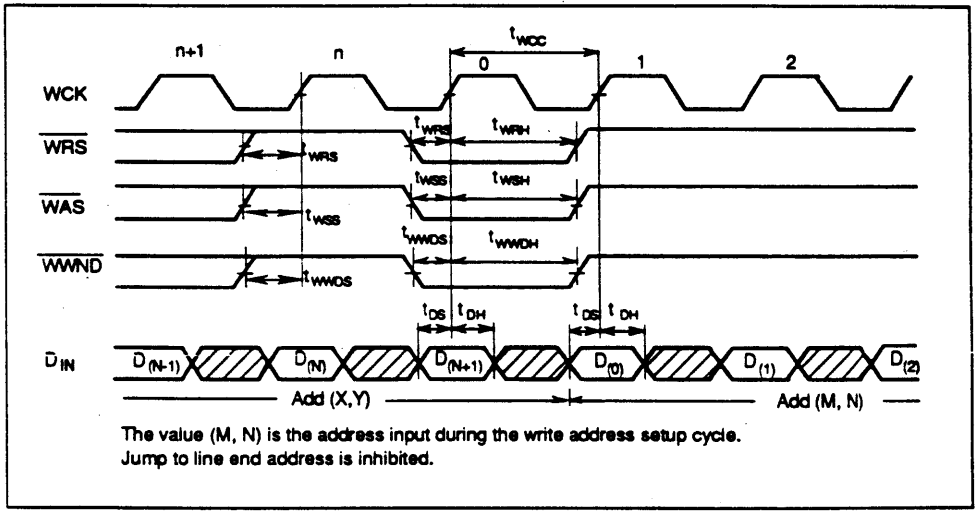
Case 4: Switching from Window A Scan to Window B Scan to Window C Scan



Window Scan Timing Charts

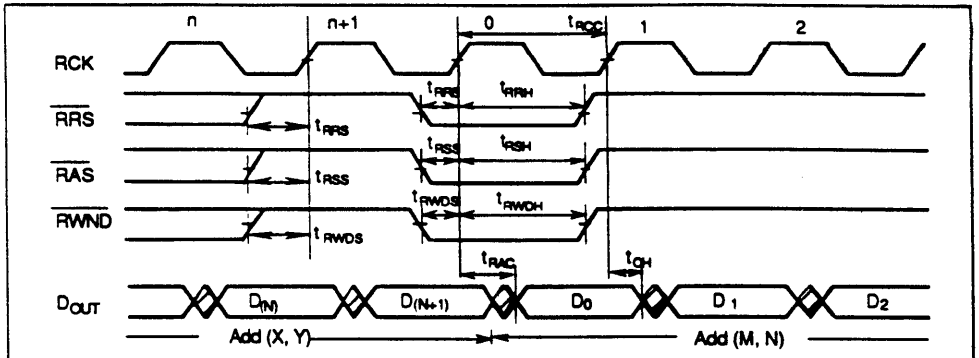
Window Jump (setup)

- Write



The value (M, N) is the address input during the write address setup cycle.
Jump to line end address is inhibited.

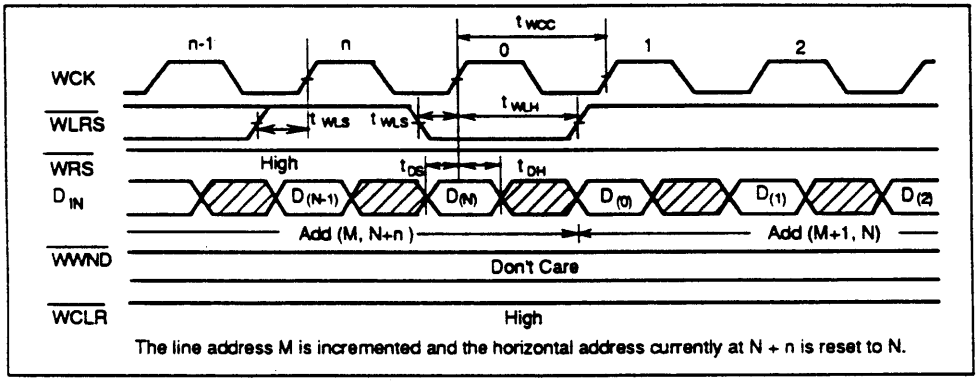
- Read



The value (M, N) is the address input during the read address setup cycle.
N should be '0' for read address.
Jump to the line end address is inhibited.

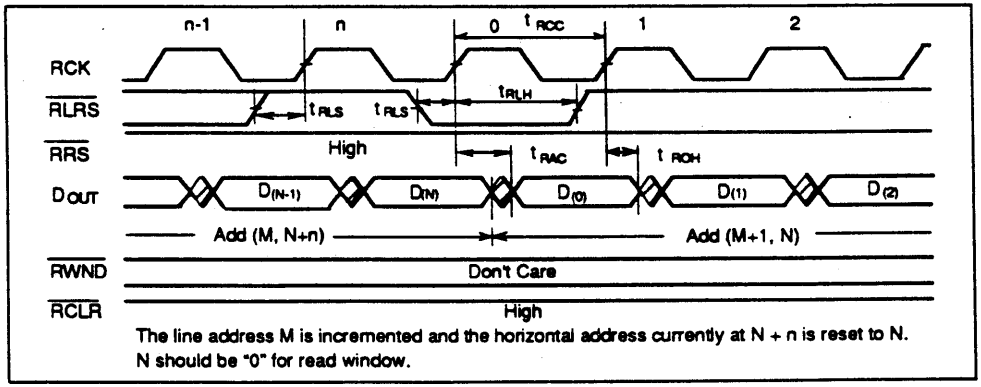
Line Increment (in window mode)

- Write



The line address M is incremented and the horizontal address currently at N + n is reset to N.

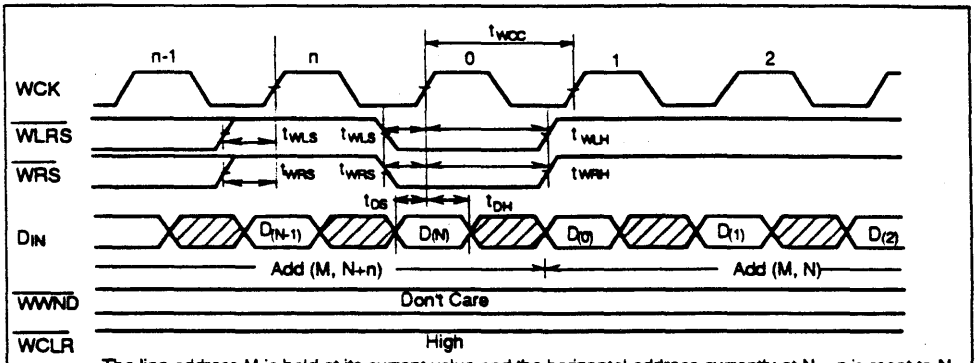
- Read



The line address M is incremented and the horizontal address currently at N + n is reset to N.
N should be "0" for read window.

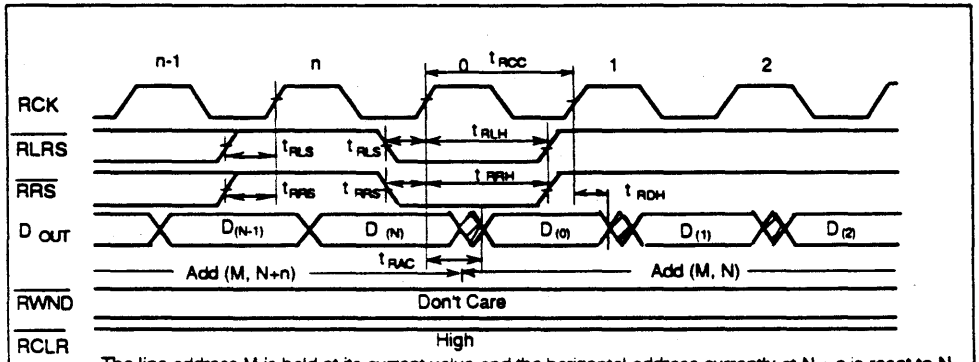
Line Hold (in window mode)

- Write



The line address M is held at its current value and the horizontal address currently at N + n is reset to N.

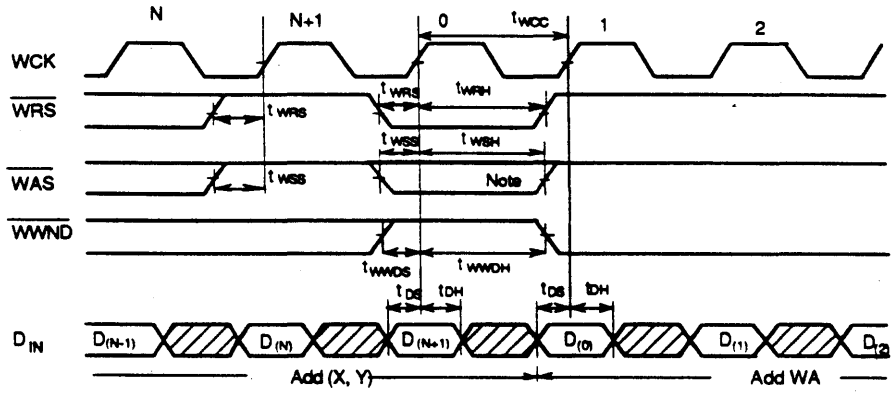
- Read



The line address M is held at its current value and the horizontal address currently at N + n is reset to N.

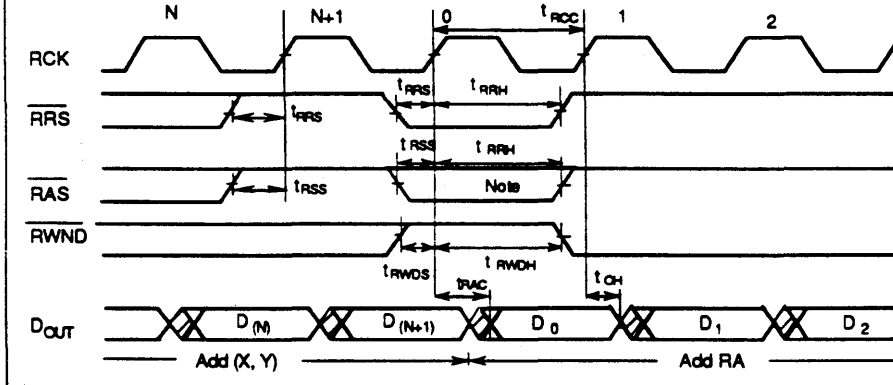
Window Clear

- Write



Note: The write address is reset to (0,0) when $\overline{WAS}$ is high.
When $\overline{WAS}$ is low, the write address jumps to WA, and in any case, the write window is cleared.

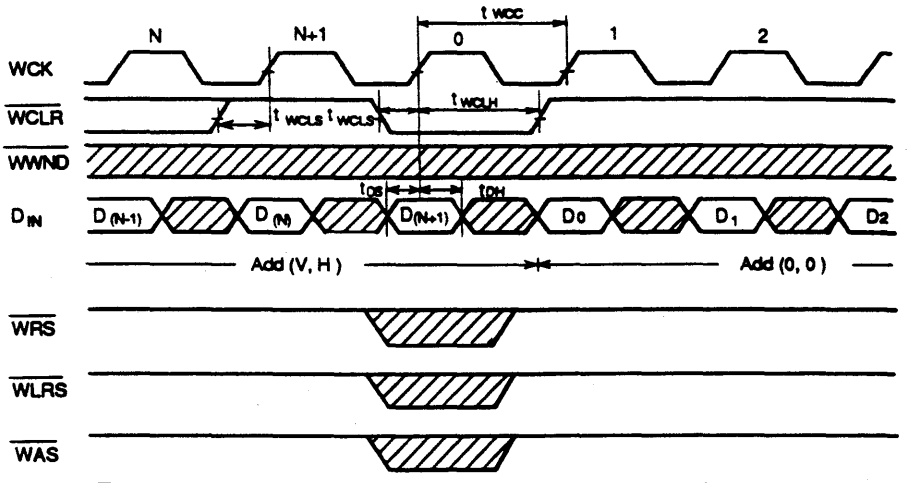
- Read



Note: The read address is reset to (0,0) when $\overline{RAS}$ is high.
When $\overline{RAS}$ is low, the read address jumps to RA, and in any case, the read window is cleared.

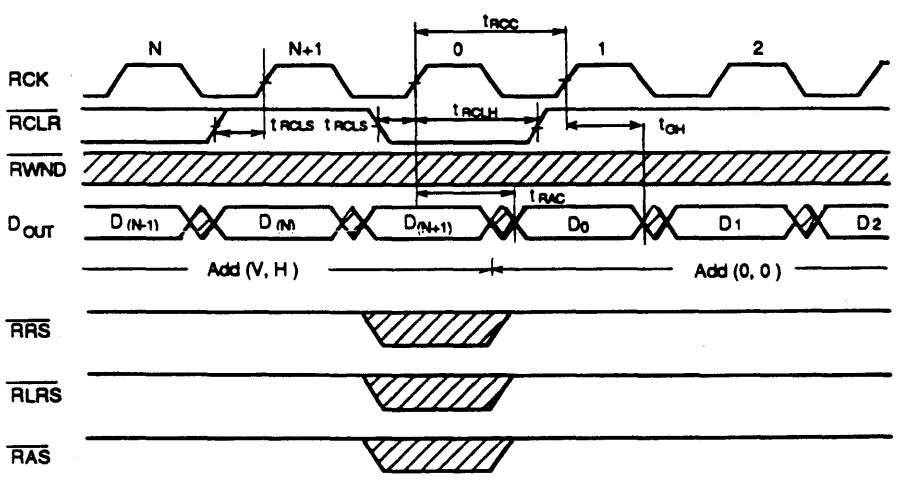
Clear

- Write clear



The write address pointer is reset to (0, 0), and window mode is turned off if it was on.

- Read clear

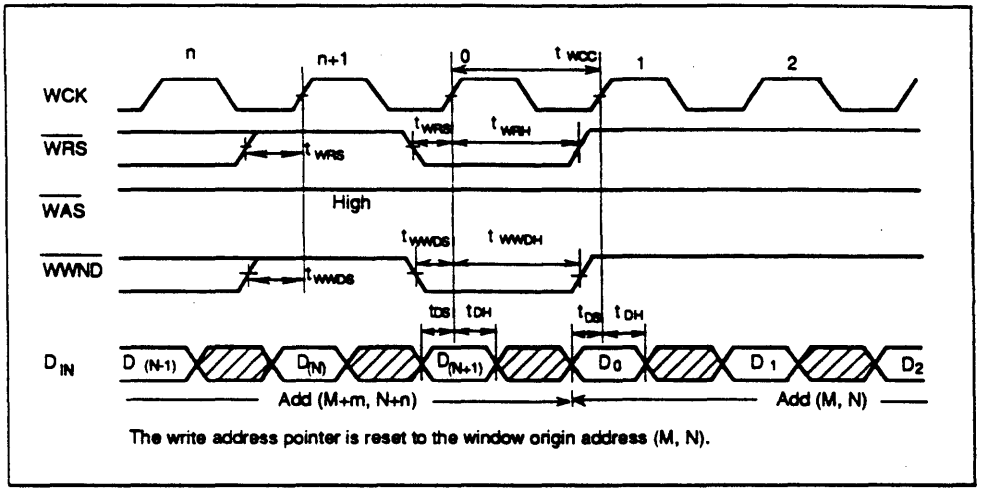


The read address pointer is reset to (0, 0), and window mode is turned off if it was on.

Reset to the Window Origin

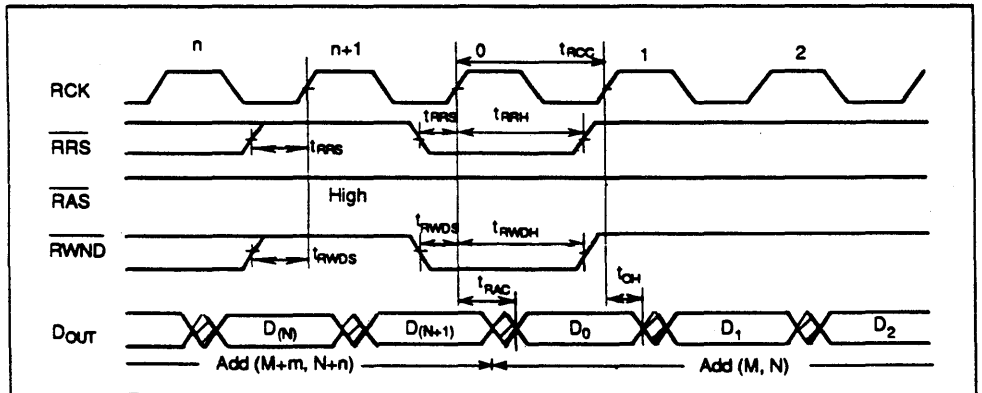
These figures show the timing charts for resetting the address pointer to the window origin address (M, N) during window scan mode execution.

- Write



The write address pointer is reset to the window origin address (M, N).

- Read

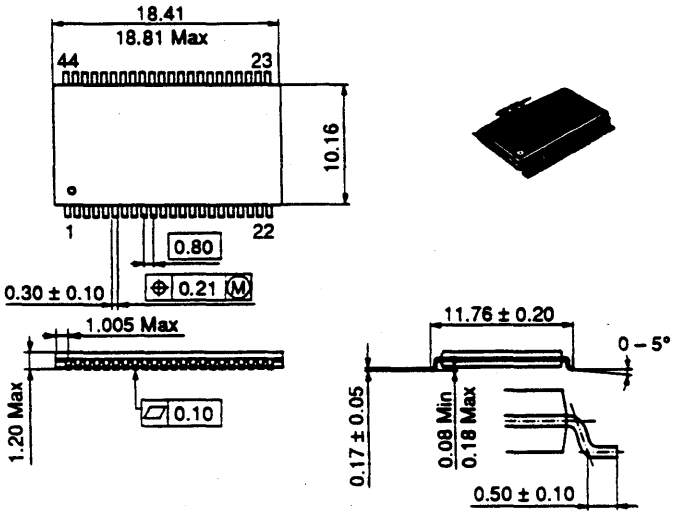


The read address pointer is reset to the window origin address (M, N).

Package Dimensions

Unit: mm

TTP44DB



Section 4

Line Memory

NEW PRODUCT

HM63021P-28/34/45
2048 x 8 - BIT LINE MEMORY

Rev. 7
Aug. 1990

HITACHI

The HM63021P is a 2048-word x 8-bit static Serial AccessMemory (SAM) with separate data inputs and outputs. Since it has an internal address counter, no external address signal is required and internal addresses are scanned serially. Using five different address scan modes, it is applicable to FIFO memories, double-speed conversions, 1H delay lines, and 1H/2H delay lines for digital TV signals. Its minimum cycle times are 28 ns and 34 ns, each corresponding to 8 fsc of PAL TV signals and NTSC TV signals. All inputs and outputs are TTL-compatible. This device is packaged in a 300-mil 28-pin DIP, and 28-pin plastic SOP.

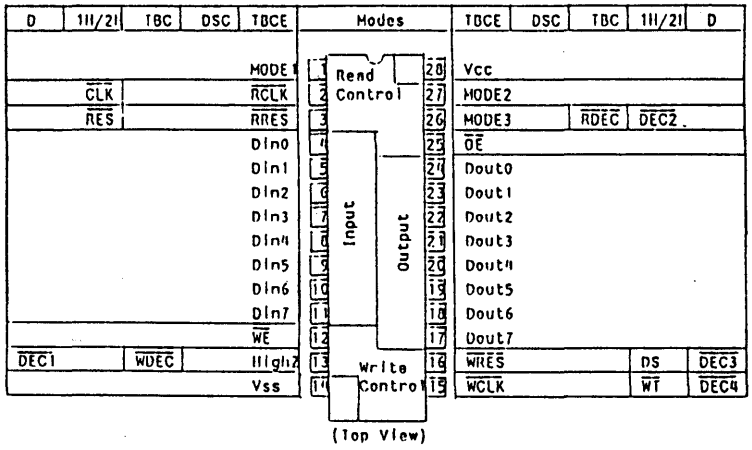
Ordering Information

Type No.	Cycle Time	Package
HM63021P-28	28 ns	300-mil 28-pin plastic DIP (DP-28N)
HM63021P-34	34 ns	
HM63021P-45	45 ns	
HM63021FP-28	28 ns	28-pin plastic SOP (FP-28DA)
HM63021FP-34	34 ns	
HM63021FP-45	45 ns	

Features

* Five modes for various applications
* Corresponds to digital TV system with 4 fsc sampling (PAL, NTSC)
* Decoder signal output pin: Fewer external circuits
* Asynchronous read/write operations
  - Separate address counters for read/write
  - No address input required
* High speed
  - Cycle time: HM63021-28: 28 ns (min)
    HM63021-34: 34 ns (min)
    HM63021-45: 45 ns (min)
* Completely static memory: No refresh required
* 8-bit SAM with separate I/O
* Low power dissipation
  - Active: 250 mW typ
* Single 5 V supply
* TTL-compatible

Pin Arrangement



Mode Table

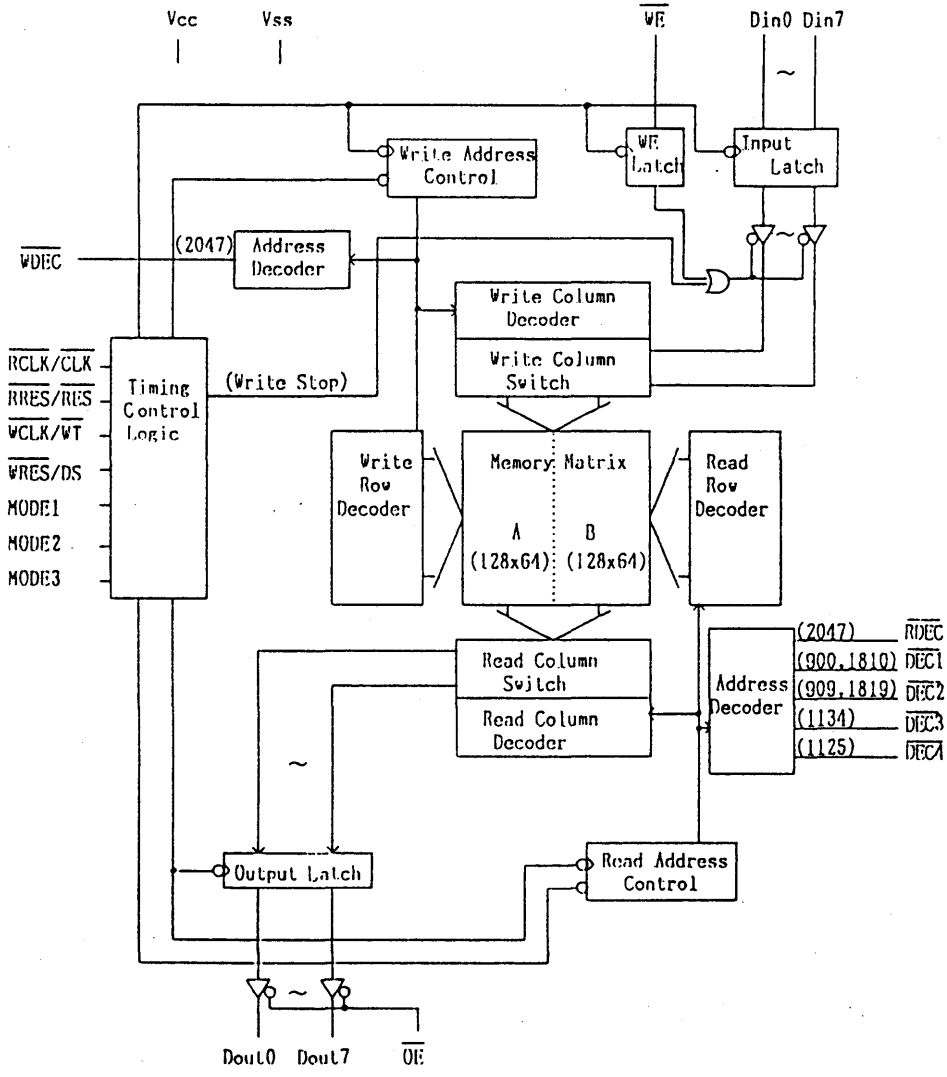
Mode Signals			Mode	Application Example
Mode1	Mode2	Mode3		
H	H	H	Time base compression/ expansion (TBCE)	Picture in picture
H	H	L	Double speed conversion (DSC)	Non interlace
H	L	- *1	Time base correction (TBC)	Time base corrector
L	H	- *1	1H/2H delay (1H/2H)	Vertical filter
L	L	- *1	Delay line (D)	Delay line

Note: *1 Decoder output signal ($\overline{\text{RDEC}}$, $\overline{\text{DEC2}}$)

Pin Description

Pin No.	Pin Name	Functions
1	MODE1	Mode input 1 (all modes)
2	$\overline{\text{RCLK}}$/CLK	Read clock input (TBCE, DSC, TBC) clock input (1H/2H, D)
3	$\overline{\text{RRES}}$/RES	Read reset input (TBCE, DSC, TBC) reset input (1H/2H, D)
4-11	Din0-Din7	Data inputs (all modes)
12	$\overline{\text{WE}}$	Write enable input (all modes)
13	HighZ/WDEC/DEC1	High impedance (TBCE, DSC) write decode pulse output (TBC) Decode pulse output 1 (1H/2H, D)
14	Vss	Ground (all modes)
15	$\overline{\text{WCLK}}$/WT/DEC4	Write clock input (TBCE, DSC, TBC) Write timing input (1H/2H) Decode pulse output 4 (D)
16	$\overline{\text{WRES}}$/DS/DEC3	Write reset input(TBCE, DSC, TBC) Delay select input (1H/2H) Decode pulse output 3 (D)
17-24	Dout0-Dout7	Data outputs (all modes)
25	$\overline{\text{OE}}$	Output enable input (all modes)
26	MODE3/RDEC/DEC2	Mode input 3 (TBCE) Read decode pulse output (TBC) Decode pulse output 2 (1H/2H, D)
27	MODE2	Mode input 2 (all modes)
28	Vcc	Power supply (+5V) (all modes)

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to Vss	V_T	-0.5* to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	-55 to +125	°C
Storage temperature under bias	Tbias	-10 to +85	°C

Note: * V_T min = -3.5 V for pulse width ≤ 10 ns

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	min	typ	max	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
	Vss	0	0	0	V
Input voltage	V_{IH}	2.4	-	6.0	V
	V_{IL}	-0.5*	-	0.8	V

Note: * V_{IL} min = -3.0 V for pulse width ≤ 10 ns

Electrical Characteristics

DC Characteristics (Ta = 0 to +70°C, Vcc = 5 V±10 %, Vss = 0 V)

Parameter	Symbol	min	typ *1	max	Unit	Test Condition
Input leakage current	$\|I_{LI}\|$	-	-	10	µA	Vcc=5.5 V Vin=Vss to Vcc
Output leakage current	$\|I_{LO}\|$	-	-	10	µA	OE=VIH Vout=Vss to Vcc
Operating power supply current	Icc	-	50	90	mA	Min.cycle, Iout=0 mA *2
Output voltage	V_{OL}	-	-	0.4	V	IOL=8mA, Dout0 - 7 $\overline{DEC}$ output pin *3
	V_{OH}	2.4	-	-	V	IOH=-4 mA, Dout0 - 7 pin
	V_{OH}	2.4	-	-	V	IOH=-1 mA, $\overline{DEC}$ output pin

Notes: *1 Typical values are at Vcc=5V, Ta=25°C and for reference only.
*2 Dout and $\overline{DEC}$
*3 I_{OL} = 6 mA for 45 ns version.

Capacitance (Ta=25°C, f=1.0 MHz)

Parameter	Symbol	min	typ	max	Unit	Condition
Input capacitance	Cin	-	-	6	pF	
Output capacitance *1	Cout	-	-	9	pF	

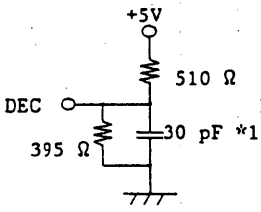
Notes: *1 13,15 - 24,26 pin
*2 This parameter is sampled and not 100 % tested.

AC Characteristics (Vcc = 5 V±10 %, Ta = 0 to 70°C unless otherwise noted)

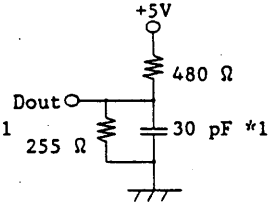
* AC Test Conditions

Input and output timing reference levels: 1.5 V
Input pulse levels: Vss to 3 V
Input rise and fall times: 5 ns

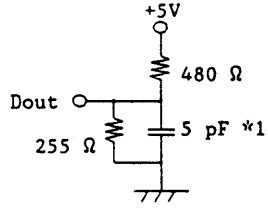
HM63021-28, -34



DEC output load

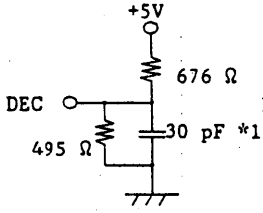


Dout output load (A)

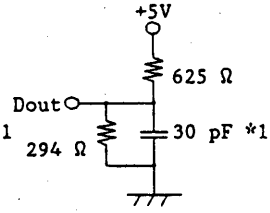


Dout output load (B) (t_{OLZ}, t_{OHZ})

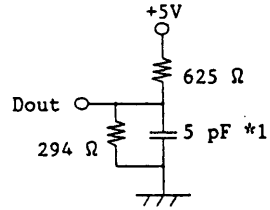
HM63021-45



DEC output load



Dout output load (A)



Dout output load (B) (t_{OLZ}, t_{OHZ})

Note: *1 Including scope and jig

Read Cycle

Parameter	Symbol	HM63021-28 min	HM63021-28 max	HM63021-34 min	HM63021-34 max	HM63021-45 min	HM63021-45 max	Unit
Read cycle time	t_{RC}	28	-	34	-	45	-	ns
Read clock width	t_{RWL}	10	-	10	-	15	-	ns
	t_{RWH}	10	-	10	-	15	-	ns
Access time	t_{AC}	-	20	-	25	-	30	ns
Decode output(fall) access time	t_{DA1}	-	20	-	25	-	30	ns
(rise)	t_{DA2}	-	40	-	50	-	60	ns
Output hold time	t_{OH}	5	-	5	-	5	-	ns
Decode output(fall) hold time	t_{DOH1}	5	-	5	-	5	-	ns
(rise)	t_{DOH2}	5	-	5	-	5	-	ns
Output enable access time	t_{OE}	-	20	-	25	-	30	ns
Output disable to output in high-Z	t_{OHZ}	0	15	0	20	0	25	ns
Output enable to output in low-Z	t_{OLZ}	5	-	5	-	5	-	ns

Write Cycle

Parameter	Symbol	HM63021-28 min	max	HM63021-34 min	max	HM63021-45 min	max	Unit
Write cycle time	t_{WC}	28	-	34	-	45	-	ns
	t_{WC}(1H/2H Mode)	56	-	68	-	90	-	ns
Write clock width	t_{WWL}	10	-	10	-	15	-	ns
	t_{WWH}	10	-	10	-	15	-	ns
Input data setup Time	t_{DS}	5	-	5	-	7	-	ns
Input data hold Time	t_{DH}	5	-	5	-	7	-	ns
$\overline{WE}$ setup time	t_{WESL}	5	-	5	-	7	-	ns
	t_{WESH}	5	-	5	-	7	-	ns
$\overline{WE}$ hold time	t_{WEHL}	5	-	5	-	7	-	ns
	t_{WEHH}	5	-	5	-	7	-	ns
$\overline{WT}$ setup time	t_{WTSL}	5	-	5	-	7	-	ns
	tWTSH	5	-	5	-	7	-	ns
$\overline{WT}$ hold time	t_{WTHL}	5	-	5	-	7	-	ns
	t_{WTHH}	5	-	5	-	7	-	ns

Reset Cycle

Parameter	Symbol	HM63021-28 min	max	HM63021-34 min	max	HM63021-45 min	max	Unit
Reset setup time	t_{RES}	8	-	9	-	10	-	ns
Reset hold time	t_{REH}	5	-	5	-	7	-	ns
Clock setup time before reset	t_{REPS}	8	-	9	-	10	-	ns
Clock hold time before reset	t_{REPH}	5	-	5	-	7	-	ns

Mode Description

* Time Base Compression/Expansion Mode

This mode turns HM63021 into a 2048-word x 8-bit FIFO memory with asynchronous input/output. The HM63021 provides 2 clocks ($\overline{RCLK}$, $\overline{WCLK}$) and 2 resets ($\overline{RRES}$, $\overline{WRES}$), one each for read and write. The internal address counters increment by 1 address clock and are reset to address 0. A write-inhibit function of HM63021 stops writing automatically after the data has been written into all addresses 0 to 2047. The write-inhibit function is released by reset using $\overline{WRES}$, and the HM63021 restarts writing into address 0.

* Double-Speed Conversion Mode

This mode turns HM63021 into a 1024-word x 8-bit x 2 memory with asynchronous input/output. It is used for generating non-interlaced TV signals. When the original signal and the inter-polated signal (1-field delay) of interlaced signals are input to the HM63021, multiplexed per dot, it outputs non-interlaced signals for each line. 8 fsc should be input to $\overline{RCLK}$ and $\overline{WCLK}$. A standard H synchronizing signal and a non-interlace H synchronizing signal are input to $\overline{WRES}$ and $\overline{RRES}$ respectively. A write-inhibit function is provided in this mode, making it applicable to PAL TV, where extra data (1135 - 1024 = 111 bits) is ignored.

* TBC Mode

This mode turns HM63021 into a 2048-word x 8-bit FIFO memory with asynchronous input/output. The HM63021 provides 2 clocks ($\overline{RCLK}$, $\overline{WCLK}$) and 2 resets ($\overline{RRES}$, $\overline{WRES}$), one each for read and write. The internal address counters increment by 1 address at each clock and are reset to address 0. The internal address counters return to address 0 after they reach address 2047. The HM63021 outputs a write decode pulse from WDEC, synchronizing it with address 2047 in the write address counter, and read a decode pulse from $\overline{RDEC}$, synchronizing it with address 2047 in the read address counter. Using these pulses, the memory area can be extended easily (multiple HM63021s can be used with ease).

* 1H/2H Delay Mode

This mode turns HM63021 into a 1024-word x 8-bit x 2 delay line with synchronous input/output. Delay time is defined by the reset period of $\overline{RES}$. Since the HM63021 outputs a 901 decode pulse ($\overline{DEC1}$) and a 910 decode pulse ($\overline{DEC2}$), connecting $\overline{DEC2}$ to $\overline{RES}$, for example, outputs 1H- and 2H-delayed signals alternately at a 8-fsc cycle when the original signal is input at a 4-fsc cycle. A write-inhibit function is provided in this mode, making it applicable to PAL TV, where extra data (1135 - 1024 = 111 bits) is ignored.

* Delay Line Mode

This mode turns the HM63021 into a 2048-word x 8-bit delay line with synchronous input/output. Delay time (3 to 2048 bits) is defined by the reset period of $\overline{RES}$. The delay is 2048 bits when $\overline{RES}$ is fixed high. Signals delayed by 910 bits to 1135 bits, for example; can be easily obtained without external circuits by just connecting selected decoded pulses on $\overline{DEC1}$ - $\overline{DEC4}$ to $\overline{RES}$.

Notes on Using HM63021

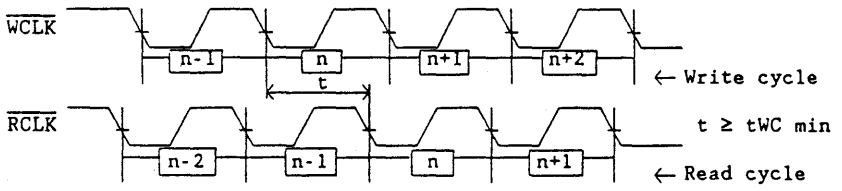
* Hitachi recommends that pin 13 (high impedance) should be fixed by pulling up or down with a resistor (of several kΩ) in TBC or DSC mode.

* Hitachi recommends that the mode signal input pins and DS pin should be fixed by pulling them up or down with a resistor (of several kΩ).

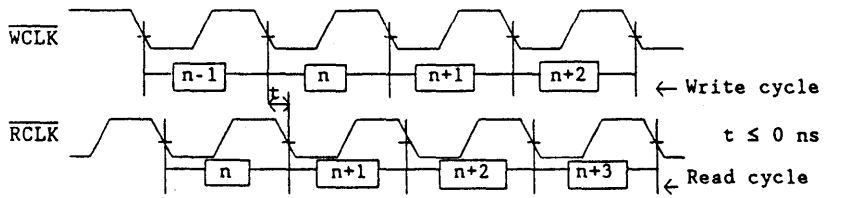
* Data integrity cannot be guaranteed when mode or DS is changed during operation.

* When a read address coincides with a write address in TBCE, TBC or DSC mode, the data is written correctly but it is not always read correctly.

(1) Read after write (3 bits delay)



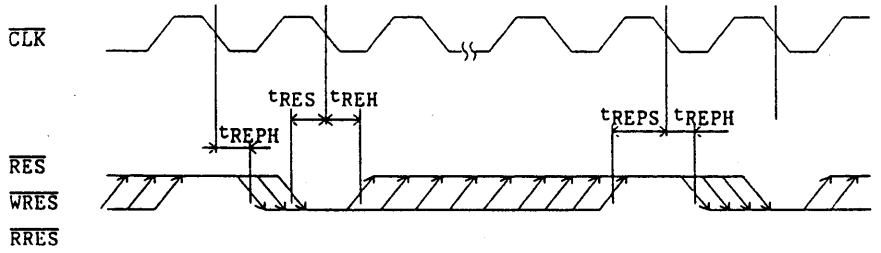
(2) Write after read (2048 bits delay)



* At power on, the output of the address counter is not defined. Therefore, operations before the system is reset cannot be guaranteed, and decode signal output is not defined until after the first reset cycle.

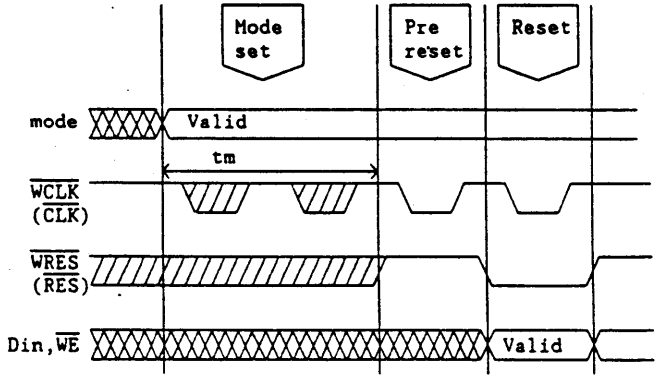
* The decode signal is latched by a decode output latch circuit at the previous address of the internal counter address and is output synchronized with the next address. For example, $\overline{WDEC}$ in TBC mode is latched at write address 2046 and is output at write address 2047. If a write reset is performed on address 2047 at this time, the write address becomes 0 and $\overline{WDEC}$ is output.
The same operation is performed in other modes.

* In the reset cycle, the input levels of $\overline{WRES}$, $\overline{RRES}$, $\overline{RES}$ are raised to satisfy t_{REH}, and are fixed high until t_{REPH} in the next pre-reset cycle is satisfied. The rise timings of the reset signals ($\overline{RES}$, $\overline{WRES}$, $\overline{RRES}$) are optionals provided that the t_{REPS} specification is satisfied. The timings at which $\overline{RES}$, $\overline{WRES}$, and $\overline{RRES}$ fall after pre-reset are also optional, provided that the t_{REPH} and t_{RES} specifications are satisfied.

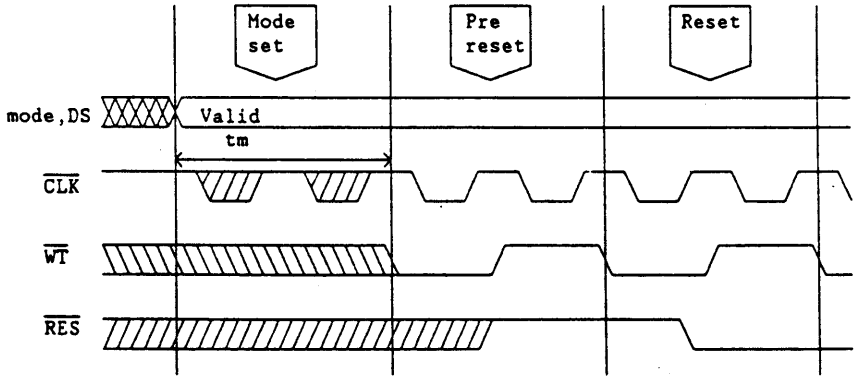


* Hitachi recommends that t_m (time between mode set and the first cycle (Pre-reset)) should be kept for 2 cycle time (56 ns/68 ns /90 ns) or more while the power supply is on.

(1) TBCE, TBC, DSC and Delay Line Mode



(2) 1H / 2H Delay Mode



Note: When mode pins are fixed with V_{CC}, V_{SS} in mode set while the power supply is on, t_m spec is not needed.

Decode Signal

When the internal address counter reaches the specified address as shown below, decode outputs become low.

Mode	Pin No.	Pin Name	Internal Address Counter	Timing of the Output Signal	Operation
TBC	13	$\overline{WDEC}$	Write 2047	After write 2047	Completion of writing on all bits is detected.
	26	$\overline{RDEC}$	Read 2047	Output of 2046	Completion of reading from all bits is detected.
1H/2H	13	$\overline{DEC1}$	Read 900 (2H)	Output of 900(1H)	By inputting this signal to pin #3, 901/1802-bit delay output is obtained.
	26	$\overline{DEC2}$	Read 909 (2H)	Output of 909(1H)	By inputting this signal to pin #3, 910/1820-bit delay output is obtained.
Delay line	13	$\overline{DEC1}$	Read 900	Output of 899	By inputting this signal to pin #3, 910-bit delay output is obtained.
			Read 1810	Output of 1809	By inputting this signal to pin #3 after the frequency of $\overline{DEC1}$ is devided into two, 1811-bit delay output is obtained.
	26	$\overline{DEC2}$	Read 909	Output of 908	By inputting this signal to pin #3, 910-bit delay output is obtained.
			Read 1819	Output of 1818	By inputting this signal to pin #3 after the frequency of $\overline{DEC2}$ is devided into two, 1820-bit delay output is obtained.
	16	$\overline{DEC3}$	Read 1134	Output of 1133	By inputting this signal to pin #3, 1135-bit delay output is obtained.
	15	$\overline{DEC4}$	Read 1125	Output of 1124	By inputting this signal to pin #3, 1126-bit delay output is obtained.

Note: When the counter is reset by reset signal (RRES, $\overline{RES}$, WRES), address becomes 0.

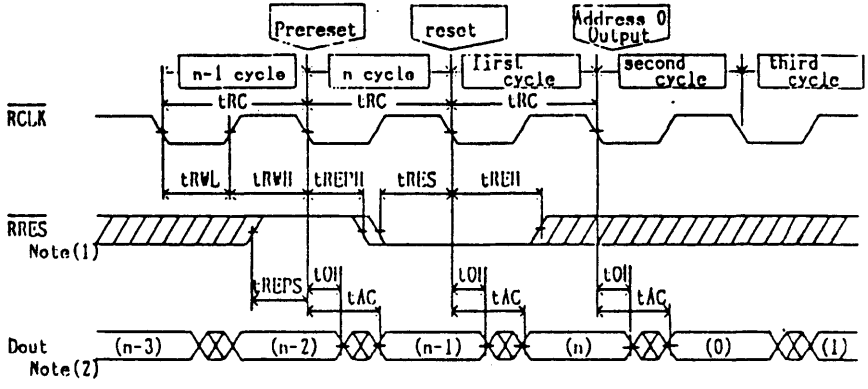
Write-inhibit Function

When internal address counter is as follows, writing is inhibited automatically for the next cycle. The write-inhibit function is cancelled by reset through $\overline{WRES}$ or $\overline{RES}$.

Mode	Write-inhibit Function (internal counter address)
TBCE	Write-inhibit after address 2047
DSC	Write-inhibit after address 1023 x 2
TBC	No function
1H/2H	Write-inhibit after address 1023
D	No function

Note: When the address counter is reset by WRES or $\overline{RES}$, address becomes 0.

Read Reset Cycle (TBCE, TBC Modes)



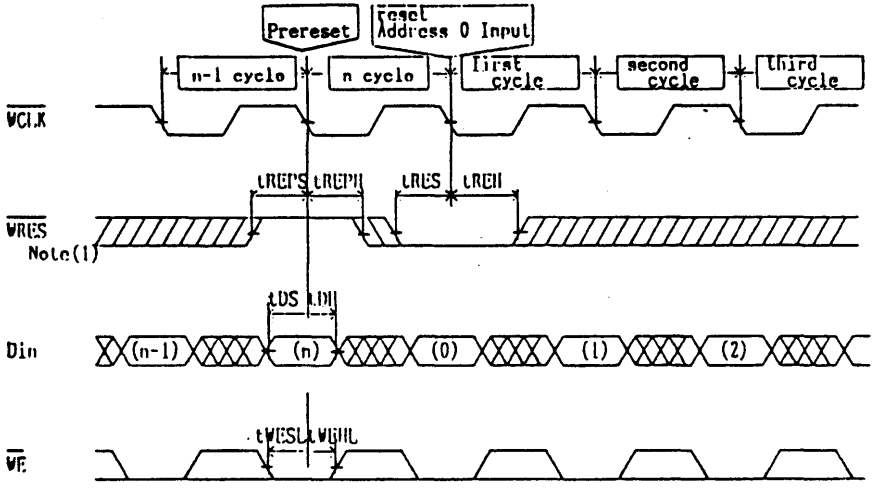
Notes: 1. The read address counter is reset at the first falling edge of $\overline{RCLK}$ after $\overline{RRES}$ falls, meeting the specifications of t_{REPS} and t_{REPH}, and it is not reset at the next falling edge of $\overline{RCLK}$ even if $\overline{RRES}$ is kept low.

When t_{RES}, t_{REH}, t_{REPS}, and t_{REPH} cannot meet the specifications, the reset operation is not guaranteed. In reset operation, both prereset and reset are required.

2. Output is from the read address of the previous cycle.

3. When $\overline{RRES}$ is fixed high, the data at the read address counter is reset after the data of address 2047 is output, and the same operation restarts.

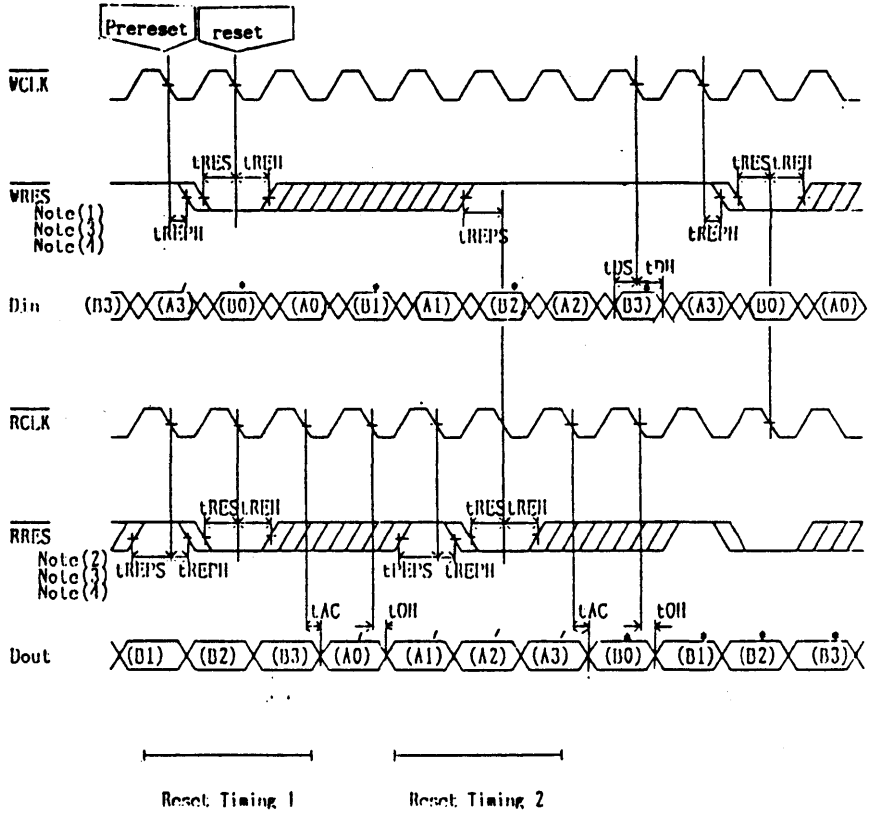
Write Reset Cycle (TBCE, TBC Modes)



Note: The write address counter is reset at the first falling edge of $\overline{WCLK}$ after $\overline{WRES}$ falls, meeting the specifications of t_{REPS} and t_{REPH}, and it is not reset at the next falling edge of $\overline{WCLK}$ even if $\overline{WRES}$ is kept low.

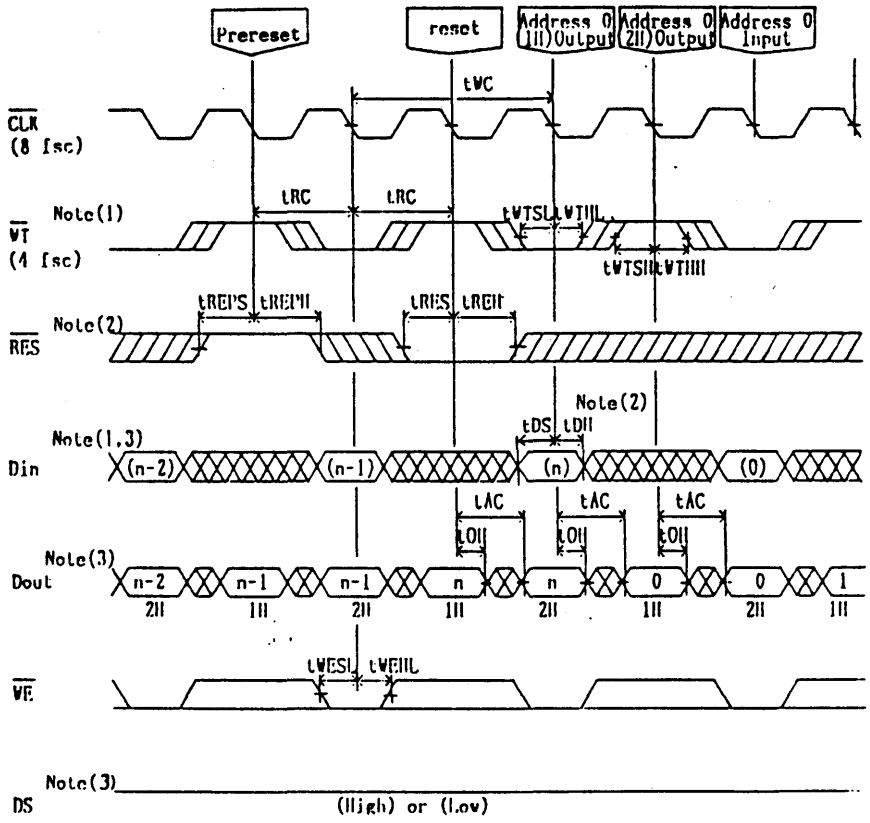
When t_{RES}, t_{REH}, t_{REPS}, and t_{REPH} cannot meet the specifications, the reset operation is not guaranteed.
In reset operation, both prereset and reset are required.

Reset Cycle (DSC Mode)



Notes:
1. The write address counter is reset at the first falling edge of $\overline{WCLK}$ after $\overline{WRES}$ falls, meeting the specifications of t_{REPS} and t_{REPH}, and it is not reset at the next falling edge of $\overline{WCLK}$ even if $\overline{WRES}$ is kept low. When t_{RES}, t_{REH}, t_{REPS}, and t_{REPH} cannot meet the specifications, the reset operation is not guaranteed.
2. The read address counter is reset at the first falling edge of $\overline{RCLK}$ after $\overline{RRES}$ falls, meeting the specifications of t_{REPS} and t_{REPH}, and it is not reset at the next falling edge of $\overline{RCLK}$ even if $\overline{RRES}$ is kept low. When t_{RES}, t_{REH}, t_{REPS}, and t_{REPH} cannot meet the specifications, the reset operation is not guaranteed.
3. When t_{REPH}, t_{RES}, and t_{REH} ($\overline{WRE}$ to $\overline{WCLK}$), or t_{REPS}, t_{REPH}, t_{RES}, t_{REH} ($\overline{PRES}$ to $\overline{RCLK}$) cannot meet the specifications, the output of video signal A is not guaranteed. (Reset Timing 1)
4. When t_{REPS} ($\overline{WRES}$ to $\overline{RCLK}$), or t_{RES}, t_{REH}, t_{REPH} ($\overline{RRES}$ to $\overline{RCLK}$) cannot meet the specifications, the interpolation signal B is not guaranteed. (Reset Timing 2)

Reset Cycle (1H/2H Mode)

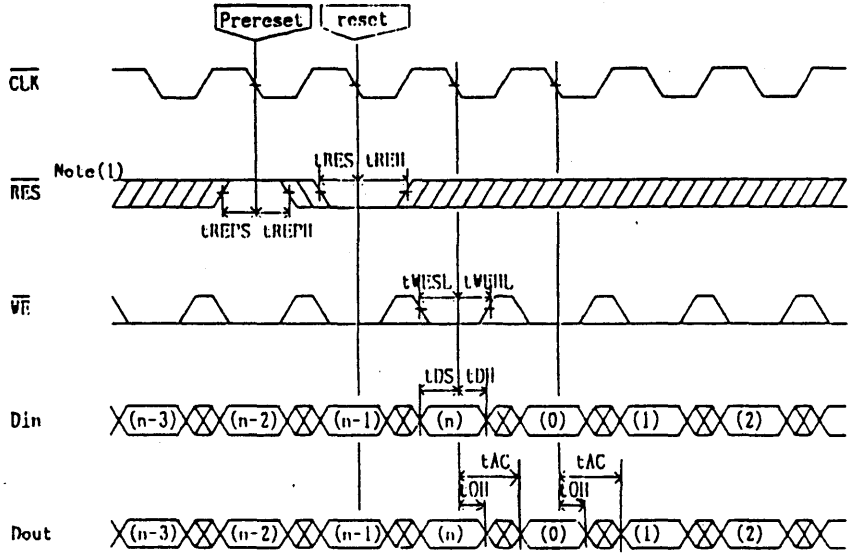


Notes: 1. $\overline{WT}$ is the input during half cycle of $\overline{CLK}$, meeting the specifications of t_{WTSL}, t_{WTHL}, t_{WTSH}, and t_{WTHH}. Data is written when $\overline{WT}$ is low. Reset is possible when $\overline{WT}$ is high.

2. Read address counter is reset at the first falling edge of $\overline{CLK}$ after $\overline{RES}$ falls, meeting the specifications of t_{REPS} and t_{REPH}, and it is not reset at the next falling edge of $\overline{CLK}$ even if $\overline{RES}$ is kept low. When t_{RES}, t_{REH}, t_{REPS}, and t_{REPH} cannot meet the specifications, the reset operation is not guaranteed. In reset operation, both prereset and reset are required.

3. When DS is fixed high, 1H output data is delayed by n bits and 2H output data is delayed by 2n-bits where 2n is the reset cycle of $\overline{RES}$. When DS is fixed low, 1H output data is delayed in n-5 bits and 2H output data is delayed in 2n-5 bits.

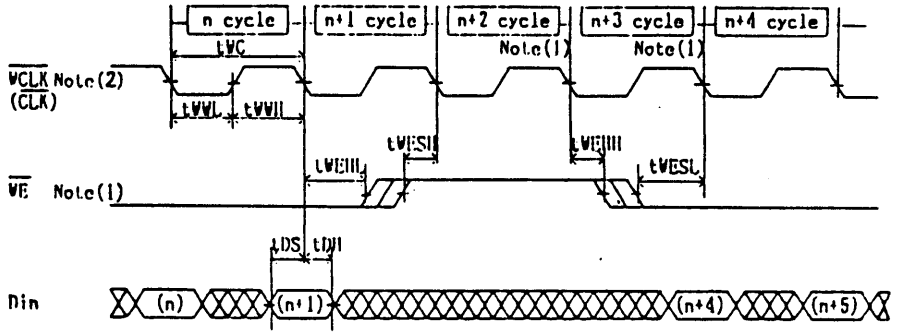
Reset Cycle (D Mode)



Note: The read address counter is reset at the first falling edge of $\overline{CLK}$ after $\overline{RES}$ falls, meeting the specifications of t_{REPS} and t_{REPH}, and it is not reset at the next falling edge of $\overline{CLK}$ even if $\overline{RES}$ is kept low.

When t_{RES}, t_{REH}, t_{REPS}, and t_{REPH} cannot meet the specifications, the reset operation is not guaranteed.
In reset operation, both prereset and reset are required.

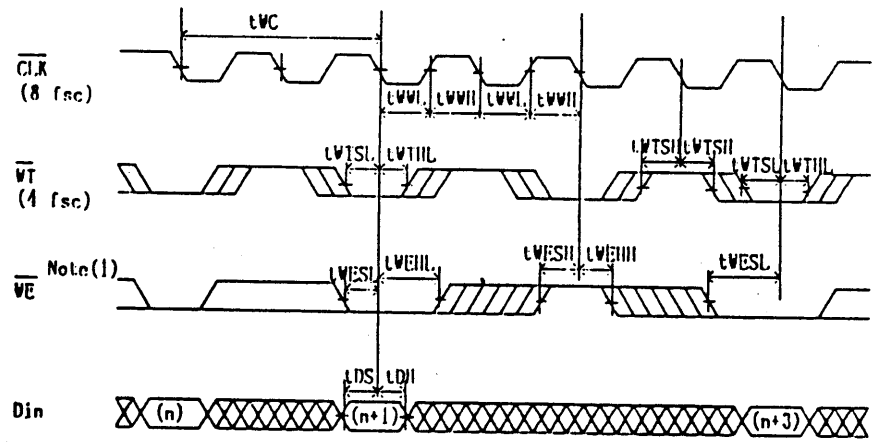
Write Enable (TBCE, DSC, TBC, D Modes)



Notes: 1. When t_{WEHL}, t_{WESH}, t_{WEHH}, and t_{WESL} cannot meet this specifications, the write enable operation is not guaranteed.

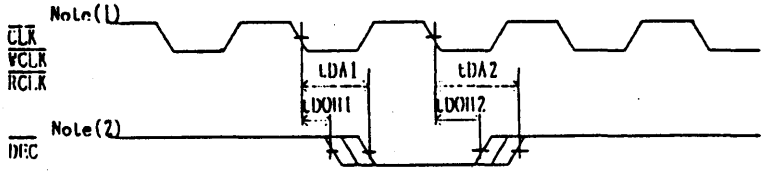
2. In the delay line mode, $\overline{CLK}$ takes the place of $\overline{WCLK}$.

Write Enable (1H/2H Mode)



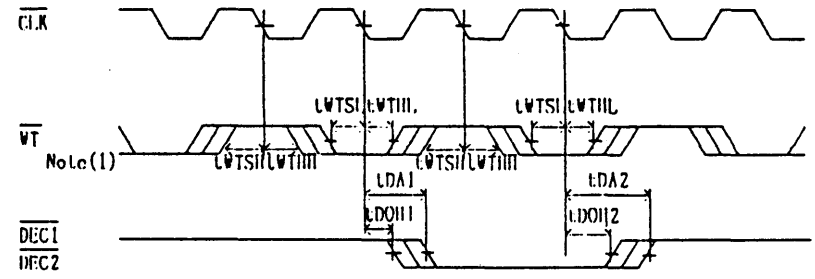
Note: When t_{WTSL}, t_{WTHL}, t_{WEHL}, and t_{WEHH} cannot meet the specifications, the write enable operation is not guaranteed.

Decode Output (TBC, D Modes)



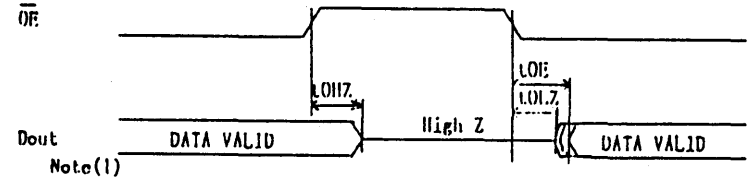
Notes: 1. In TBC mode, $\overline{WCLK}$ or $\overline{RCLK}$ takes the place of $\overline{CLK}$.
2. $\overline{DEC}$ is $\overline{WDEC}$ or $\overline{RDEC}$ in TBC, $\overline{DEC1}$, $\overline{DEC2}$, $\overline{DEC3}$, or $\overline{DEC4}$ in D mode.

Decode Output (1H/2H Modes)



Note: When t_{WTSL}, t_{WTHL}, t_{WTSH}, and t_{WTHH} cannot meet the specifications, the decode output operation is not guaranteed.

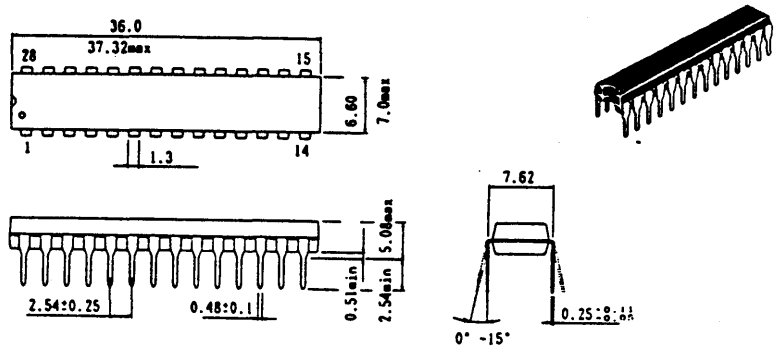
Output Enable (All Modes)



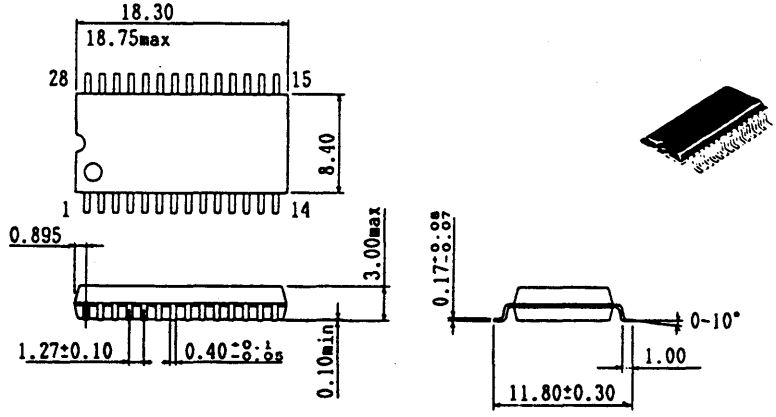
Note: Transition of t_{OHZ} and t_{WLZ} is measured ±200 mV from steady state voltage with Output Load B.
This parameter is sampled and not 100 % tested.

Package Dimensions Unit: mm

•HM63021P Series



•HM63021FP Series



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