# Headland
Technology

# HT12
## Single 286 AT Chip

## Features

- **Single chip 80286 PC/AT Compatible Solution**
- **Supports CPU speeds to 16 MHz 0 or 1 Wait State**
- **Up to 4 Meg on-board Memory**
- **EMS with 4 Registers**
- **Supports 1M, 256K, and 64K devices in mixed modes**
- **Independent Clocking Source for the AT Bus**
- **Shadow RAM Support for System and Video BIOS in 16K blocks**
- **384K Remapping in 64K blocks**
- **Hot Reset, Fast A20Gate**
- **HCMOS design for High Speed and Low Power Consumption**
- **Surface Mount Technology**

## Description

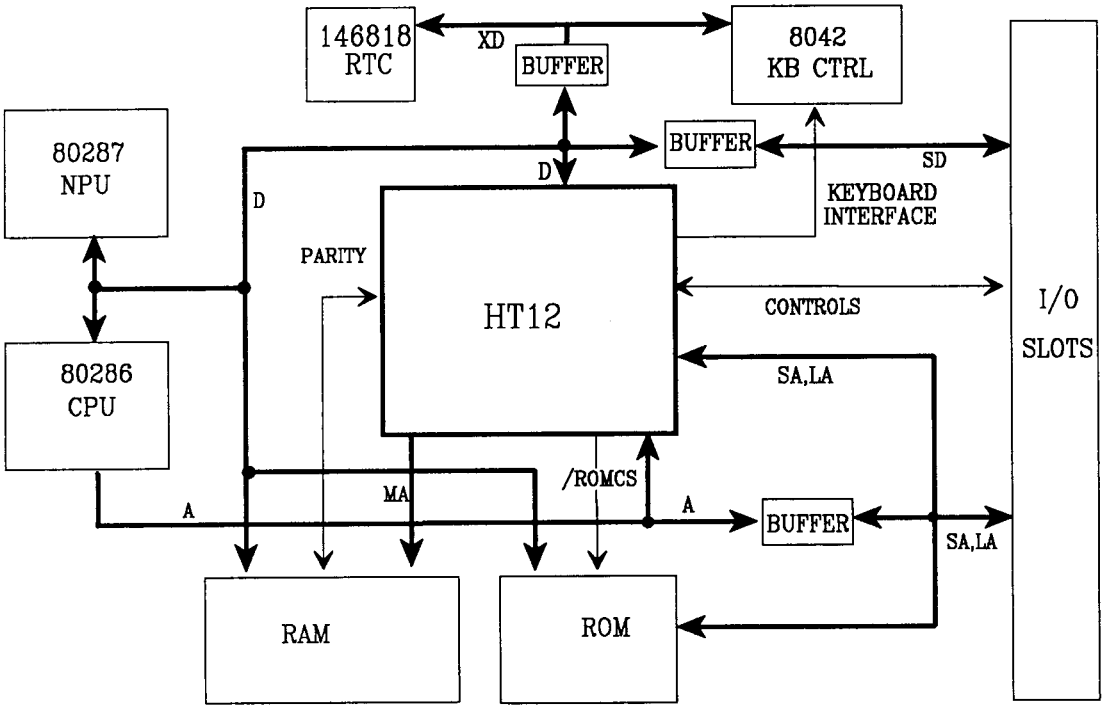
The HT12, an IBM PC/AT compatible chip, supports the 80286 CPU at clock speeds to 16MHz. This highly integrated chip solution offers high performance and reliability, with low cost, minimal power consumption, and low board-space requirements. It differs from the HT11 by the addition of 4 EMS Registers and an EMS Software Driver.

A fully PC/AT compatible system is implemented with this chip by adding a CPU/NPU, KBD CNTRL, RTC, BIOS, Memory and a few low cost TTL devices.

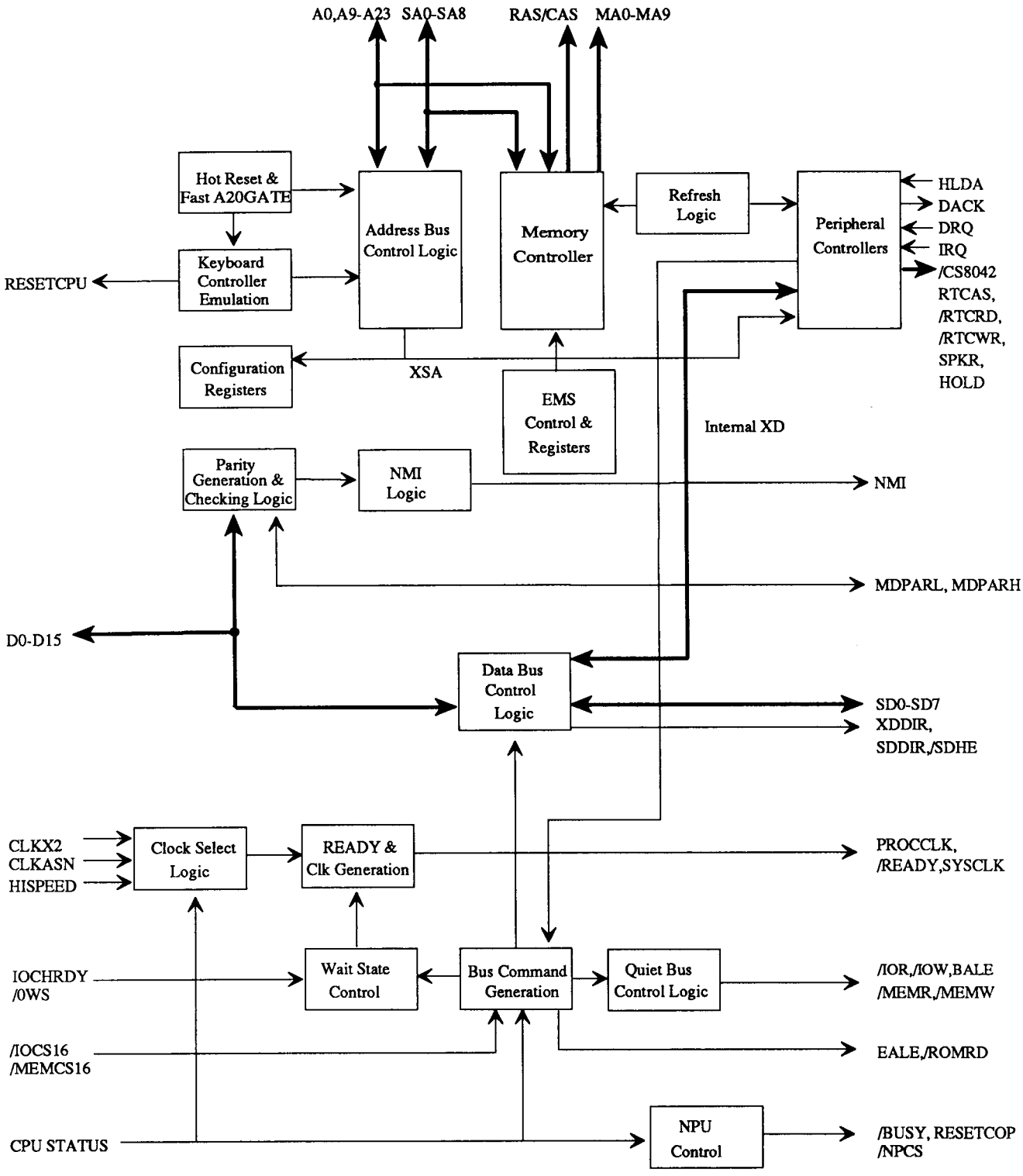
This chip supports 64K, 256K and 1M, x1 and x4, DRAMs in configurations up to 4 Meg. A 12.5MHz 0 wait-state system can be implemented using 80ns DRAMs while a 10MHz 0 wait-state system requires 100ns DRAMs. The memory controller also supports the shadow RAM feature and the Split Memory option. The Split Memory option allows the System RAM located between 640K and 1M to be remapped above top of memory.

The HT12 contains CPU and peripheral support functions; including DMA controllers, a memory mapper, timer/counters, interrupt controllers, and a bus controller. This chip replaces board address buffers, data transceivers, memory drivers, parity generators and their support circuits. This chip is packaged in a 160 pin Flat Pack.

## System Board Block Diagram



# Internal Block Diagram



The HT12 incorporates virtually all of the control circuits and "glue" logic of an AT architecture into a single CMOS VLSI chip. Circuits embedded in this device include: an 82284, 74612, 8284, 8254, two 8237s and two 8259s. The 82284 generates PROCCLK, /READY and /RESET for system use. It also provides all the CPU I/O command signals for memory, peripherals, and add-on boards. A 10-bit refresh counter produces the row address of memory during refreshes. The 74612 supplies DMA memory mapping addresses.

An 8284 uses the 14.318 MHz input clock to generate OSC and a 1.193 MHz base clock for the 8254 timer/counter. The 8254 provides 3 programmable timer/counters (channels 0 through 2). Channel 0 is used to generate IRQ 0 for the 8259A (Interrupt Controller). Channel 1 is used to generate Refresh Request cycles and Channel 2 is used for speaker tone generation.

The 8237s support Direct Memory Access, transferring 8-bit and 16-bit data between memory and I/O devices. The DMA controllers generate the correct commands to the CPU (Hold Request) and drive the appropriate bus command signals. The HT12 supports 2 8237 equivalent DMA controllers for a total of 7 DMA channels. The first DMA controller supports 8 bit peripherals and 8 or 16 bit memory using channels 0 through 3. The second DMA controller supports channels 4 through 7. Transfers between 16 bit peripherals and 16 bit memory use channels 5 through 7. Channel 4 is not available for use externally as it is used to cascade to the first DMA controller.

The two 8259s provide a total of 16 interrupt request lines (8 per 8259). IRQ0 is connected to the output of Channel 0 of the 8254 counter/timer. A second line, IRQ2 is used in cascading. IRQ1 is connected to the keyboard controller, IRQ8 is connected to the real time clock and IRQ13 is connected to the numeric processor. This leaves a total of 11 interrupt request lines that can be used externally. The 8259s issue signals to the CPU to initiate interrupt services.

The chip buffers data for the CPU(D0-15) and the system expansion data bus (SD0-7). In addition, address buffers for the System expansion bus (SA0-8), and the system board DRAMs (MA0-8) are provided. BALE is included to latch addresses from the CPU.

During memory read cycles, 16 RAM chips on the system board output MD to the HT11. Two additional RAM output MDPL (lower byte) and MDPH (upper byte). These 18 inputs are used in two 9-bit wide parity error detection circuits.

The RESETCPU signal on the HT12 is connected to the input of the 80286 processor. This signal can be generated from one of 3 sources. The first source is the PWRGOOD input signal. The next source is the /RC signal from the keyboard controller. The RESETCPU signal will also be generated if a shutdown command is generated from the 80286.

The HT12 can access 1M, x1 and x4, 256K and 64K DRAMs. The design encompasses zero or one wait state for memory operations and four wait states for I/O. The HT12 is internally programmed to insert, command delay based on the cycle type. Memory is configurable from 256K to 4 Mbytes.

The chip operates up to 16 MHz in the full commercial temperature range.

An independent clocking source for the AT bus clock is implemented. The clock input to the CLKASN (Asynchronous Clock) pin should be four times the desired bus clock speed. A 32MHz input to CLKASN will generate an 8MHz bus clock.

The chip converts 16-bit accesses for peripherals having only 8-bit wide buses; thus maintaining compatibility with the 8088 PC.

The coprocessor functions as an I/O device operating through I/O port addresses 0F8H, 0FAH, and 0FCH. The microprocessor sends OP codes and operands to the 80287 through these ports. The co-processor generates a BUSY signal to instruct the CPU that it is executing instructions. When this occurs the processor will generate a WAIT instruction to itself until the coprocessor is no longer BUSY. Once instructions are initiated, the CPU continues program execution with the co-processor.

| COMMAND DELAY, WAIT STATES BASED ON CYCLE TYPE | | | | | |
|---|---|---|---|---|---|
| COMMAND DELAY | LOCAL ROM READ | | LOCAL RAM READ | | WRITE |
| | NO | | NO | | NO |
| | AT BUS MEMORY 8 BIT | 16 BIT | AT BUS I/O 8 BIT | 16 BIT | AT BUS INTERRUPT ACKNOWLEDGE |
| COMMAND DELAY | YES | NO | YES | YES | YES |
| WAIT STATES | 4 | 1 | 4 | 1 | 4 |

## I/O Address Map

| Hex Range | Device Address | Part Number |
|---|---|---|
| 000 - 0FF | Reserved for System board I/O | |
| 000 - 01F | DMA Controller #1 | 8237A-5 |
| 020 - 03F | Interrupt Controller #1 | 8259A |
| 040 - 05F | Timer | 8254-2 |
| 060,062 - 06F | Keyboard Controller | 8042 |
| 061 | Port B Register,PPI | 8255 |
| 070 - 07F | Real Time Clock, NMI (Non-interruptable Mask) bit | |
| 080 - 08F | DMA Page Register | 74LS612 |
| 090 - 091 | Reserved | |
| 092 | Hot Reset and A20Gate | |
| 093 - 09F | Reserved | |
| 0A0 - 0BF | Interrupt Controller #2 | 8259A |
| 0C0 - 0DF | DMA Controller #2 | 8237A-5 |
| 0F0 | Clear Math Coprocessor Busy | |
| 0F1 | Reset Math Coprocessor | |
| 0F2 - 0F7 | Reserved | |
| 0F8 - 0FF | Math Coprocessor | 80287 only |
| 1ED, 1EF | Configuration Registers | |

## PORT B (8255) PPI Register, Address 61h

### Data Written

| | |
|---|---|
| Bit 3 = 1 | Disable NMI for IOCHCK(*) |
| Bit 2 = 1 | Disable NMI for Memory Parity error |
| Bit 1 | Speaker data |
| Bit 0 = 1 | Enable Timer (8254) for speaker |

### Data read back

| | |
|---|---|
| Bit 7 = 1 | Memory Parity error |
| Bit 6 = 1 | IOCHCK error(*) |
| Bit 5 | Timer 2 (8254), output |
| Bit 4 | REFRESH detect |
| Bit 3 = 1 | NMI disabled, for IOCHCK(*) |
| Bit 2 = 1 | NMI disabled for Memory Parity error(*) |
| Bit 1 | Speaker data |
| Bit 0 = 1 | Timer 2 (8254) for speaker enabled |

NOTE(*) Cleared on RESET

## Memory Configurations

The HT12 supports 8 different RAM configurations using combinations of 64K, 256K and 1M x1 or x4 DRAMs. The RAM configuration is determined by three configuration pins (DACK:2-0) on power up. The RAM configuration information is stored in the read/write System Configuration Register (index 04H and is over-ridable by software. The following is a table of valid RAM combinations.

| Configuration | /DACK (Read) | | | Bank 0 | Bank 1 | Total |
|---|---|---|---|---|---|---|
| | 2 | 1 | 0 | | | |
| 0 | 0 | 0 | 0 | 0K | 0K | 0K |
| 1 | 0 | 0 | 1 | 256K | 0K | 512K |
| 2 | 0 | 1 | 0 | 256K | 64K | 640K |
| 3 | 0 | 1 | 1 | 256K | 256K | 1M |
| 4 | 1 | 0 | 0 | 256K | 1M | 2.5M |
| 5 | 1 | 0 | 1 | 1M | 0K | 2M |
| 6 | 1 | 1 | 0 | 1M | 1M | 4M |
| 7 | 1 | 1 | 1 | - | - | Reserved |

### BIOS Shadowing and Memory Relocation

The HT12 supports BIOS shadowing in 16K blocks in the range of C0000 to FFFFF. In the case that 1M of memory is installed, the HT12 also supports relocation of memory from address A0000 to address FFFFF that are not used in shadowing to above 1M. The following table shows the various shadowing and relocation combinations. Basically, contiguous memory above A0000 that are not used in shadowing can be relocated in 64K blocks. However, the combination of shadowing in only C0000-CFFFF and F0000-FFFFF can have both A0000-BFFFF and D0000-EFFFF relocated.

| Shadow Range | Reloc Range | Memory Relocated |
|---|---|---|
| No shadowing | A0000-FFFFF | 384K |
| C0000- | A0000-BFFFF | 128K |
| D0000- | A0000-CFFFF | 192K |
| E0000- | A0000-DFFFF | 256K |
| F0000- | A0000-EFFFF | 320K |
| C0000-CFFFF, F0000-FFFFF | A0000-BFFFF, D0000-EFFFF | 256K |

For shadowing operations, the BIOS should first select the required shadowing ranges in Shadow RAM Configuration Registers 1 to 2. When an address range is selected for shadowing, it becomes accessible and write only. This allows the BIOS to load ROM data into the shadow RAM. After all the shadow RAM are loaded, the BIOS enables the shadowing feature by setting the Shadow Enable bit in the Misc Feature Enable Register, Index 14H. Once shadowing is enabled, the shadow RAM becomes read only and all read cycles to the selected address ranges will be directed to the shadow RAM.

## Hot Reset and A20Gate (Port 92H)

The HT12 supports the Hot Reset and A20Gate functions as defined in the PS/2 Technical Reference. Both functions can be used in conjunction with the keyboard controller functions.

## Independent Bus Clock

HT12 supports two independent clock sources. It normally runs off the high speed clock (CLKX2), but swithces to the asynchronous clock (CLKASN) for off-board memory accesses or I/O accesses such that AT bus timing requirements are satisfied. The AT bus clock (SYSCLK) is maintained constant at 1/4 the asynchronous clock (CLKASN).

## Address and Data Bus

The HT12 uses a modified address and data bus design. The address bus is made up of the upper 15 address signals from the CPU and the lower 9 address signals from the SA bus. The remaining portion of the SA bus and the LA bus are generated externally using TTL latches and buffers. The direct use of CPU high order addresses allows the chip to perform fast DRAM accesses. All peripherals normally connected to XA should be connected to A and SA.

The data bus consists of the 16 bit CPU D bus and the lower 8 bits of the SD bus. The upper 8 bits of the SD bus and the XD bus are generated externally using TTL buffers. The MD bus is eliminated in the design. On-board DRAMs and BIOS EPROMs are both tied to the CPU local D bus.

To generate MA for the row addresses in time for RAS, the row addresses must come directly from the CPU address bus especially when running at 16MHz. The HT12 must include address lines A(23:9) in its address bus and use the remaining pins to generate SA(0:7). Since only a portion of the SA bus is generated by the HT12, five TTL latches/buffers are used to generate the remaining SA and LA signals. Furthermore, although the column address timing is not as critical as the row address timing, to provide proper column MA, the SA signals must be latched with an Early ALE signal.

## Memory Controller

The memory controller consists of five major sub-blocks:

**ECONTROL**

The ECONTROL block is used to generate the early control signals EALE, /EMEMR and /EMEMW. The /EMEMR and /EMEMW signals are synchronized to the processor clock for master cycles. Since A1 is not directly accessible, EALE is generated for CPU shutdown/halt cycle as well, so that A1 can be accessed via SA1.

**PARGEN**

Due to the tight RAM access time, RAM data are not valid until the very end of a RAM read. To ensure sufficient time for parity generation, parity generation logic is required to allow separate read and write path for the parity generation. Moreover, on a RAM read, the data are latched to provide more time for the parity to be generated.

**ADDRTRAN**

To support mixed 64K/256K/1M DRAMs, BIOS shadowing, EMS and memory relocation, an address translating and decoding block ADDRTRAN is required. Given the RAM configuration, the ADDRTRAN block performs address translations to relocate unused memory in segments A000-F000 to the top of memory and provides output signals to indicate shadow RAM accesses and relocated memory accesses.

**RAMCONTROL**

The RAMCONTROL logic is a state machine that generates the necessary RAS, CAS and WE signals. It provides 10MHz to 16MHz accesses in either 0 or 1 wait state.

**MAGEN**

The MAGEN block generates the row and column addresses for the DRAM. It supports mixed 64K, 256K and 1M DRAM types.

Nine read/write registers are available in the P11. They consist of eight configuration registers and a Hot reset and Gate A20 control register.

The configuration registers are accessed through the two I/O ports at locations 1ED and 1EF. Port 1ED serves as an index register in determining which configuration register is accessed at port 1EF. To access a configuration register, the corresponding index must first be written into the index register at location 1ED. The index register and all configuration registers are read/write register.The status registers are Read only.

The Hot reset and Gate A20 control register is a partial emulation of the PS/2 Port 92H. It supports the Hot Reset and the Gate A20 functionalities as defined in the PS/2 Technical Reference.

## INDEXED CONFIGURATION REGISTERS

Index Port: 1ED
Data Port: 1EF

| Index | Register |
|---|---|
| 10H | System configuration Register |
| 11H | Reserved |
| 12H | Shadow RAM configuration Register 1 |
| 13H | Shadow RAM configuration Register 2 |
| 14H | Misc Feature Enable Register |
| 15H | Misc Status Register |
| 16H | Extended Information Register |
| 17H | Revision Information Register |
| 18H | Top of Memory Register |
| 19H | EMS Configuration Register |
| 20H | EMS Page Register 0 |
| 21H | EMS Page Register 1 |
| 22H | EMS Page Register 2 |
| 23H | EMS Page Register 3 |

## I/O MAPPED REGISTERS

| Address | Register |
|---|---|
| 92H | Hot Reset and A20 Gate Control Register |

NOTE: When modifying a configuration register **always** read the configuration register first. Change only the bits that must be changed, then write the data back to the register. This will insure compatability with future design features.

## SYSTEM CONFIGURATION REGISTER (INDEX: 10H)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | | WS CTRL1 | WS CTRL0 | 0 WS MEM | BUS SPEED | RAM SEL2 | RAM SEL1 | RAM SEL0 |

| Bits | Access | Default | Description (As Inputs during Power On Reset) |
|---|---|---|---|
| 2-0 | R/W | DACK2-0 | RAM Configuration<br><br>RAMSEL <2:0> — Bank 0 RAM Type — Bank 1 RAM Type — Total Size<br>0 — 0K — 0K — 0K<br>1 — 256K — 0K — 512K<br>2 — 256K — 64K — 640K<br>3 — 256K — 256K — 1M<br>4 — 256K — 1M — 2.5M<br>5 — 1M — 0K — 2M<br>6 — 1M — 1M — 4M<br>7 — - — - — - |
| 3 | R/W | DACK3 | AT Bus Speed<br>1: Low Speed on I/O<br>0: Full Speed |
| 4 | R/W | DACK5 | 0 Wait State Memory<br>1: 0 wait state memory<br>0: 1 wait state memory |
| 6-5 | R/W | DACK6-7 | Wait State Control*<br>WSCTRL (1:0)<br>0 0: 1 extra Wait State for EMS + relocation cycles<br>0 1: 1 extra Wait State for EMS cycles only<br>1 0: 1 extra Wait State for Relocation cycles only<br>1 1: No extra Wait State |
| 7 | R/W | TC | Reserved |

**Special Note**: the DACK and TC lines are used as configuration inputs during power up reset.

*Wait state control can be used to add an extra wait state for the above cycle types. When a memory cycle of the selected type occurs, the cycle will not be started until one wait state later. For example, if WSCTRL <1:0> is set to 0, EMS cycles that require memory relocation would have an extra wait state inserted; that is, a normally 0 wait state cycle would become 1 wait state and a normally 1 wait state cycle would become 2 wait state. This allows additional RAM address setup time for high speed operations.

## SHADOW RAM CONFIGURATION REGISTER 1 (INDEX: 12H)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | DC000<br>DFFFF | D8000<br>DBFFF | D4000<br>D7FFF | D0000<br>D3FFF | CC000<br>CFFFF | C8000<br>CBFFF | C4000<br>C7FFF | C0000<br>C3FFF |

| Bits | Access | Default | Description |
|---|---|---|---|
| 0 | R/W | 0 | Enable Shadowing C0000-C3FFF<br>1: Enable<br>0: Disable |
| 1 | R/W | 0 | Enable Shadowing C4000-C7FFF<br>1: Enable<br>0: Disable |
| 2 | R/W | 0 | Enable Shadowing C8000-CBFFF<br>1: Enable<br>0: Disable |
| 3 | R/W | 0 | Enable Shadowing CC000-CFFFF<br>1: Enable<br>0: Disable |
| 4 | R/W | 0 | Enable Shadowing D0000-D3FFF<br>1: Enable<br>0: Disable |
| 5 | R/W | 0 | Enable Shadowing D4000-D7FFF<br>1: Enable<br>0: Disable |
| 6 | R/W | 0 | Enable Shadowing D8000-DBFFF<br>1: Enable<br>0: Disable |
| 7 | R/W | 0 | Enable Shadowing DC000-DFFFF<br>1: Enable<br>0: Disable |

## SHADOW RAM CONFIGURATION REGISTER 2 (INDEX: 13H)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | FC000 FFFFF | F8000 FBFFF | F4000 F7FFF | F0000 F3FFF | EC000 EFFFF | E8000 EBFFF | E4000 E7FFF | E0000 E3FFF |

| Bits | Access | Default | Description |
|---|---|---|---|
| 0 | R/W | 0 | Enable Shadowing E0000-E3FFF<br>1: Enable<br>0: Disable |
| 1 | R/W | 0 | Enable Shadowing E4000-E7FFF<br>1: Enable<br>0: Disable |
| 2 | R/W | 0 | Enable Shadowing E8000-EBFFF<br>1: Enable<br>0: Disable |
| 3 | R/W | 0 | Enable Shadowing EC000-EFFFF<br>1: Enable<br>0: Disable |
| 4 | R/W | 0 | Enable Shadowing F0000-F3FFF<br>1: Enable<br>0: Disable |
| 5 | R/W | 0 | Enable Shadowing F4000-F7FFF<br>1: Enable<br>0: Disable |
| 6 | R/W | 0 | Enable Shadowing F8000-FBFFF<br>1: Enable<br>0: Disable |
| 7 | R/W | 0 | Enable Shadowing FC000-FFFFF<br>1: Enable<br>0: Disable |

## MISC FEATURE ENABLE REGISTER (INDEX: 14H)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | | | MEM PAR DIS | ENABLE 64K BIOS | 256K-640K | RELOC ENABLE | SHADOW ENABLE | QUIET BUS |

| Bits | Access | Default | Description |
|---|---|---|---|
| 0 | R/W | 1 | Quiet Bus Enable<br>1: Enable<br>0: Disable |
| 1 | R/W | 0 | Enable Shadowing Function<br>1: Enable<br>0: Disable |
| 2 | R/W | 0 | Enable Relocation Function<br>1: Enable<br>0: Disable |
| 3 | R/W | 1 | Enable Memory 40000H-9FFFFH<br>1: Enable<br>0: Disable |
| 4 | R/W | 0 | Enable 64K BIOS<br>This option selects the size of the system BIOS. When enabled, the system BIOS occupies only the 64K addressing space F000:0000-F000:FFFF. When disabled, the system BIOS occupies the normal AT compatible 128K addressing space E000:0000-F000:FFFF.<br>1: Enable<br>0: Disable |
| 5 | R/W | 0 | Memory Parity Disable<br>This option allows memory parity to be disabled regardless of the port 61H bit 2 setting.<br>0: Don't disable parity<br>1: Disable Parity |
| 6-7 | R/W | | Reserved<br>Must be set to 0 by BIOS on power up. |

## MISC STATUS REGISTER (INDEX: 15H)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | 0 | 0 | 0 | 0 | 0 | 0 | NMI EN | 8042 A20GATE |

| Bits | Access | Default | Description |
|---|---|---|---|
| 0 | R | | 8042 A20Gate<br>1: A20 Enabled<br>0: A20 Forced Low |
| 1 | R | | NMI Enable Status<br>1: NMI Enabled<br>0: NMI Disabled<br>(inverse of data written at Port 70) |
| 2-7 | R | 0 | Reserved |

## EXTENDED INFO REGISTER (INDEX: 16H)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Default | Description |
|---|---|---|---|
| 0-7 | R | 0 | Reserved |

## REVISION INFO REGISTER (INDEX: 17H)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | CHIP ID | CHIP ID | CHIP ID | CHIP ID | REV | REV | REV | REV |

| Bits | Access | Default | Description |
|---|---|---|---|
| 3-0 | R | | Revision Number 0= Rev. A |
| 7-4 | R | 1 | HT12 Identification Number |

## TOP OF EXTENDED MEMORY REGISTER (INDEX: 18H)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | | | TA 21 | TA 20 | TA 19 | TA 18 | TA 17 | TA 16 |

| Bits | Access | Default | Description |
|---|---|---|---|
| 0-5 | R/W | 03FH | Top of Extended Memory<br>This register specifies the top of extended memory with a granularity of 64K. Extended memory address must be less than or equal to the Top of Memory setting. The memory above the Top of Extended Memory and below the total available memory can be used for EMS. This register defaults to 03FH (No EMS memory). On power up, the BIOS should set this register to reflect the actual top of extended memory. |
| 6-7 | | | Reserved |

## EMS Configuration Register (Index: 19H)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | EMS EN | PAGE ADDR2 | PAGE ADDR1 | PAGE ADDR0 | PAGE 3 EN | PAGE2 EN | PAGE1 EN | PAGE0 EN |

| Bits | Access | Default | Description |
|---|---|---|---|
| 0 | R/W | 0 | Page Enable 0<br>1: Enable 0: Disable<br>If the Global EMS Enable is on (1), the enable bit associated with each EMS page enables or disables the corresponding page. |
| 1 | R/W | 0 | Page Enable 1<br>1: Enable 0: Disable |
| 2 | R/W | 0 | Page Enable 2<br>1: Enable 0: Disable |
| 3 | R/W | 0 | Page Enable 3<br>1: Enable 0: Disable |
| 4-6 | R/W | 0 | EMS Pages Starting Address<br>0 (000): C000:0000<br>1 (001): C400:0000<br>2 (010): C800:0000<br>3 (011): CC00:0000<br>4 (100): D000:0000<br>This starting address specifies the address of EMS page 0. EMS page 1 to 3 follow consecutively in 16K increments. |
| 7 | R/W | 0 | Global EMS Enable<br>1: Enable 0: Disable<br>If the Global EMS Enable is off (0), all EMS pages are disabled regardless of their individual enable bit. |

## EMS PAGE REGISTERS 0-3 (INDEX: 20H-23H)

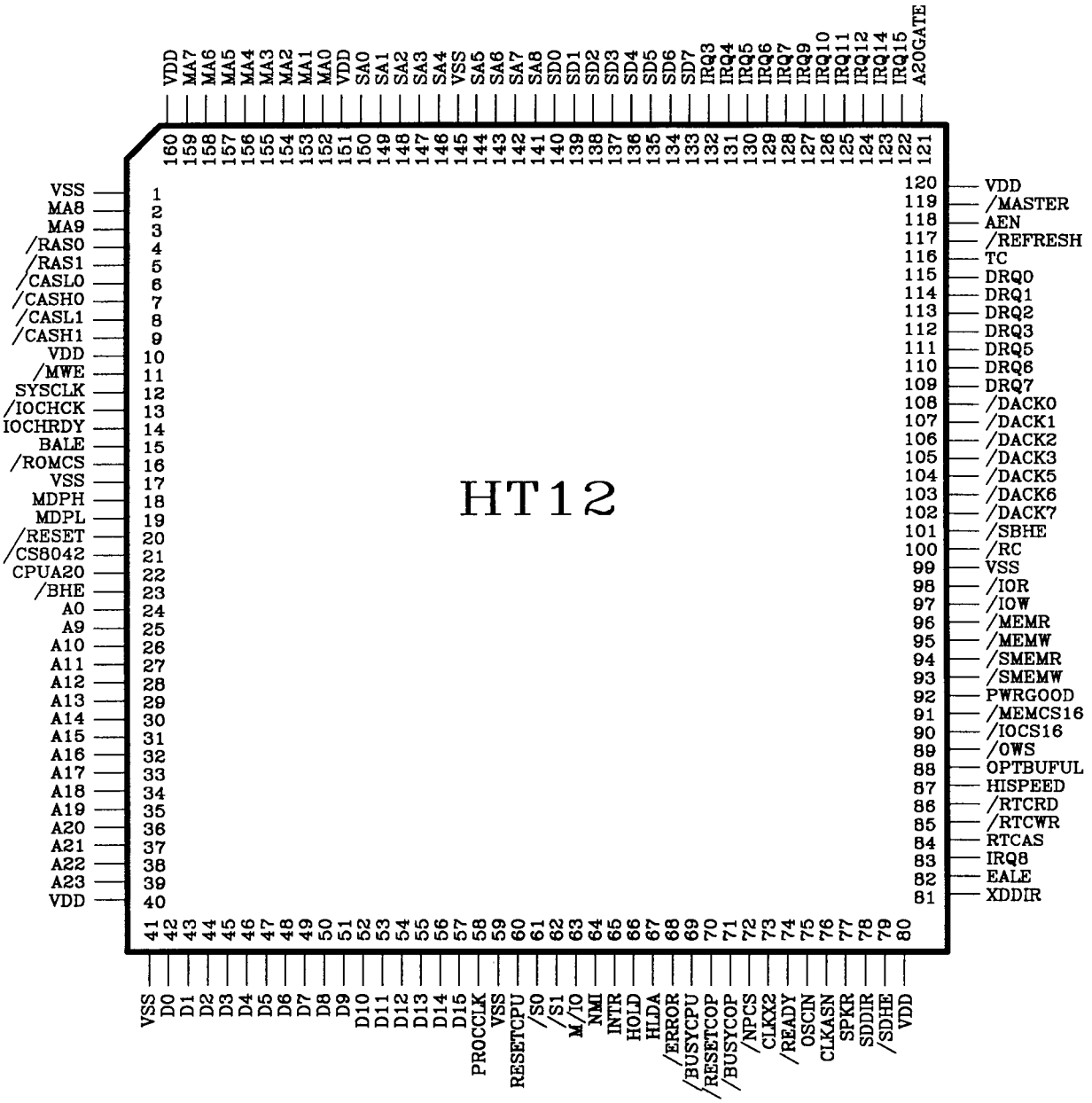
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | PA 21 | PA 20 | PA 19 | PA 18 | PA 17 | PA 16 | PA 15 | PA 14 |

| Bits | Access | Default | Description |
|---|---|---|---|
| 0-7 | R/W | | Translated EMS address lines |

## PORT 92H (HOT RESET AND GATE A20)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | 0 | 0 | 0 | 0 | 0 | 0 | GATE A20 | HOT RESET |

| Bits | Access | Default | Description |
|---|---|---|---|
| 0 | R/W | 0 | Hot Reset<br>This function provides an alternate means to reset the CPU. When this bit is set high, it triggers an alternate reset pulse to the reset logic. The reset occurs after a minimum of 6.72us and the entire reset operation takes 13.4us. When the reset bit is set to 1, it remains set until cleared by the BIOS.<br>1: Reset<br>0: Clear reset |
| 1 | R/W | 0 | Gate A20<br>1: A20 active<br>0: A20 inactive |
| 2-7 | R | 0 | Reserved |


HT12
1 VSS
2 MA8
3 MA9
4 /RAS0
5 /RAS1
6 /CASL0
7 /CASH0
8 /CASL1
9 /CASH1
10 VDD
11 /MWE
12 SYSCLK
13 /IOCHCK
14 IOCHRDY
15 BALE
16 /ROMCS
17 VSS
18 MDPH
19 MDPL
20 /RESET
21 /CS8042
22 CPUA20
23 /BHE
24 A0
25 A9
26 A10
27 A11
28 A12
29 A13
30 A14
31 A15
32 A16
33 A17
34 A18
35 A19
36 A20
37 A21
38 A22
39 A23
40 VDD
41 VSS
42 D0
43 D1
44 D2
45 D3
46 D4
47 D5
48 D6
49 D7
50 D8
51 D9
52 D10
53 D11
54 D12
55 D13
56 D14
57 D15
58 PROCCLK
59 VSS
60 RESETCPU
61 /S0
62 /S1
63 M/IO
64 NMI
65 INTR
66 HOLD
67 HLDA
68 /ERROR
69 /BUSYCPU
70 /RESETCOP
71 /BUSYCOP
72 /NPCS
73 CLKX2
74 /READY
75 OSCIN
76 CLKASN
77 SPKR
78 SDDIR
79 /SDHE
80 VDD
81 XDDIR
82 EALE
83 IRQ8
84 RTCAS
85 /RTCWR
86 /RTCRD
87 HISPEED
88 OPTBUFUL
89 /OWS
90 /IOCS16
91 /MEMCS16
92 PWRGOOD
93 /SMEMW
94 /SMEMR
95 /MEMW
96 /MEMR
97 /IOW
98 /IOR
99 VSS
100 /RC
101 /SBHE
102 /DACK7
103 /DACK6
104 /DACK5
105 /DACK3
106 /DACK2
107 /DACK1
108 /DACK0
109 DRQ7
110 DRQ6
111 DRQ5
112 DRQ3
113 DRQ2
114 DRQ1
115 DRQ0
116 TC
117 /REFRESH
118 AEN
119 /MASTER
120 VDD
121 A20GATE
122 IRQ15
123 IRQ14
124 IRQ12
125 IRQ11
126 IRQ10
127 IRQ9
128 IRQ7
129 IRQ6
130 IRQ5
131 IRQ4
132 IRQ3
133 SD7
134 SD6
135 SD5
136 SD4
137 SD3
138 SD2
139 SD1
140 SD0
141 SA8
142 SA7
143 SA6
144 SA5
145 VSS
146 SA4
147 SA3
148 SA2
149 SA1
150 SA0
151 VDD
152 MA0
153 MA1
154 MA2
155 MA3
156 MA4
157 MA5
158 MA6
159 MA7
160 VDD

| Pin Symbol | Pin Numbers | Pin Type | Pull Up/Dn* | Description |
|---|---|---|---|---|
| A0 | 24 | I | PU | Address line 0: Address input from CPU. |
| A9-23 | 25-39 | I/O | | Address lines: These are bi-directional address lines that input from the CPU and the I/O slot and output from the DMA controllers and the memory mapper. |
| A20GATE | 121 | I | | Gates address from 80286: If CPUHLDA=0, the 80286 CPU is driving the address bus. When A20GATE is high, the upper address bit (CPUA20 input) drives the A20 pin directly, when low the A20 output is forced low regardless of the state of CPUA20. |
| AEN | 118 | O | | Address Enable: This signal is used to disconnect the microprocessor and other devices from the I/O channel to allow DMA transfers to take place. When AEN is high, the DMA controller drives the address bus, data buses, and read/write command lines for both memory and I/O. |
| BALE | 15 | O | | Buffered Address Latch Enable: This signal is provided by the 82288 bus controller and is used to latch valid addresses and memory decodes from the microprocessor. It is used by the I/O channel as an indicator of a valid microprocessor or DMA address (when used with AEN). BALE is forced high during DMA cycles. |
| /BHE | 23 | I | PU | Byte High Enable: A low level enables the high byte D15-8 of the data bus. |
| /BUSYCOP | 71 | I | PU | Connect /BUSY out of the 80287 to this /BUSYCOP input. When the math co-processor is working it drives this input pin low, which in turn forces the /BUSYCPU output low and stops 80286 program execution on WAIT and some ESC instructions until /BUSYCPU becomes inactive (high). |

* Indicates Internal Resistor

| Pin Symbol | Pin Numbers | Pin Type | Pull Up/Dn* | Description |
|---|---|---|---|---|
| /BUSYCPU | 69 | O | | Connect /BUSYCPU output to the /Busy input of the 80286 CPU. A low level on this pin indicates the math co-processor (80287) is executing a command. Interrupts are honored by the 80286 while this input is low. /BUSY latched by /ERROR. (See /Error) |
| /CASH0, /CASH1 | 7,9 | O | | Column Address Strobe High order byte: These control 2 banks of DRAMS. |
| /CASL0, /CASL1 | 6,8 | O | | Column Address Strobe Low order byte: These control 2 banks of DRAMS. |
| CLKASN | 76 | I | PU | Asyncronous AT Bus clock source. The input frequency should be four times the required bus frequency. |
| CLKX2 | 73 | I | PU | CLKX2: Drive this clock input at twice the desired processor clock (PROCCLK) frequency. |
| CPUA20 | 22 | I | PU | Address 20 from the 80286. This input drives the A20 output pin, if CPUHLDA=0 and A20GATE=1. |
| /CS8042 | 21 | O | | Chip Select 8042: is used to drive the /CS input of the 8042 keyboard controller.This signal is low when the address decode is in the range of 60-6F (hex). used to drive the /CS input of the 8042 keyboard controller. |
| D(0-15) | 42-57 | I/O | PU | Bi-directional Data Bus: Data to/from the 80286. |
| /DACK (0-3,5-7) | 108-105 104-102 | I/O | PU | DMA ACKnowledge: These are active low signals used to acknowledge DMA requests (DRQ0-3 5-7) from peripherals on the I/O expansion slots. These pins are also read as configuration pins on power up. |

* Indicates Internal Resistor

| Pin Symbol | Pin Numbers | Pin Type | Pull Up/Dn* | Description |
|---|---|---|---|---|
| DRQ (0-3,5-7) | 115-112 111-109 | I | PD | These asynchronous channel requests are used by peripheral devices and the I/O channel microprocessors to gain DMA service, or control of the system. They are prioritized with DRQ0 having the highest priority and DRQ7 having the lowest. Each signal should be held high until the corresponding DMA Request Acknowledge (/DACK) signal goes active (low). DRQ0-3 govern 8 bit DMA transfers, DRQ5-7 govern 16-bit transfers. |
| EALE | 82 | O | | Early Address Latch Enable latches SA1-19. |
| /ERROR | 68 | I | PU | /ERROR: Connect /ERROR from the 80287 to this input. A low level indicates the math co-processor has an unmasked error condition. The HT12 responds by latching /BUSY and setting IRQ13. |
| HISPEED | 87 | I | PU | HIgh SPEED: When high, PROCCLK (the processor clock) speed is equal to CLKX2 . When low, PROCCLK is equal to half of CLKASN. |
| HLDA | 67 | I | PD | HoLD Acknowledge: The 80286 drives this high, when it relinquishes control of the system. This forces the A20 output tristate.<br><br>With CPUHLDA low, a low on A20GATE forces A20 low. A high on A20GATE passes CPUA20 through to pin A20. |
| HOLD | 66 | O | | CPU Hold to 80286. |
| INTR | 65 | O | | INTerrupt Request: Interrupt request signals from the HT12 to the 80286. A high on this output requests an interrupt from the 80286 CPU. |

* Indicates Internal Resistor

| Pin Symbol | Pin Numbers | Pin Type | Pull Up/Dn* | Description |
|---|---|---|---|---|
| /IOCHCK | 13 | I | PU | I/O CHannel CheckK: A low on this input indicates that there is an uncorrectable system error. It provides the system board with parity (error) information about memory or devices on the I/O channel. This causes the NMI (Non-Maskable Interrupt) output to become active (high), and interrupts the 80286 CPU. |
| IOCHRDY | 14 | I | PU | I/O CHannel ReaDY: Held low by the I/O or memory devices to lengthen the cycles. Any slow device using this line should drive it low immediately upon detecting its valid address and a Read/Write command. This signal should not be held low for more than 2.5 microseconds, or memory data may be lost due to inadequate refresh. |
| /IOCS16 | 90 | I | PU | I/O Chip Select 16: A low indicates a 16-bit, 1 wait state I/O cycle, data transfer on the I/O bus. This signal should be driven by an open collector or tri-state driver capable of sinking 20mA. |
| /IOR | 98 | I/O | PU | I/O Read: When low, instructs an I/O device to drive its data onto the data bus. It is driven by the microprocessor or DMA controller, either resident in the system or on the I/O channel. |
| /IOW | 97 | I/O | PU | I/O Write: When low, instructs an I/O device to read the data on the data bus. It may be driven by any microprocessor or DMA controller in the system or on the I/O channel. |
| IRQ(3-7, 9-12,14,15) | 132-128 127-124 123,122 | I | PU | Interrupt ReQuest: These pins signal the microprocessor that an I/O device needs attention. An interrupt request is generated when an IRQ line is raised from low to high. The line must be held high until the microprocessor acknowledges the interrupt request (Interrupt Service routine.) IRQ3 has the highest priority interrupt, IRQ15 the lowest. |
| /IRQ8 | 83 | I | PU | This input is driven by the Real Time Clock interrupt output. (Note that Interrupt Request 8 is active low unlike the other Interrupt Requests). |

* Indicates Internal Resistor

| Pin Symbol | Pin Numbers | Pin Type | Pull Up/Dn* | Description |
|---|---|---|---|---|
| MA(0-9) | 152-159,2,3 | O | | Memory Address bus: Address lines of the system RAM. |
| /MASTER | 119 | I | PU | /MASTER: This signal is used with a DRQ line to gain control of the system. A processor or DMA controller on the I/O channel issues a DRQ to a DMA channel in cascade mode and receives a /DACK. Upon receiving the /DACK, an I/O microprocessor pulls /MASTER input low, which will allow it to control the system address, data, and control lines ( a condition known as tri-state). After this signal is pulled low the I/O microprocessor must wait one system clock period before driving the address and data lines and two clock periods before issuing a Read/Write command. If this signal is held low for more than 15 microseconds, the system memory may be lost because of a lack of refresh. |
| MDPL<br>MDPH | 19,18 | I/O | PU | Memory Data Parity: Low (0) and high (1) bytes: When data is written to RAM or read from RAM its parity value is calculated. |
| /MEMCS16 | 91 | I | PU | MEMory Chip Select 16: A low signals the system board that the present data transfer is a 1 wait-state, 16 bit, memory cycle. This signal should be driven by open collector or tri-state driver capable of sinking 20mA. |
| /MEMR | 96 | I/O | PU | MEMory Read: Output is low during a memory read cycle. This signal instructs the memory devices to drive data onto the data bus. It can be driven by any microprocessor or DMA controller in the system. When a microprocessor on the I/O channel drives this signal it must have the address lines valid on the bus for 1 system clock period before driving /MEMR active. Not active during local memory cycles. |

*Indicates Internal Resistor

| Pin Symbol | Pin Numbers | Pin Type | Pull Up/Dn* | Description |
|---|---|---|---|---|
| /MEMW | 95 | I/O | PU | MEMory Write: Output is low during a memory write. This signal instructs the memory devices to store the data present on the data bus. It is active during all memory read cycles and can be driven by any microprocessor or DMA controller in the system. When driven by a microprocessor on the I/O channel the address lines on the bus must be valid for one system clock period before driving the signal active. This is tri-stated when /MASTER is low. Not active during local memory cycles. |
| M/IO | 63 | I | PU | Memory I/O from the 80286: If high during status cycle (TS), a memory cycle is in progress; if low, an I/O cycle is occuring. Tri-state when the 80286 is in Hold Acknowledge. (See HLDA) |
| /MWE | 11 | O | | Memory Write Enable to the DRAM |
| NMI | 64 | O | | Non-Maskable Interrupt: A high level forces the 80286 CPU to unconditionally execute an interrupt routine. |
| /NPCS | 72 | O | | Numeric Processor Chip Select: A low signal enables the math co-processor chip. This pin is connected to /NPS1 of the 80287. |
| OPTBUFUL | 88 | I | PD | OutPut BUffer Full: Input from P24 of the keyboard controller. Setting this pin high activates the internal IRQ1. This causes an INTR to the 80286 CPU indicating the keyboard buffer is full. |
| OSCIN | 75 | I | PU | 14.318 MHz input. |
| PROCCLK | 58 | O | | PROCessor CLocK: this output supplies the clock signal for the 80286 and 80287 chips. It drives CLK on the 80286, and CLK286 on the 80287 math processor. Rate determined by HISPEED. |

*Indicates Internal Resistor

| Pin Symbol | Pin Numbers | Pin Type | Pull Up/Dn* | Description |
|---|---|---|---|---|
| PWRGOOD | 92 | I | PU | PoWeRGOOD: When low, it resets the entire system. A Schmitt Trigger buffers the input pin. |
| /RAS0, /RAS1 | 4,5 | O | | Row Address Strobe: Selects RAM bank 0 or 1 RAS controls. |
| /RC | 100 | I | PU | Reset CPU: When driven low by the keyboard controller (P20), the 80286 CPU is reset. |
| /READY | 74 | O | | /READY: A low level tells the 80286 CPU that the current bus cycle is near completion. |
| /REFRESH | 117 | I/O | PU | /REFRESH: indicates that the current cycle is a memory refresh cycle. /REFRESH is an open drain output and can be driven by a microprocessor or another bus master on the I/O channel. |
| /RESET | 20 | O | | /RESET: an active low output used to reset the system logic at power-up or low-line voltage. |
| RESETCOP | 70 | O | | RESET CO-Processor: A low-to-high transition resets the 80287 co-processor. This should be held high for 4 system 80287 clocks (PROCCLK). |
| RESETCPU | 60 | O | | RESET CPU: A low-to-high transition resets the 80286 CPU during powerup, keyboard reset, and shut down. The rising edge resets the CPU, if the pin is held high for 16 clock cycles. |
| /ROMCS | 16 | O | | ROM Chip Select |
| RTCAS | 84 | O | | Real Time Clock Address Strobe: When low, this latches the RAM address for read/write operations. Connect to AS on RTC. |

* Indicates Internal Resistor

| Pin Symbol | Pin Numbers | Pin Type | Pull Up/Dn* | Description |
|---|---|---|---|---|
| /RTCRD | 86 | O | | Real Time Clock ReaD: When low data is read from the RTC. Connect to /DS pin of RTC. |
| /RTCWR | 85 | O | | Real Time Clock WRite: When low data is written to the RTC. Connect to R/W pin of RTC. |
| /S0, /S1 | 61,62 | I | PU | CPU Status bits 0,1: These pins convey the current 80286 CPU status to the internal 82288 bus controller (mega function). When /S0, /S1, INTA, are low and M/IO is high a shutdown or halt of the 80286 occurs. If A1=1, the CPU halts. If A1=0 the system shuts down. |
| SA(0-8) | 150-146, 144-141 | I/O | PU | System Address bus: Bi-directional address bus for the expansion bus. They are gated on the system bus when BALE is high and are latched on the falling edge of BALE during DMA. These signals are generated by the microprocessor or DMA Controller. They also may be driven by other microprocessors or DMA controllers that reside on the I/O channel as bus masters. |
| /SBHE | 101 | I/O | PU | System Byte High Enable: A low allows high-byte data transfers on the data bus SD8-SD15. 16-bit devices use this signal to condition data bus buffers tied to SD8-SD15. This signal is the output of the /BHE latch. |
| SD(0-7) | 140-133 | I/O | PU | System Data bus: For data transfers between the expansion slots and the D bus. |
| SDDIR | 78 | O | | SD bus DIRection |
| /SDHE | 79 | O | | SD bus High ENable |

* Indicates Internal Resistor

| Pin Symbol | Pin Numbers | Pin Type | Pull Up/Dn* | Description |
|---|---|---|---|---|
| /SMEMR | 94 | O | | System MEMory Read: Low during memory reads in the low 1 MB of memory space. It instructs the memory device to drive data onto the data bus. Not active during local memory accesses or accesses above 1 MB. |
| /SMEMW | 93 | O | | System MEMory Write: Low during memory writes within the low 1 MB of memory space. It instructs the memory device to store the data present on the data bus. Not active during local memory accesses or accesses above 1 MB. |
| SPKR | 77 | O | | SPeaKeR: Output of the Timer 8254 Channel 2. This connects to a speaker, through a buffer. |
| SYSCLK | 12 | O | | SYStem CLocK: This provides a clock for devices on the expansion slot. SYSCLK is constant at one fourth the CLKASN frequency. |
| TC | 116 | I/O | PD | Terminal Count: TC pulses high when the DMA channel terminal count is reached. This signal is available on the expansion slot. Also used as power up configuration input pin. |
| XDDIR | 81 | O | | XD bus DIRection |

*Indicates Internal Resistor

| Pin Symbol | Pin Numbers | Pin Type | Pull Up/Dn* | Description |
|---|---|---|---|---|
| /0WS | 89 | I | PU | Zero Wait State: This signal tells the microprocessor that it can complete the present bus cycle without inserting additional wait cycles. It comes from an address decode gated with a Read/Write command. In order to run a memory cycle to an 8-bit device with a minimum of 2 wait states, 0WS must be driven low one system clock after Read or Write command is gated with the address decode for the device. These Read/Write commands are active on the falling edge of the system clock. This signal should be driven by an open collector or tri-state driver capable of sinking 20mA. Should be connected to external 300 Ohm pull up. |
| VDD | 10,40,80,120, 151,160 | | | Power: +5 Volts Supply |
| VSS | 1,17,41,59,99, 145 | | | Ground |

* Indicates Internal Resistor

To be added in the next revision of this document.

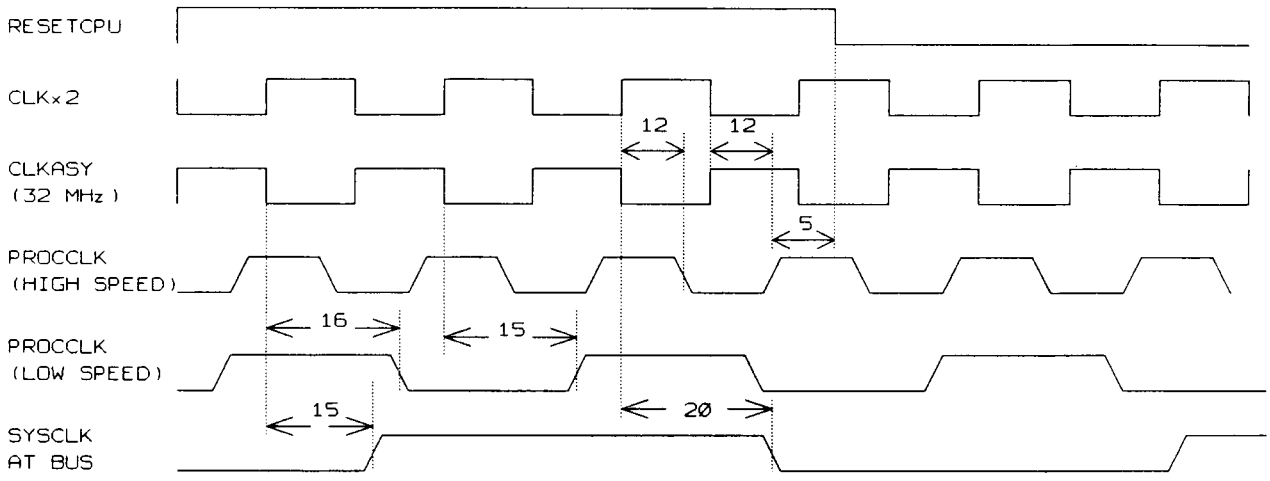
Preliminary Timing

Unspecified output pins have 65pF loading
Unspecified bi-directional pins have 100pF loading

| | | |
|---|---|---|
| D0-D15 | 100pF load; | TTL-level |
| MA0-MA9 | 250pF load; | TTL-level |
| /RAS0,/RAS1 | 150pF load; | TTL-level |
| /CASL0,/CASL1 | 100pF load; | TTL-level |
| /MWE | 300pF load; | TTL-level |
| PROCCLK | 50pF load; | TTL-level |
| /READY | 50pF load; | TTL-level |
| MDPH | 50pF load; | TTL-level |
| MDPL | 50pF load; | TTL-level |

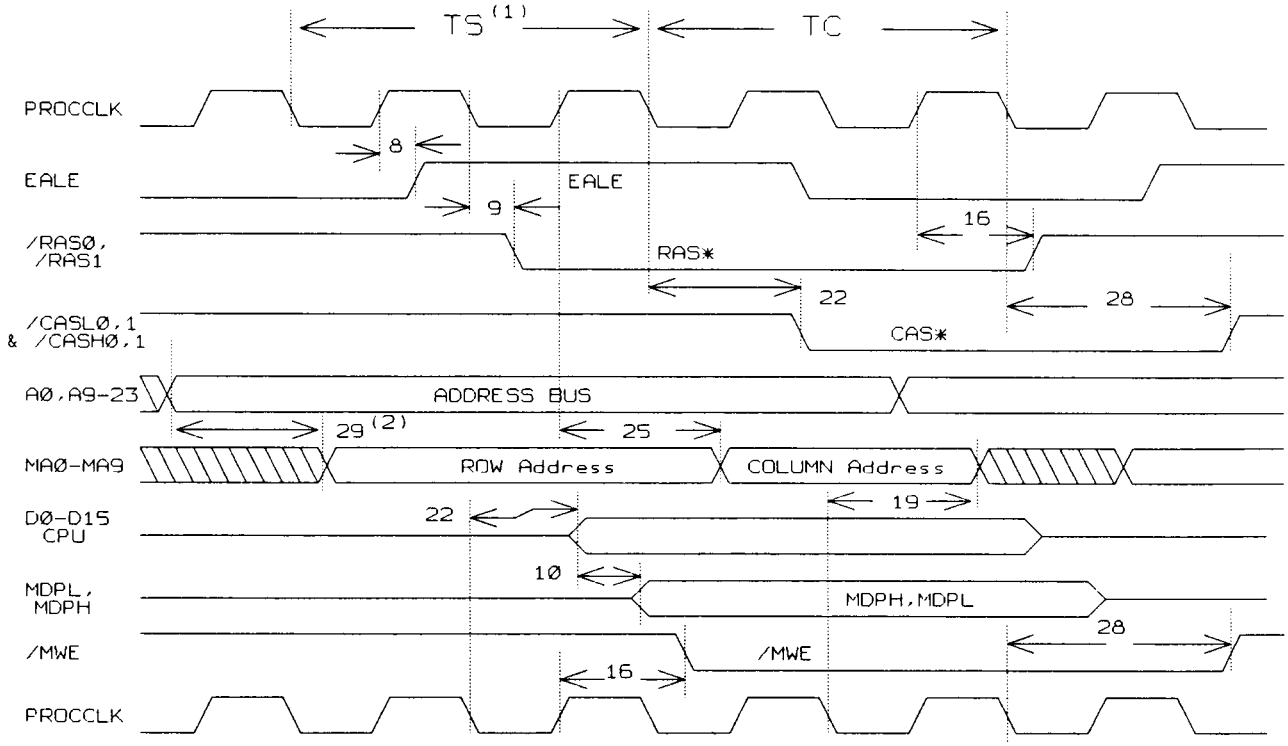
## CLOCK TIMING
## Figure 1

Max Timing



## ZERO WAIT STATE MEMORY CYCLE
**Figure 2A**

Max Timing



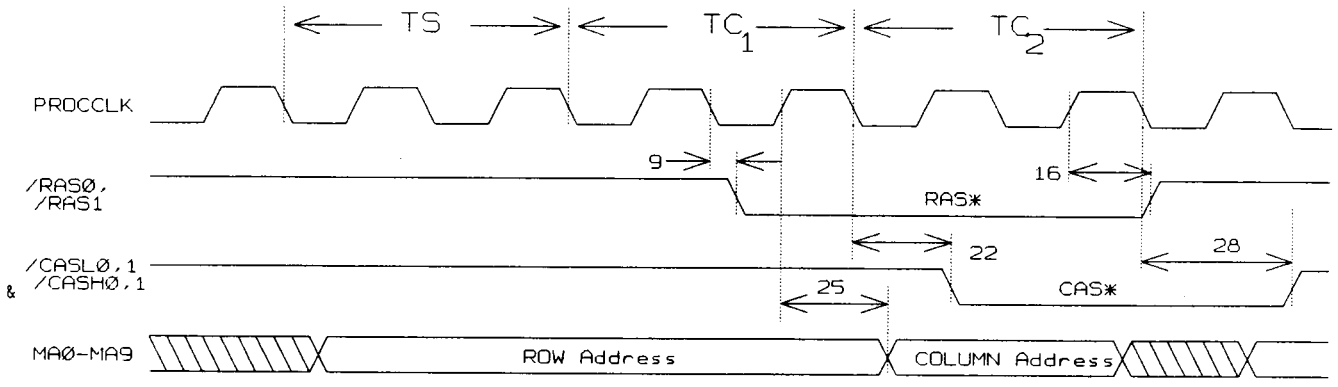

PROCCLK MUST HAVE A 50% DUTY CYCLE
Note: All DRAM timings that reference PROCCLK assume a 50pF load on PROCCLK.

NOTE1: TS = 80.0ns at 12.5 MHz
TS = 62.5ns at 16.0 MHz

Note 2: 29ns REGULAR or RELOCATED Cycles
35ns with EMS Cycles
37ns with EMS RELOCATED Cycles

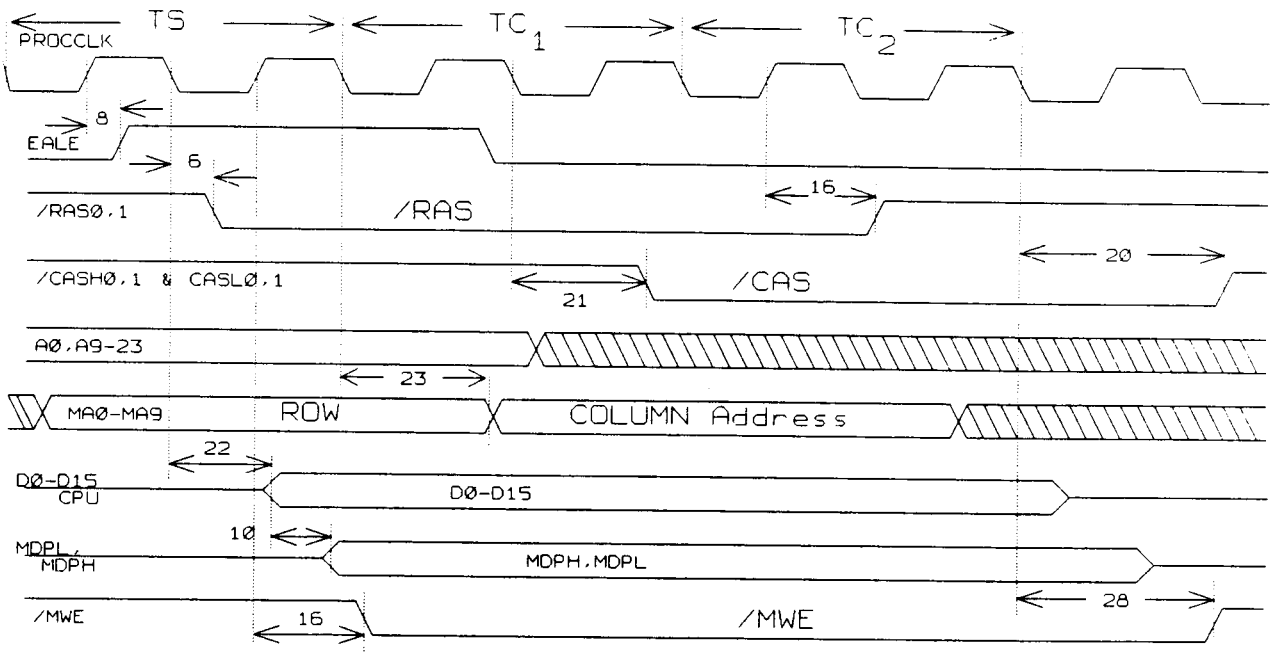
## ZERO WAIT-STATE MEMORY CYCLE WITH 1 EXTRA WAIT- STATE
**Figure 2B**

Max Timing



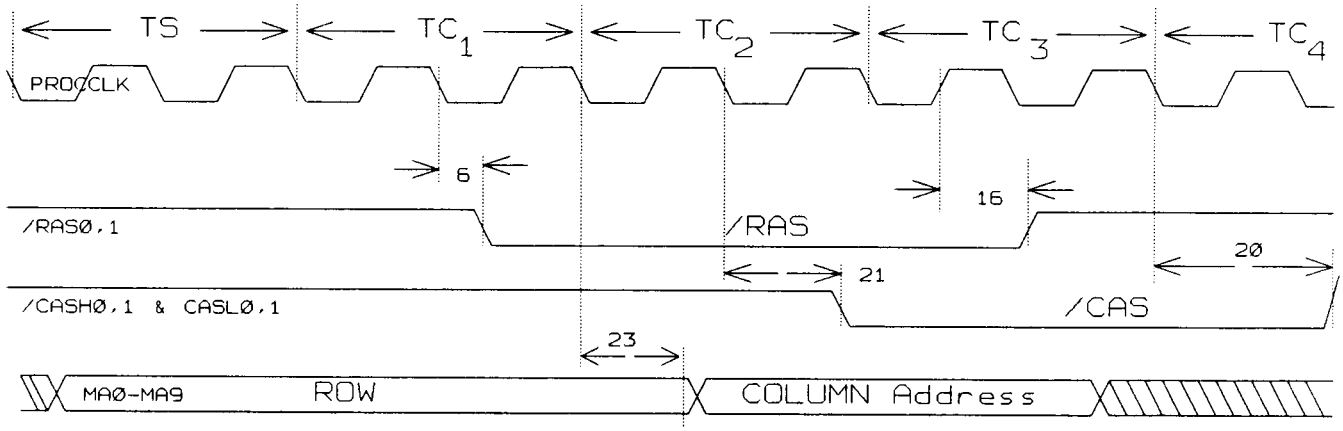
## ONE WAIT- STATE MEMORY CYCLE
**Figure 3A**

Max Timing



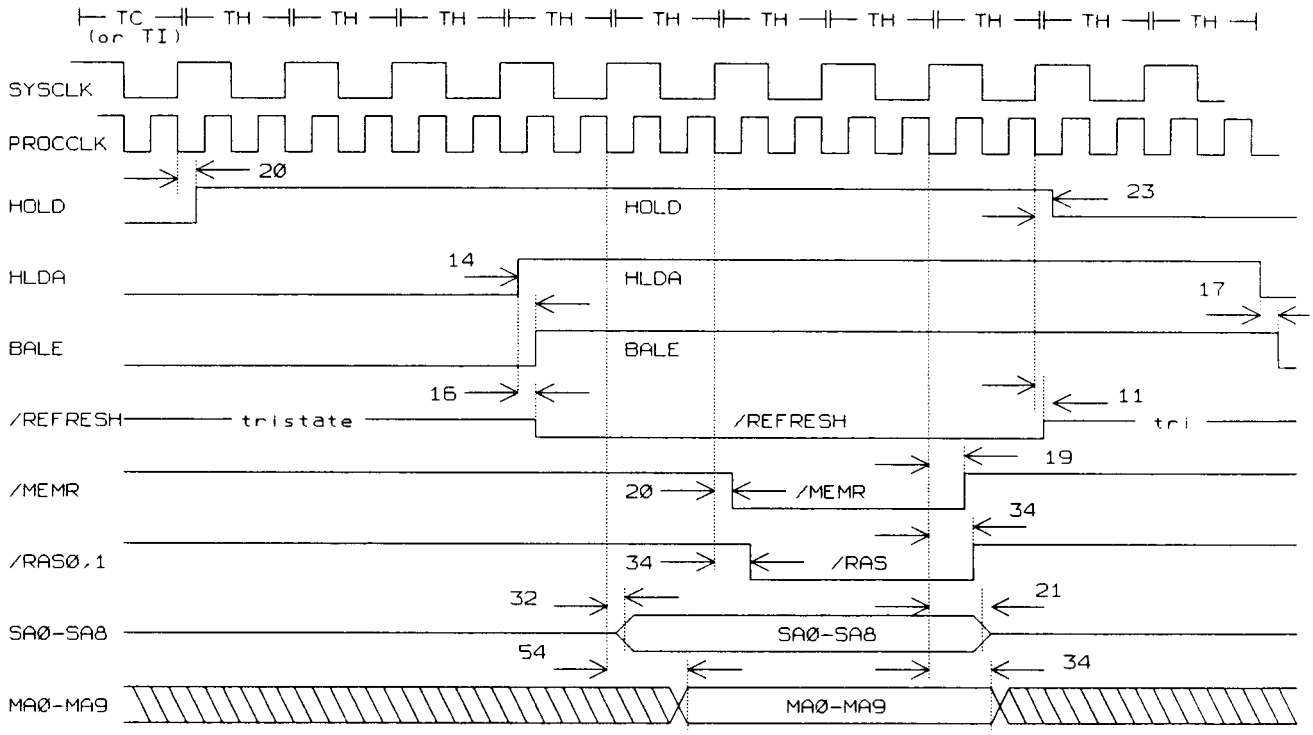
## ONE WAIT- STATE MEMORY CYCLE WITH 1 EXTRA WAIT- STATE
**Figure 3B**

Max Timing



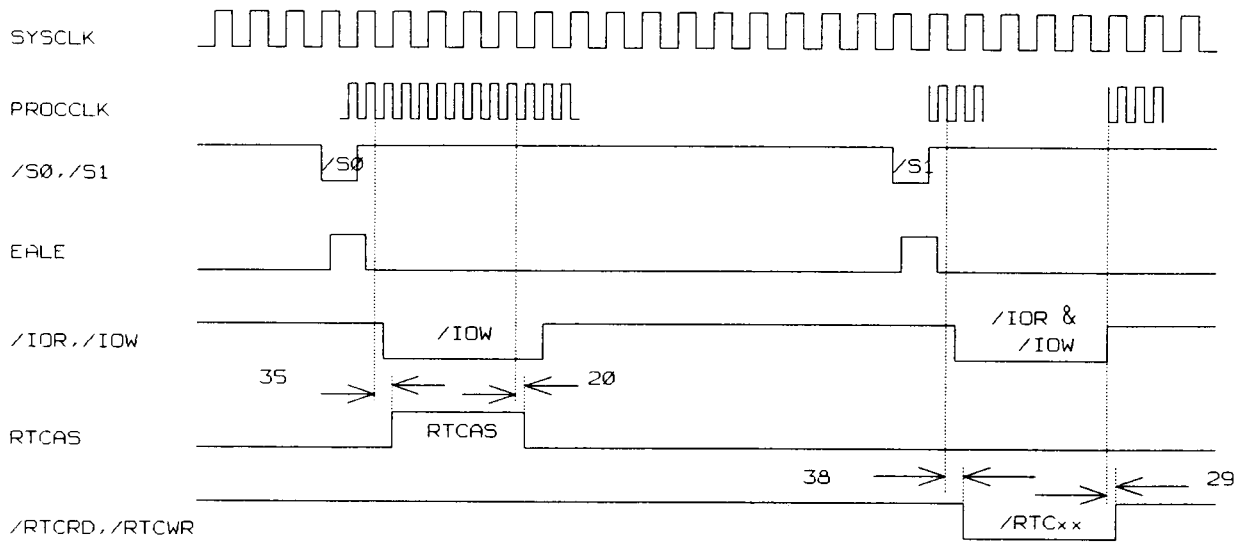
## REFRESH
## Figure 4

Max Timing



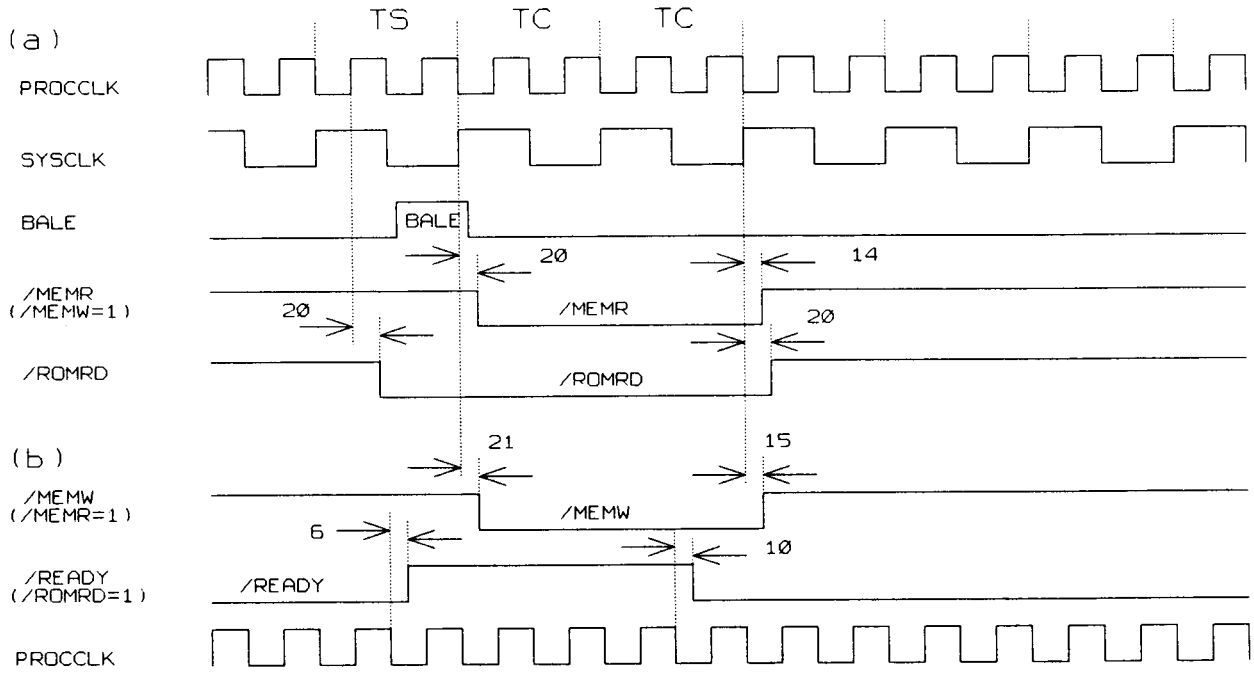
## REAL TIME CLOCK TIMING
**Figure 5**

Max Timing



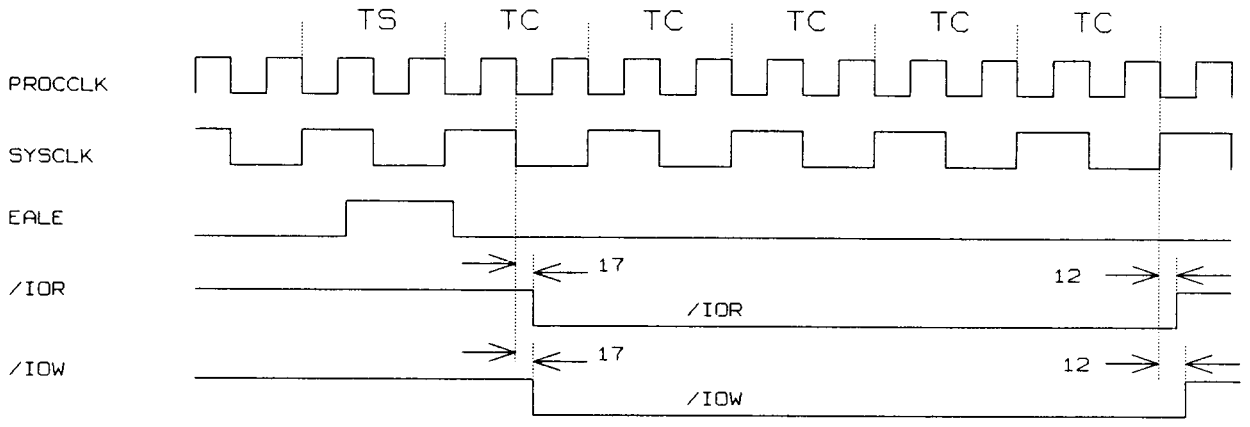
**a) ROM READ**
**b) 16-BIT MEMR TO 16-BIT DEVICES**
**Figure 6**

Max Timing



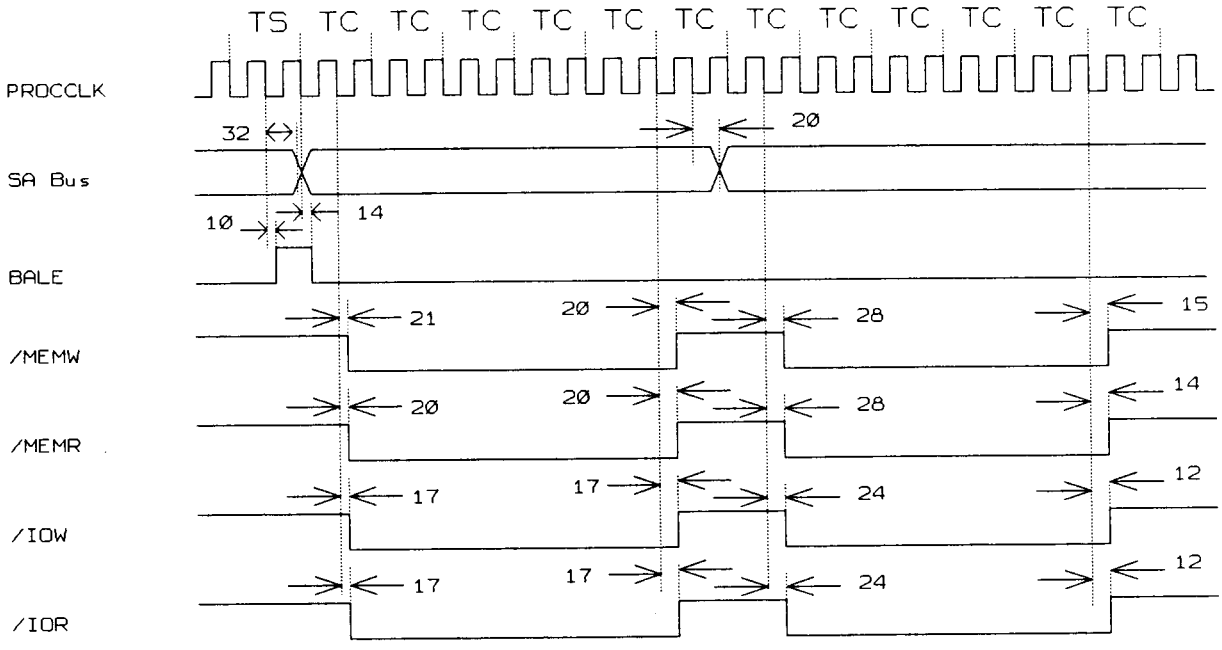
## 8-BIT /IOR AND /IOW
## Figure 7

Max Timing

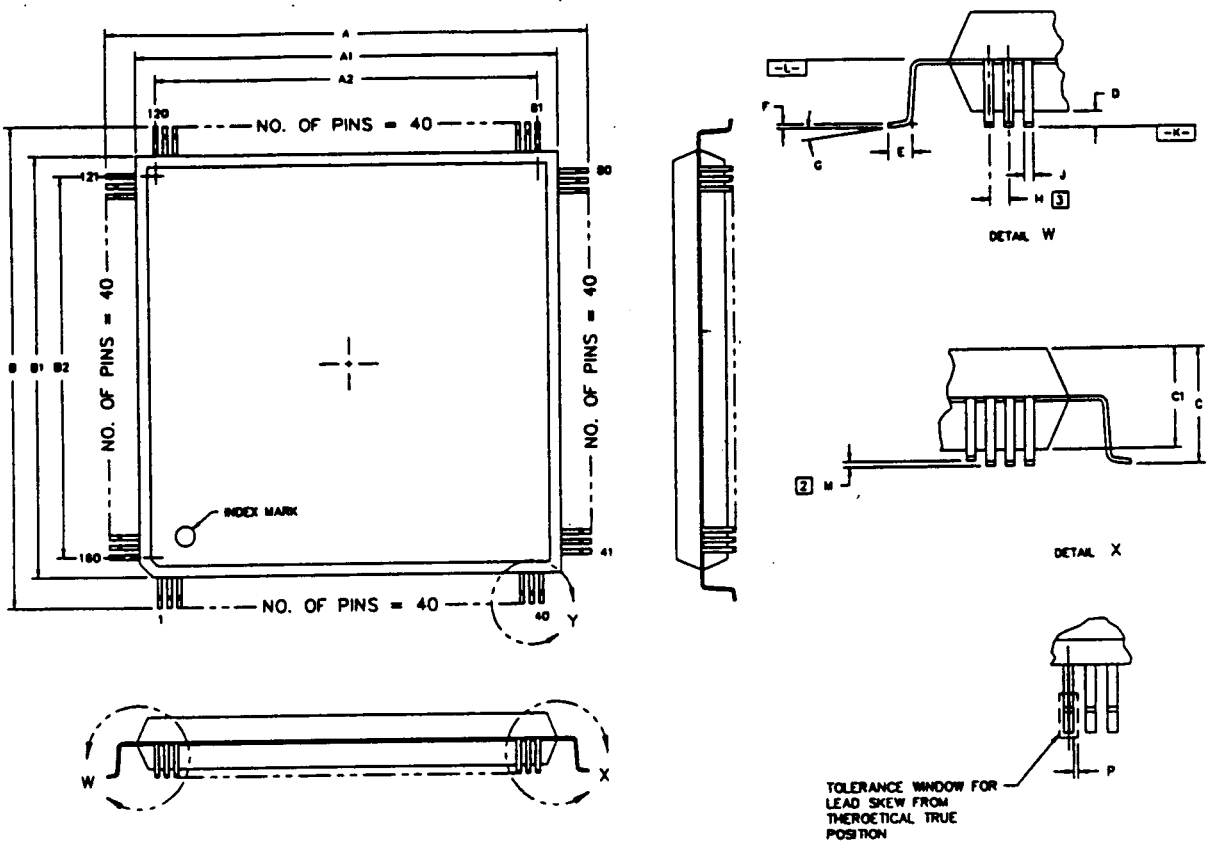


## 16-BIT /MEMR, /MEMW AND /IOR, /IOW TO 8-BIT DEVICES
**Figure 8**

Max Timing



# 160-Pin Flat Pack (Gull Wing)




NOTES: UNLESS OTHERWISE SPECIFIED

1. NOMINAL DIMENSIONS IN MILLIMETERS. INCHES ROUNDED TO THE NEAREST .001 INCH.
2. COPLANARITY OF ALL LEADS SHALL BE WITHIN 0.1 MM (0.004") (DIFFERENCE BETWEEN HIGHEST AND LOWEST LEAD WITH SEATING PLANE -K- AS REFERENCE)
3. LEAD PITCH DETERMINED AT DATUM -L-
4. CONTROLLING DIMENSIONS ARE IN MILLIMETERS.

[1]

| DIMENSIONS IN MM | | |
|---|---|---|
| SYM | MINIMUM | MAXIMUM |
| A | 31.60 | 32.40 |
| A1 | 27.90 | 28.10 |
| A2 | 25.35 REF | |
| B | 31.60 | 32.40 |
| B1 | 27.90 | 28.10 |
| B2 | 25.35 REF | |
| C | 3.68 | 4.01 |
| C1 | 3.43 | 3.66 |
| D | 0.25 | 0.38 |
| E | 0.80 | 1.00 |
| F | 0.10 | 0.25 |
| G | 0° | 10° |
| H | 0.65 ±0.15 | |
| J | 0.25 | 0.35 |
| M | 0.10 MAX | |
| P | 0.05 MAX | |
| TOTAL NO. OF PINS | 160 | |

[1]

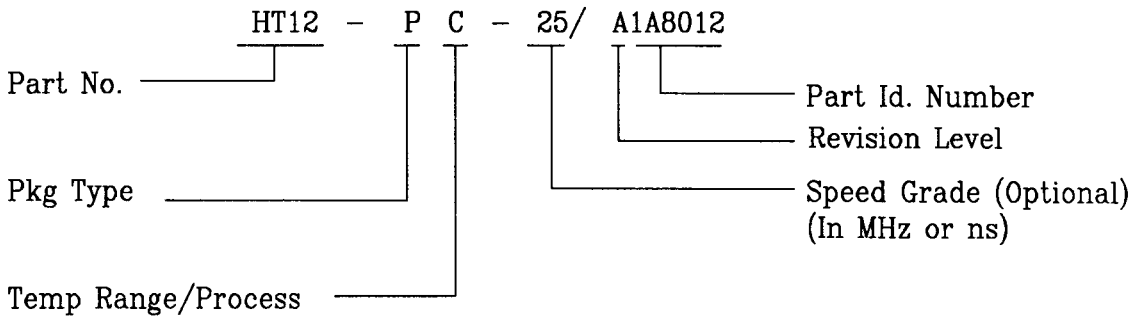
| DIMENSIONS IN INCHES | | |
|---|---|---|
| SYM | MINIMUM | MAXIMUM |
| A | 1.244 | 1.276 |
| A1 | 1.098 | 1.106 |
| A2 | 0.998 REF | |
| B | 1.244 | 1.276 |
| B1 | 1.098 | 1.106 |
| B2 | 0.998 REF | |
| C | 0.145 | 0.158 |
| C1 | 0.135 | 0.144 |
| D | 0.010 | 0.014 |
| E | 0.024 | 0.039 |
| F | 0.004 | 0.010 |
| G | 0° | 10° |
| H | 0.026 ±0.006 | |
| J | 0.010 | 0.014 |
| M | 0.004 MAX | |
| P | 0.002 MAX | |
| TOTAL NO. OF PINS | 160 | |

IMPORTANT NOTE:

If designing in inches, ALL pin positions should be calculated in millimeters (mm) then converted to inches. The inches listed have been rounded.

# Product Ordering Information & Part Marking

Order Code/Part Number Example




Temp Range/Process

C – Commercial temp range (0°C to 70°C)

Package Types

P – Plastic

IMPORTANT: Contact your local sales office for the current Order Code/Part Number

**TOKYO**
LSI LOGIC
Tama Plaza Daisen Bldg.
2-19-2, Utsukushiga-Oka,
Midori-Ku
Yokohama-city, Kanagawa-Pref
227 Japan
TEL: 81 45 902-4111
FAX: 81 45 902-4533

## SALES REPRESENTATIVES EUROPE

**FRANCE**
RTF
81, Rue Pierre-Semard
92320 Chatillon, France
TEL: 33-1-49-65-25-00
FAX: 33-1-49-65-25-39

REP'TRONIC, S.A
1 Bis, Rue Marcel Paul
Bat A
Z I De La Bonde
91300 Massy, France
TEL: 33-1-60-13-93-00
FAX: 33-1-60-13-91-98

**GERMANY**
ADVANCED ELECTRONICS
Stefan-George-Ring 19
8000 Munich 81
West Germany
TEL: 49-89-9300-9850
FAX: 49-89-9300-9866

ADVANCED ELECTRONICS
TheaterstraBe 14
3000 Hannover 1
West Germany
TEL: 49-511-368-1756
FAX: 49-511-368-1759

**ITALY**
COMPREL
Viale Fulvio Testi 115
20092 Cinisello
Balsamo (Milano)
Italy
TEL: 39 2 612 0641
FAX: 39 2 612 90526

**NETHERLANDS**
ARCOBEL
Griekenweg 25
5342 PX Oss, Netherlands
TEL: 31 4120 30335
FAX: 31 4120 30635

**NORWAY**
SEMI DEVICES
Asenveien 1
1400 Ski, Norway
TEL: 47-9-876-550
FAX: 47-9-876-577

**SWEDEN**
MARTINSSON ELEKTRONIK AB
Instrumentvagen 16
Box 9060
S-12609 Hagersten, Sweden
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