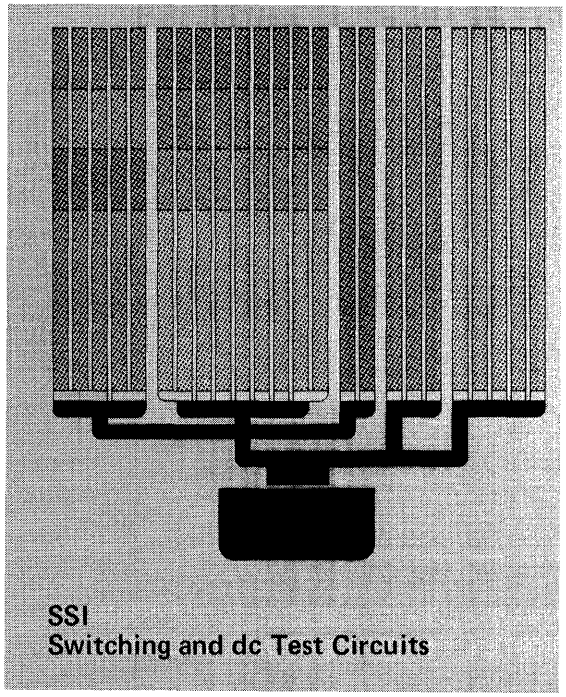
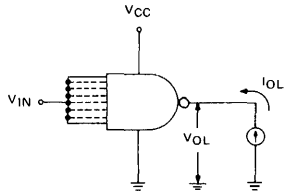


SSI
Switching and dc Test Circuits

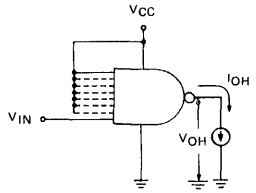
PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS*



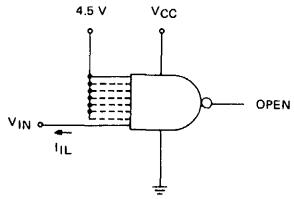
1. All inputs are tested simultaneously

Fig. 1



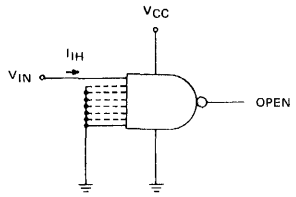
1. Each input is tested separately.

Fig. 2



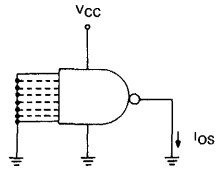
1. Each input is tested separately.

Fig. 3



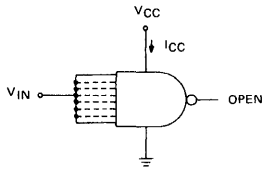
1. Each input is tested separately.

Fig. 4



1. Each gate is tested separately.

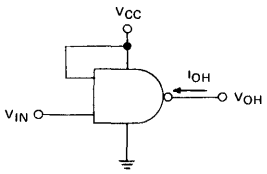
Fig. 5



1. LOW level and HIGH level conditions are tested.
2. All gates are tested simultaneously.
3. Average supply current per gate:

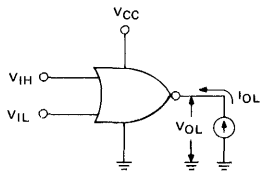
$$I_{CC(AVG)} = \frac{I_{CCH} + I_{CCL}}{2X \text{ No. of gates in package}}$$

Fig. 6



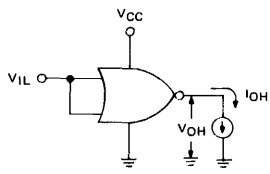
1. Each input is tested separately.

Fig. 7



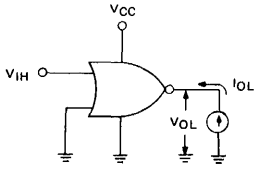
1. Each input is tested separately.

Fig. 8



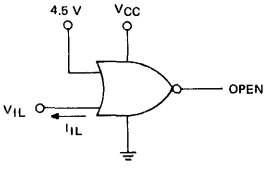
1. Both inputs are tested simultaneously.

Fig. 9



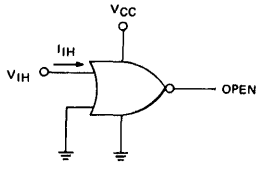
1. Each input is tested separately.

Fig. 10



1. Each input is tested separately.

Fig. 11



1. Each input is tested separately.

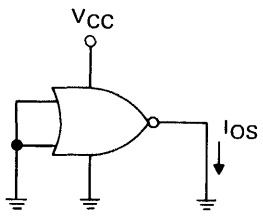
Fig. 12

*Arrows indicate actual direction of current flow.

6

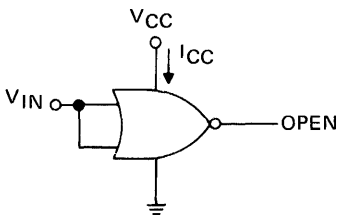
PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS* (Continued)



1. Each gate is tested separately.

Fig. 13



1. Low level and high level conditions are tested.
2. All gates are tested simultaneously.

Fig. 14

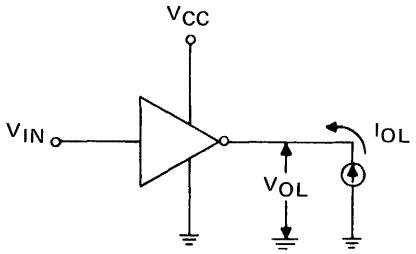


Fig. 15

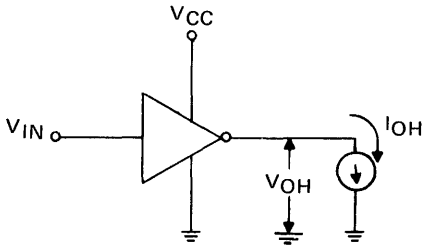


Fig. 16

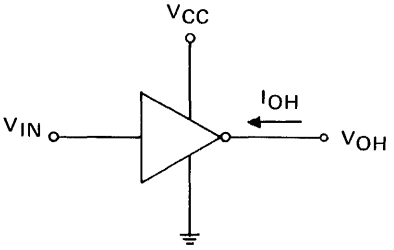


Fig. 17

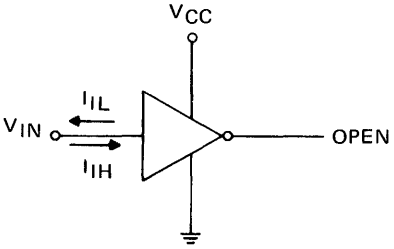
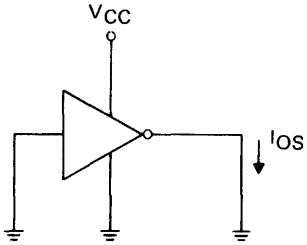
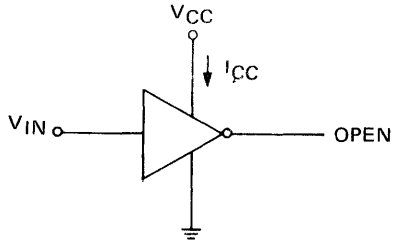


Fig. 18



1. Each inverter is tested separately.

Fig. 19



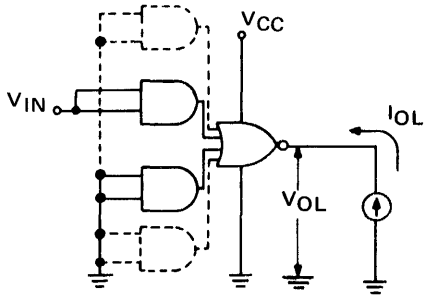
1. All inverters are tested simultaneously.

Fig. 20

*Arrows indicate actual direction of current flow.

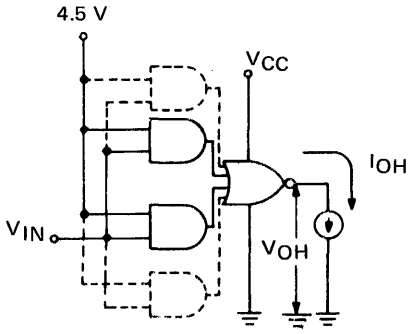
PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS* (Continued)



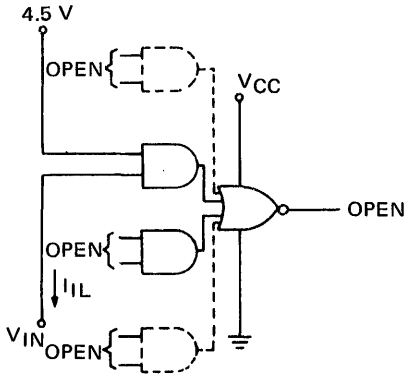
1. Each AND section is tested separately.

Fig. 21



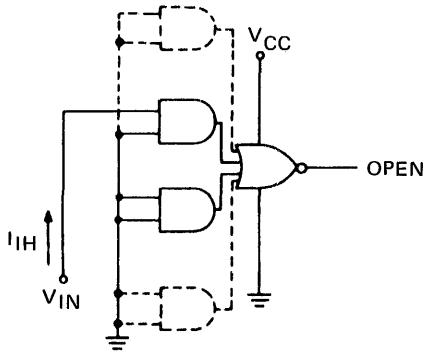
1. Each pair of inputs is tested separately.

Fig. 22



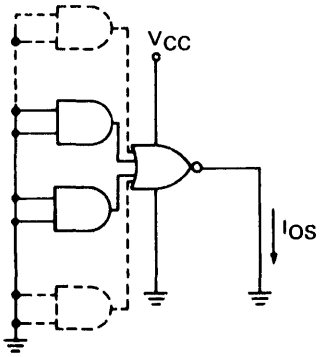
1. Each input is tested separately.

Fig. 23



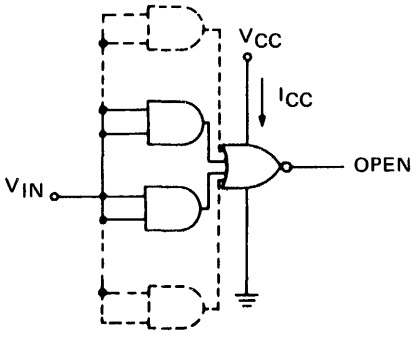
1. Each input is tested separately.

Fig. 24



1. Each gate is tested separately.

Fig. 25



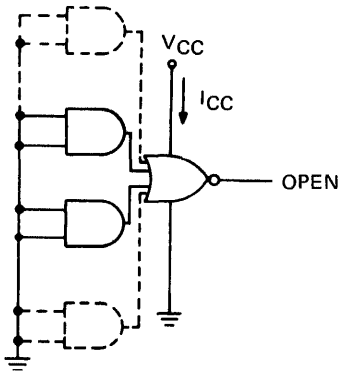
1. All gates are tested simultaneously.

Fig. 26

*Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS* (Continued)



1. All gates are tested simultaneously

Fig. 27

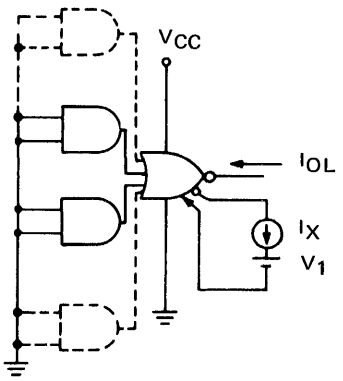


Fig. 28

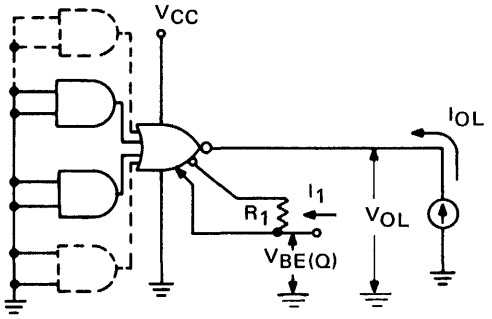


Fig. 29

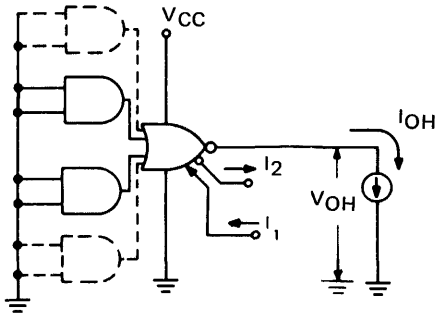
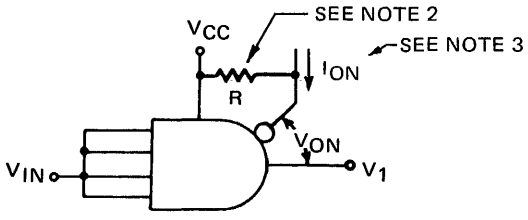
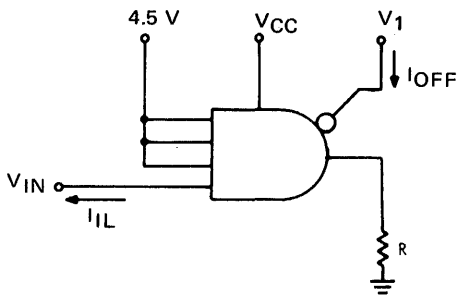


Fig. 30



1. All inputs are tested simultaneously.
2. Deleted on 9H60/5460, 7460
3. Deleted on 9N60/5460, 7460

Fig. 31



1. Each input is tested separately.

Fig. 32

*Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS* (Continued)

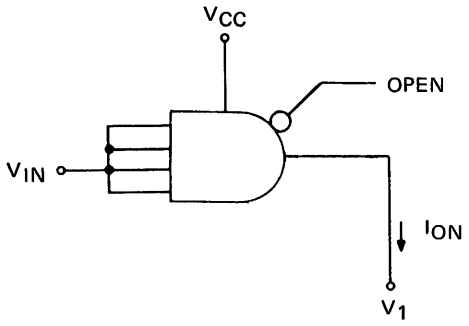
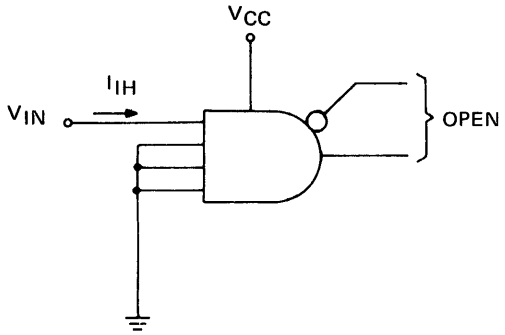
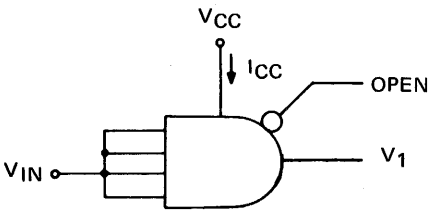


Fig. 33



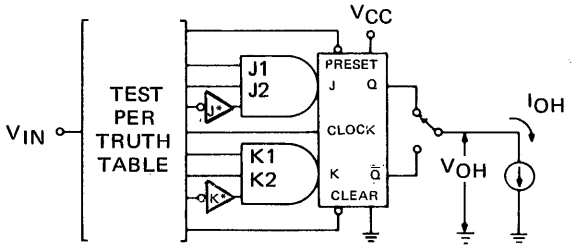
1. Each input is tested separately.

Fig. 34



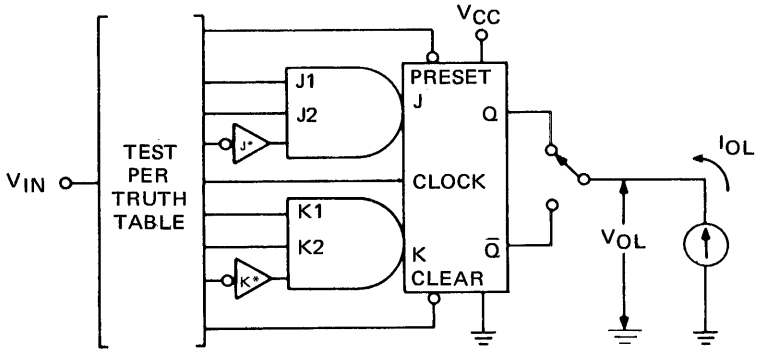
1. "On" and "off" conditions are tested separately.
2. All gates are tested simultaneously

Fig. 35



1. Each output is tested separately.
2. Preset and clear are tested with $V_{IN(clock)} = 0$.

Fig. 36



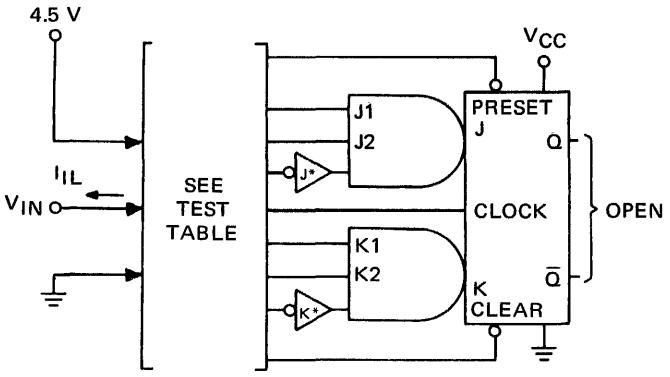
1. Each output is tested separately.

Fig. 37

*Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS* (Continued)

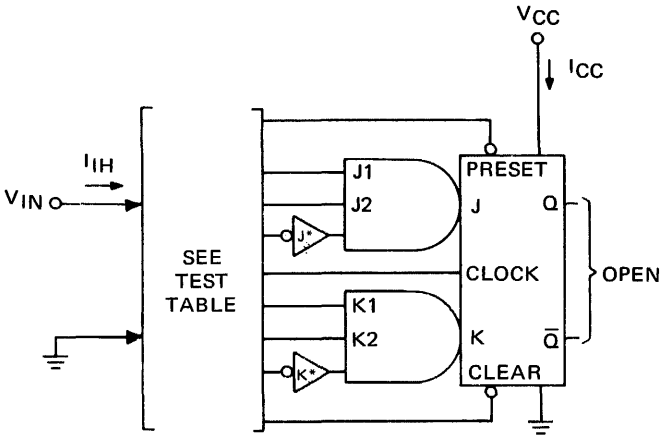


TEST TABLE

Apply V_{IN} (Test I_{IL})	Apply 4.5 V	Ground	Apply Momentary GND, then 4.5 V
J2	J1	J*	Clear
J1	J2	J*	Clear
J*	None	None	None
K2	K1	K*	Preset
K1	K2	K*	Preset
K*	None	None	None
Clock	None	None	None
Preset	K1 and K2	K*	None
Clear	J1 and J2	J*	None

1. Each output is tested separately.

Fig. 38

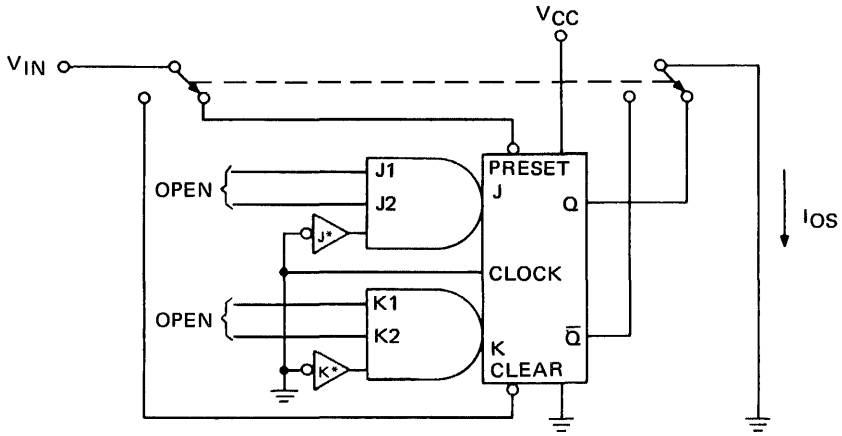


TEST TABLE

Apply V_{IN} (Test I_{IH})	Ground	Apply 4.5 V
J2	J1 and Clear	J*
J1	J2 and Clear	J*
J*	None	None
K2	K1 and Preset	K*
K1	K2 and Preset	K*
K*	None	None
Clock	None	None
Preset	K1 and K2	K*
Clear	J1 and J2	J*

1. Each input is tested separately.
2. I_{CC} is measured with clear at GND, then with preset at GND.

Fig. 39



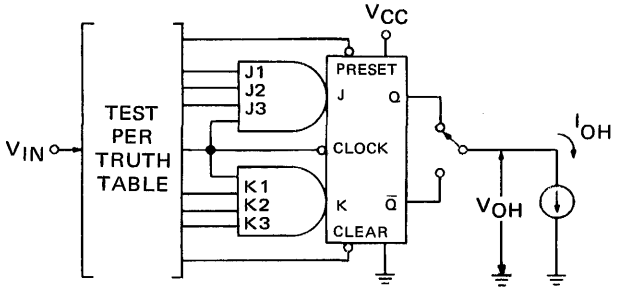
1. Each output is tested separately.

Fig. 40

*Arrows indicate actual direction of current flow.

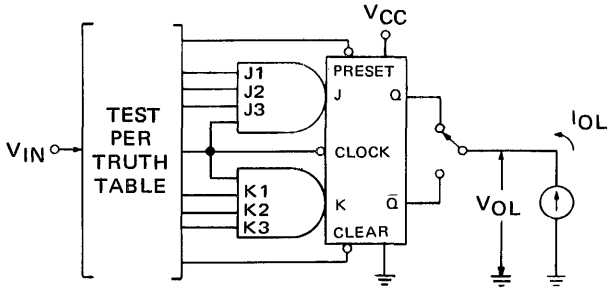
PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS* (Continued)



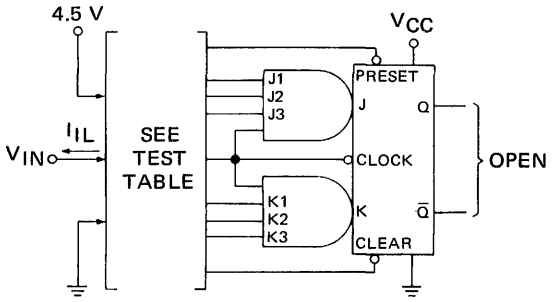
1. Each output is tested separately.

Fig. 41



1. Each output is tested separately.

Fig. 42



1. Each input is tested separately.

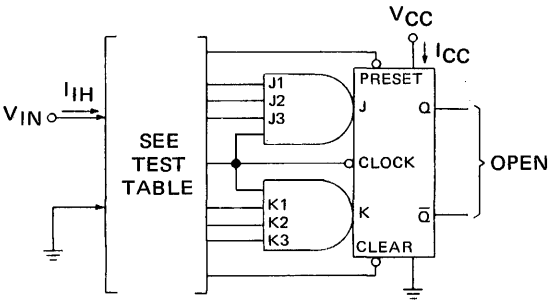
Fig. 43

TEST TABLE

Apply V_{IN} (Test I_{IL})	Apply Momentary GND, then 4.5 V	Apply 4.5 V
Clock	Preset	J1, J2, J3, K1, K2, and K3
Clock	Clear	J1, J2, J3, K1, K2, and K3
Preset	None	J1, J2, J3, K1, K2, and K3
Clear	None	J1, J2, J3, K1, K2, and K3
J1	Clear	Clock, J2, and J3
J2	Clear	Clock, J1, and J3
J3	Clear	Clock, J1, and J2
K1	Preset	Clock, K2, and K3
K2	Preset	Clock, K1, and K3
K3	Preset	Clock, K1, and K2

9H102/54H102, 74H102

Apply V_{IN} (Test I_{IL})	Apply 4.5 V	Ground
Clock	J1, J2, J3, K1, K2, K3, Clear	Preset
Clock	J1, J2, J3, K1, K2, K3, Preset	Clear
Preset	J1, J2, J3, K1, K2, K3, Clock, Clear	None
Clear	J1, J2, J3, K1, K2, K3, Clock, Preset	None
J1	J2, J3, K1, K2, K3, Clock, Preset	Clear
J2	J1, J3, K1, K2, K3, Clock, Preset	Clear
J3	J1, J3, K1, K2, K3, Clock, Preset	Clear
K1	J1, J2, J3, K2, K3, Clock, Clear	Preset
K2	J1, J2, J3, K1, K3, Clock, Clear	Preset
K3	J1, J2, J3, K1, K2, Clock, Clear	Preset



1. Each input is tested separately.
2. I_{CC} is measured with clear at GND, then with preset at GND.

Fig. 44

TEST TABLE

Apply V_{IN} (Test I_{IH})	Ground
Clock	Preset, Clear, J1, J2, J3, K1, K2, and K3
Preset	Clock, K1, K2, and K3
Clear	Clock, J1, J2, and J3
J1	Clock, Clear, J2, and J3
J2	Clock, Clear, J1, and J3
J3	Clock, Clear, J1, and J2
K1	Clock, Preset, K2, and K3
K2	Clock, Preset, K1, and K3
K3	Clock, Preset, K1, and K2

9H102/54H102, 74H102

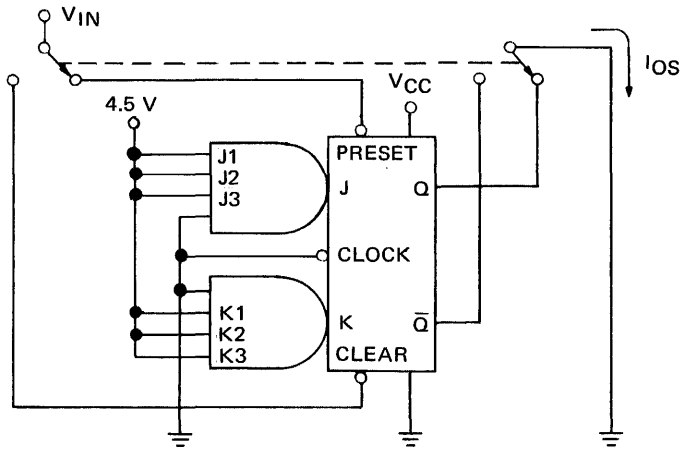
Apply V_{IN} (Test I_{IH})	Ground	4.5V
Clock	J1, J2, J3, K1, K2, K3, Preset	Clear
Clock	J1, J2, J3, K1, K2, K3, Clear	Preset
Preset†	J1, J2, J3, K1, K2, K3, $\bar{Q}$	Clock, Clear
Clear†	J1, J2, J3, K1, K2, K3, $\bar{Q}$	Clock, Preset
J1	J2, J3, Clock, Preset	K1, K2, K3, Clear
J2	J1, J3, Clock, Preset	K1, K2, K3, Clear
J3	J1, J2, Clock, Preset	K1, K2, K3, Clear
K1	K2, K3, Clock, Clear	J1, J2, J3, Preset
K2	K1, K3, Clock, Clear	J1, J2, J3, Preset
K3	K1, K2, Clock, Clear	J1, J2, J3, Preset

*Arrows indicate actual direction of current flow.

†Duration of this test should not exceed 1 second.

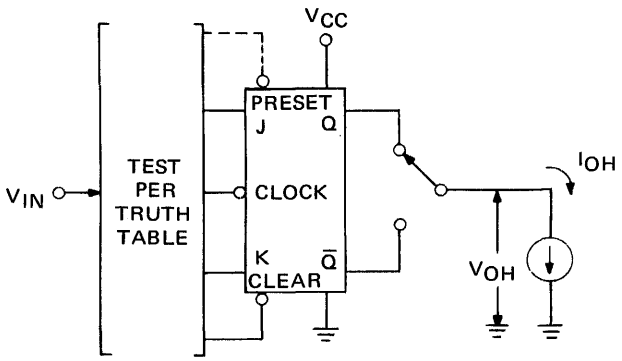
PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS* (Continued)



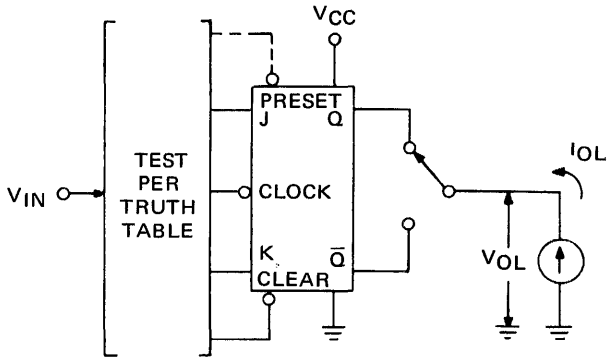
1. Each output is tested separately.

Fig. 45



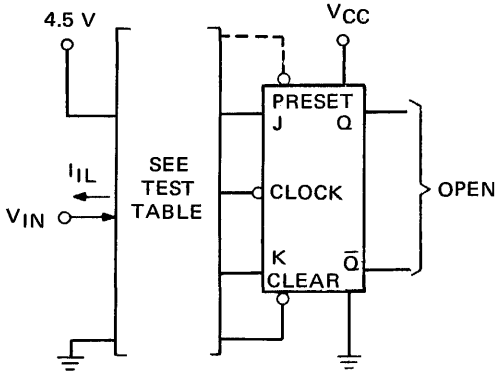
1. Each flip-flop is tested separately.
2. Each output is tested separately.
3. Preset is applicable for 9H78/54H78, 74H78 only.

Fig. 46



1. Each flip-flop is tested separately.
2. Each output is tested separately.
3. Preset is applicable for 9H78/54H78, 74H78 only.

Fig. 47



TEST TABLE

Apply V_{IN} (Test I_{IL})	Apply Momentary GND	Apply 4.5 V
Clock	Clear (See Note 2)	J and K
Clear	None	Clock and J
Preset	None (See Note 5)	Clock and K
J	Q (See Note 3)	Clock and Clear
K	$\bar{Q}$ (See Note 3)	Clock and Clear

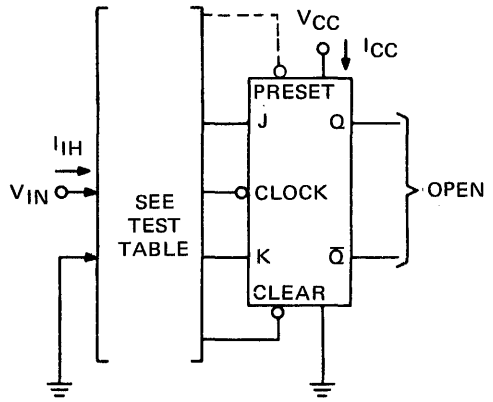
1. Each flip-flop is tested separately.
2. Apply momentary ground, then 4.5 V.
3. After application of momentary ground, Q and $\bar{Q}$ are left floating.
4. Ground all inputs of the unused flip-flop.
5. Preset is applicable for 9N76/5476, 7476 circuits only.

Fig. 48

*Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS* (Continued)

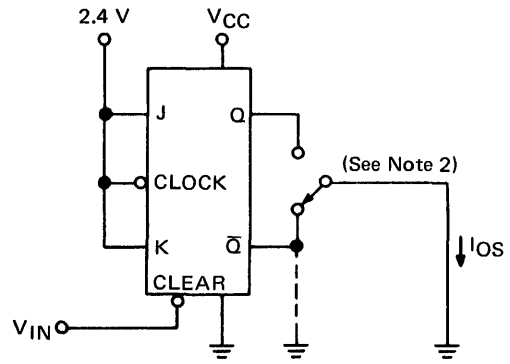


TEST TABLE

Apply V_{IN} (Test I_{IH})	Ground	Apply Momentary GND, then 4.5 V
Clock	Clear, J, and K	None
Clear	Clock and J	None
Preset (See Note 1)	Clock and K	None
J (See Note 1)	Clock and Clear	Preset
K (See Note 1)	Clock and Preset	Clear

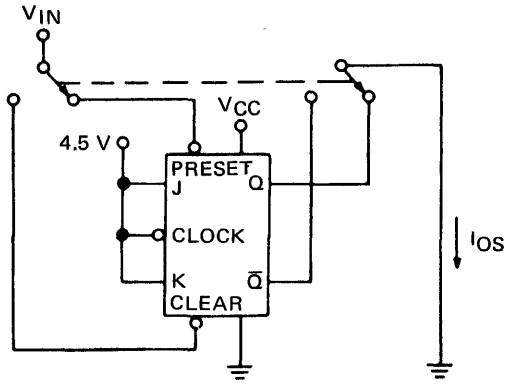
1. Preset is applicable for 9N76/5476, 7476 circuits only.
2. I_{CC} is measured (simultaneously for both flip-flops) for the following conditions:
   a. J = K = Clock = Clear = GND. For 9N76/5476, 7476: Preset = 4.5 V.
   b. For 9N73/5473, 7473: J = Clear = 4.5 V, K = GND, and apply momentary 4.5 V, then GND to Clock. For 9N76/5476, 7476: J = K = Clock = Preset = GND, and Clear = 4.5 V.
3. Each flip-flop is tested separately for I_{IH}.

Fig. 49



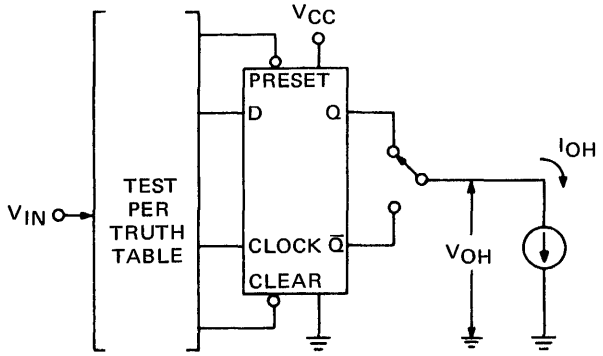
1. Each flip-flop is tested separately.
2. Test circuit shows setup for testing $\overline{Q}$. When testing Q, apply 2.4 V to Clear, ground $\overline{Q}$, and limit duration of test to 100 ms.

Fig. 50



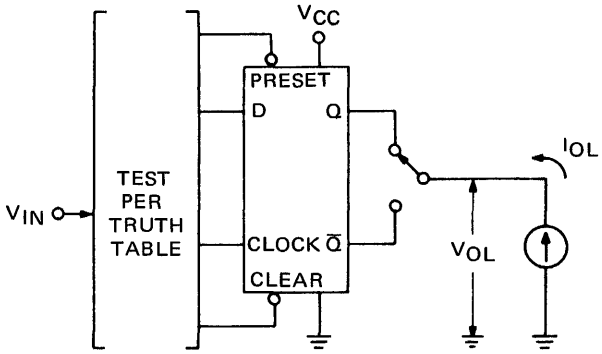
1. Each flip-flop is tested separately.

Fig. 51



1. Each flip-flop is tested separately.
2. Each output is tested separately.

Fig. 52



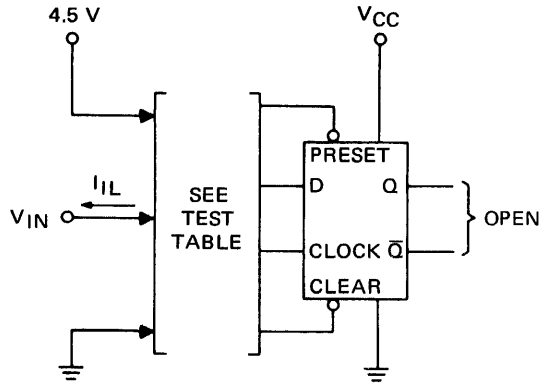
1. Each flip-flop is tested separately.
2. Each output is tested separately.

Fig. 53

*Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS* (Continued)

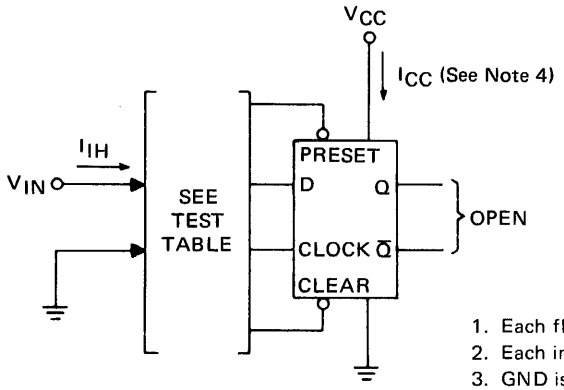


TEST TABLE

Apply V_{IN} (Test I_{IL})	Apply 4.5 V	Apply GND
Clock	Clear	Preset and D
Preset	Clear	Clock and D
Clear	Clock, D, and Preset	None
D	Clear and Clock	Preset

1. Each flip-flop is tested separately.
2. Each input is tested separately.

Fig. 54

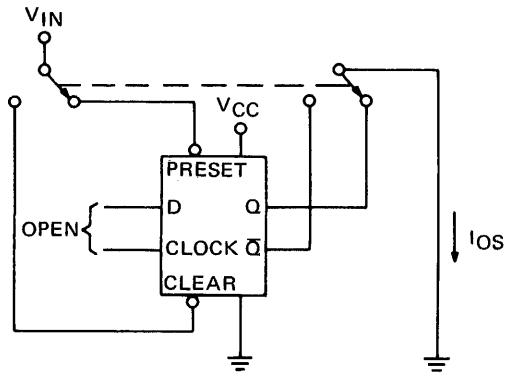


TEST TABLE

Apply V_{IN} (Test I_{IH})	Apply 4.5 V	Apply GND
Clock	Clear and D	Preset
Clock	Preset and D	Clear
Preset	Clear and D	Clock (See Note 3)
Clear	Preset	Clock, D, and Q
Clear	Preset	D and Clock (See Note 3)
D	Preset and Clock	Clear

1. Each flip-flop is tested seperately.
2. Each input is tested seperately.
3. GND is momentarily applied to clock, then 4.5V.
4. For 9N74/5474, 7474: I_{CC} is measured with D, clock, and preset at GND, then with D, clock, and clear at GND.
5. For 9H74/5474, 74H74: I_{CC} is measured simultaneously for both flip-flops with D. Clock, and Preset at GND, then with D, Clock, and Clear at GND.

Fig. 55



Each input is tested separately.

Fig. 56

*Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS* (Continued)

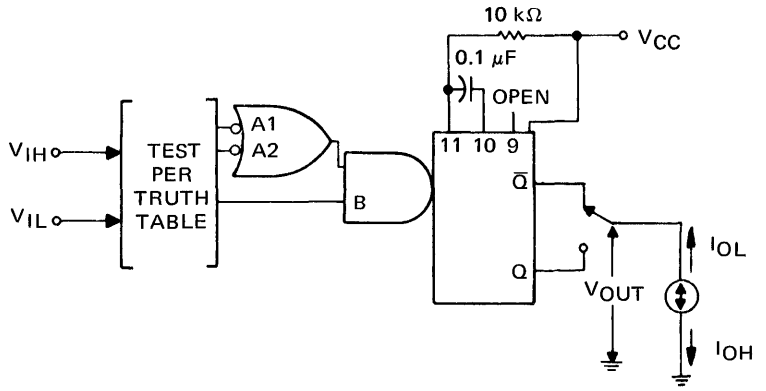
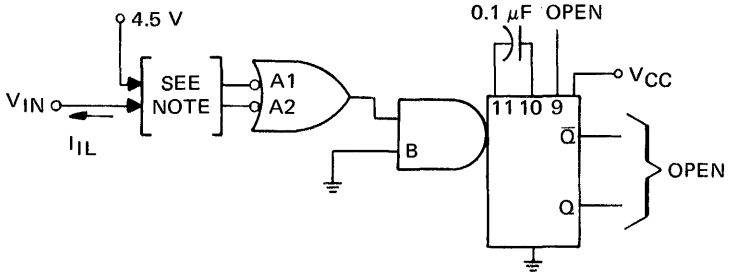


Fig. 57



1. Each input is tested separately. Input not being tested is at 4.5 V.

Fig. 58

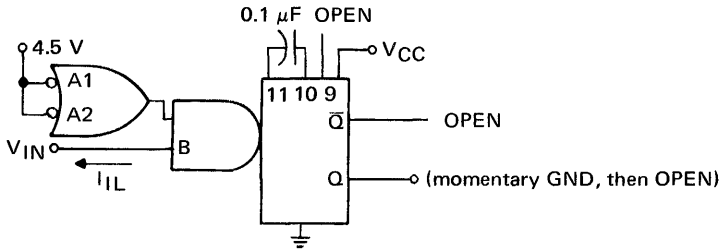
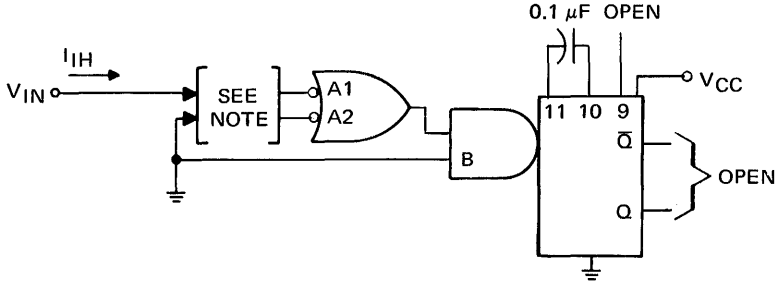


Fig. 59



1. Each input is tested separately. Input not being tested is at ground.

Fig. 60

*Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS* (Continued)

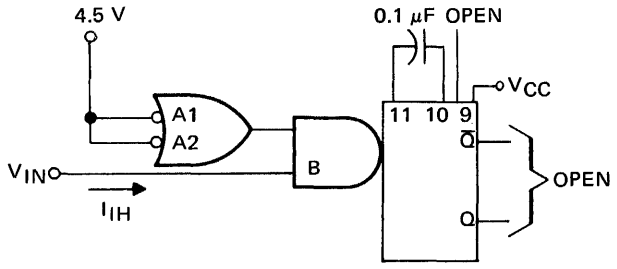
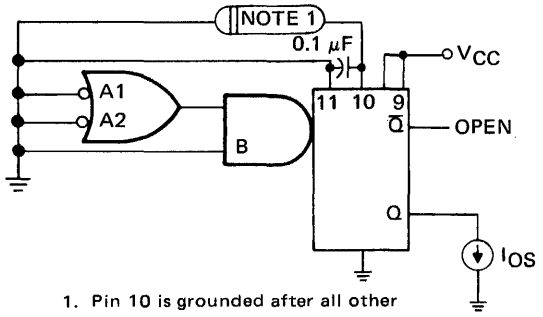


Fig. 61



1. Pin 10 is grounded after all other indicated grounds are made.

Fig. 62

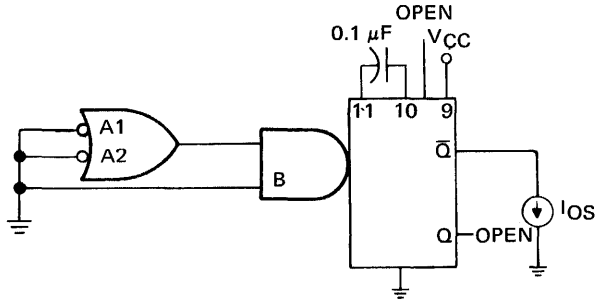
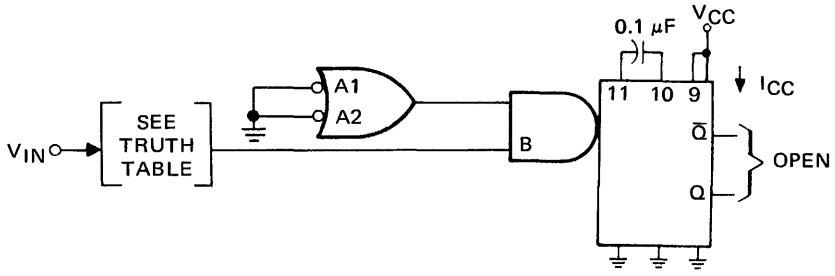


Fig. 63



1. Quiescent and fired conditions are tested.

Fig. 64

*Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS* (Continued)

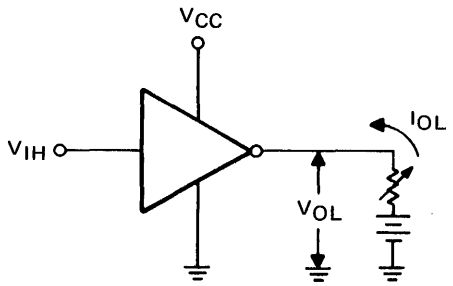


Fig. 65 V_{IH}, V_{OL}

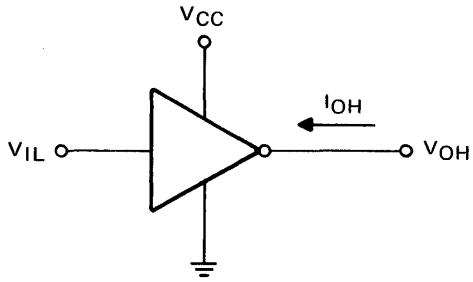


Fig. 66 V_{IL}, I_{OH}

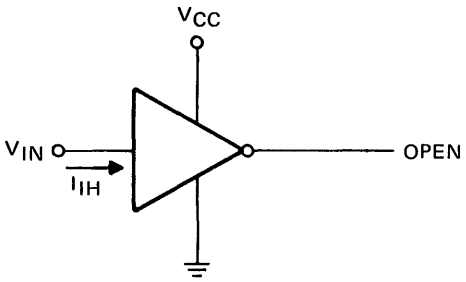


Fig. 67 I_{IH}

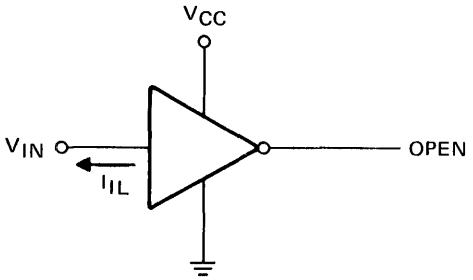
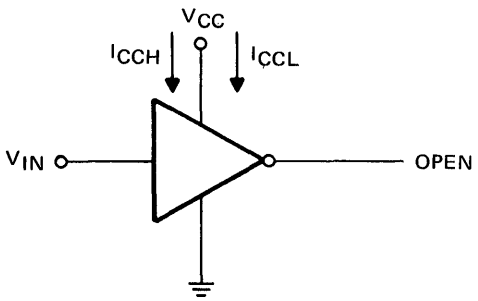


Fig. 68 I_{IL}



All inverters are tested simultaneously

Fig. 69 I_{CCH}, I_{CCL}

*Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS*

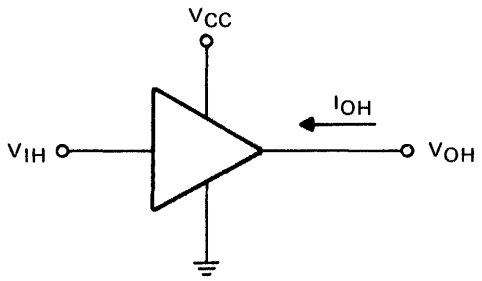


Fig. 70 V_{IH}, I_{OH}

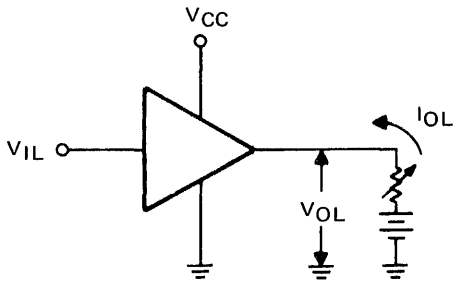


Fig. 71 V_{IL}, V_{OL}

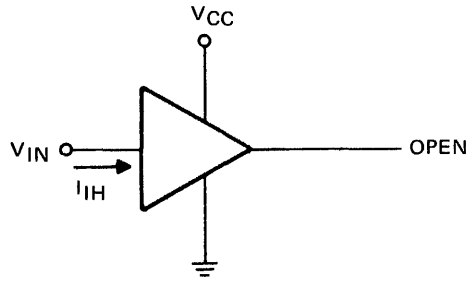


Fig. 72 I_{IH}

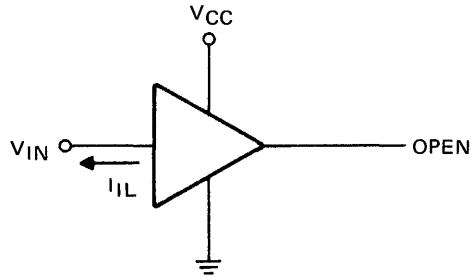
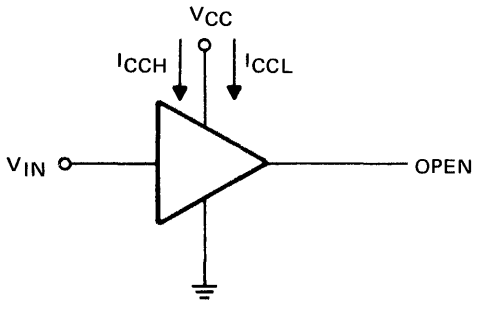


Fig. 73 I_{IL}



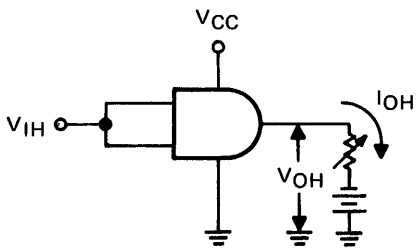
All buffers/drivers are tested simultaneously.

Fig. 74 I_{CCH}, I_{CCL}

*Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS* (Continued)



Both inputs are tested simultaneously.

Fig. 75 V_{IH}, V_{OH}

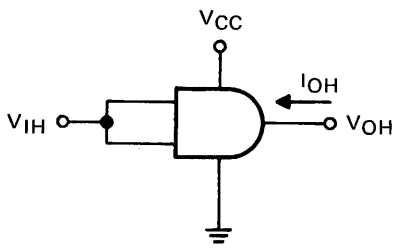
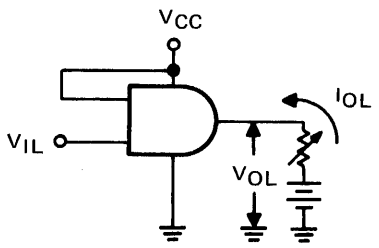
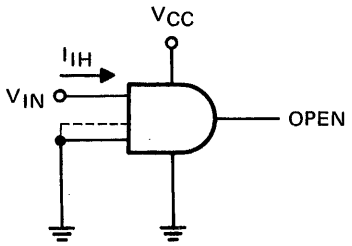


Fig. 76 V_{IH}, I_{OH}



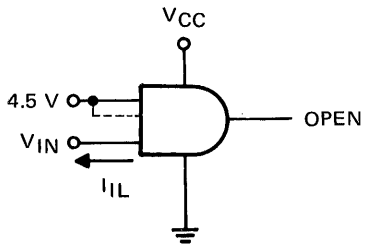
Each input is tested separately.

Fig. 77 V_{IL}, V_{OL}



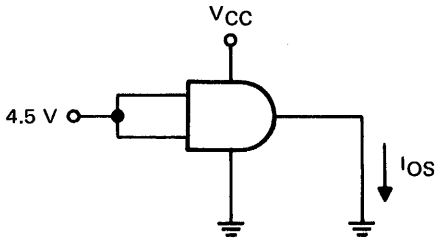
Each input is tested separately.

Fig. 78 I_{IH}



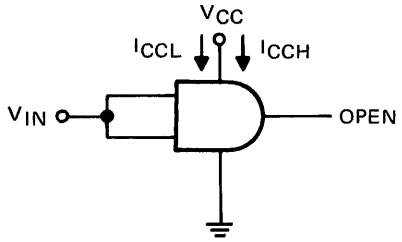
Each input is tested separately.

Fig. 79 I_{IL}



Each gate is tested separately.

Fig. 80 I_{OS}



1. HIGH level and LOW level conditions are tested.
2. All gates are tested simultaneously.

Fig. 81 I_{CCH}, I_{CCL}

*Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS* (Continued)

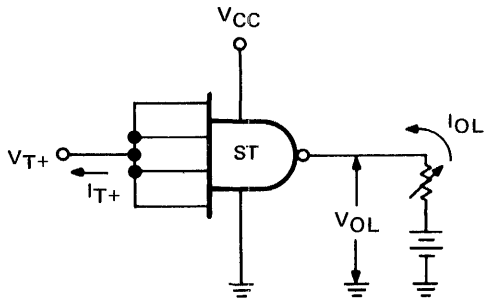


Fig. 82 V_{T+}, I_{T+}, V_{OL}

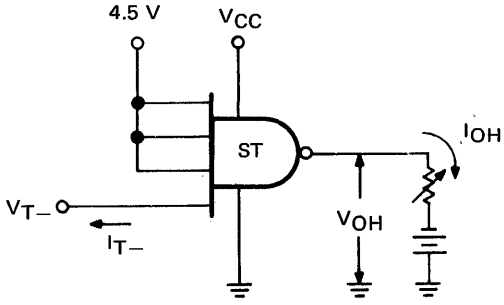
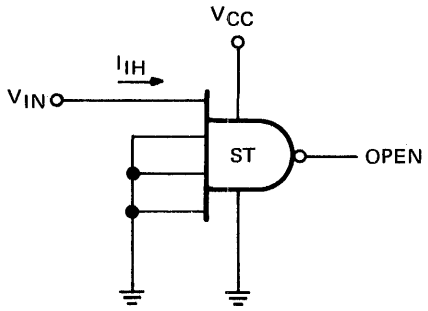
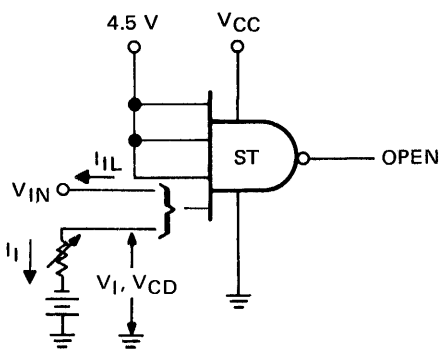


Fig. 83 V_{T-}, I_{T-}, V_{OH}



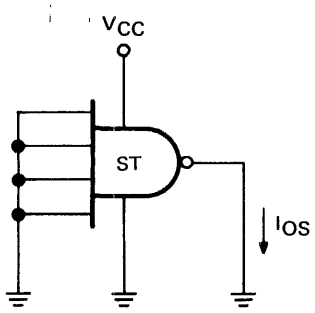
Each input is tested separately.

Fig. 84 I_{IH}



Each input is tested separately.

Fig. 85 V_I, V_{CD}, I_{IL}



Each gate is tested separately.

Fig. 86 I_{OS}

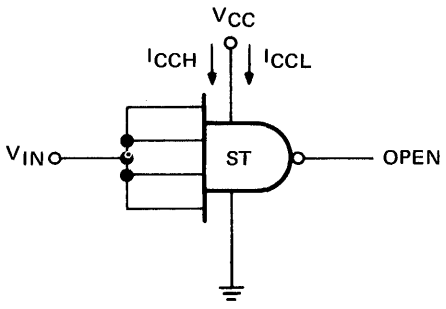
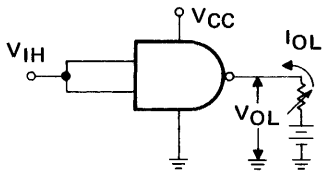


Fig. 87 I_{CCH}, I_{CCL}

*Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

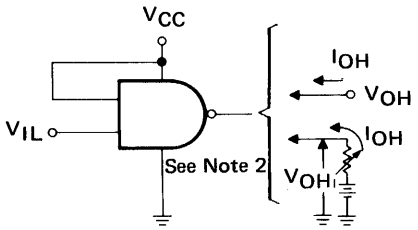
PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS* (Continued)



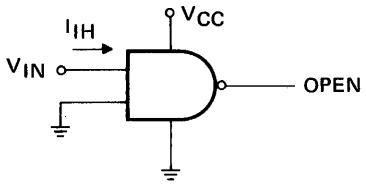
Both inputs are tested simultaneously

Fig. 88 V_{IH}, V_{OL}



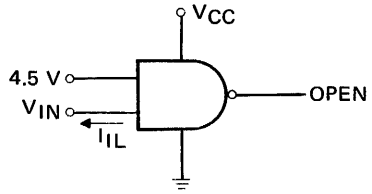
1. Each input is tested separately.
2. I_{OH} is tested at V_{OH} = 12 V and V_{OH} is tested at I_{OH} = 1 mA.

Fig. 89 V_{IL}, V_{OH}, I_{OH}



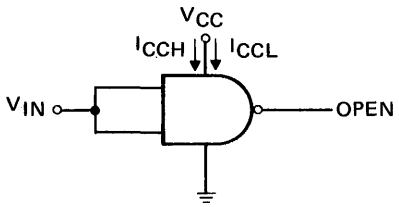
Each input is tested separately.

Fig. 90 I_{IH}



Each input is tested separately.

Fig. 91 I_{IL}



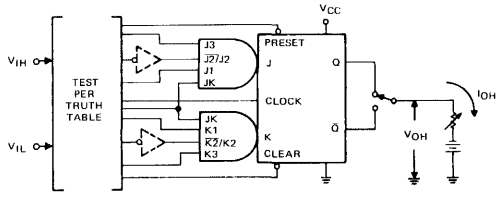
High-level and low-level output conditions are tested.

Fig. 92 I_{CCH}, I_{CCL}

*Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

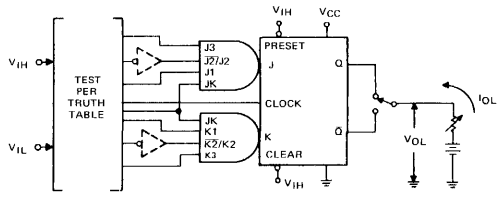
PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS* (Continued)



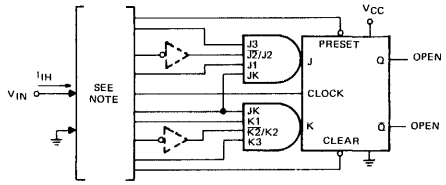
NOTES:
1. Each output is tested separately.
2. V_{OH} is also tested using clear and preset inputs.

Fig. 93 V_{IH}, V_{IL}, V_{OH}



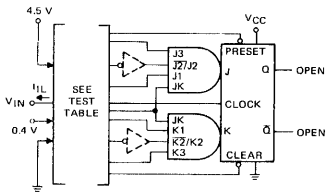
NOTE: Each output is tested separately.

Fig. 94 V_{IH}, V_{IL}, V_{OL}



NOTE: V_{IN} is applied and I_{IH} is measured separately for each input. All other inputs are grounded.

Fig. 95 I_{IH}



NOTES:
1. Each input is tested separately.
2. V_{IN} is applied and I_{IL} is measured separately for each input.
3. All unspecified inputs are at 4.5 V.

Fig. 96 I_{IL}

TEST TABLE

Apply V_{IN} (Test I_{IL})	CONDITIONS ON OTHER INPUTS	
	Apply 0.4 V	Apply GND
Clock	None	None
Preset	Clear	Clock
Clear	Preset	Clock
J1	$\overline{J2}$ (OR 4.5 V TO J2)	Clock, Clear
$\overline{J2}$ (OR J2)	None	Clock, Clear
J3	$\overline{J2}$ (OR 4.5 V TO J2)	Clock, Clear
JK	$\overline{J2}$, K2 (OR 4.5 V TO J2, K2)	Clock, Clear
JK	$\overline{J2}$, $\overline{K2}$ (OR 4.5 V TO J2, K2)	Clock, Preset
K1	$\overline{K2}$ (OR 4.5 V TO K2)	Clock, Preset
$\overline{K2}$ (OR K2)	None	Clock, Preset
K3	$\overline{K2}$ (OR 4.5 V TO K2)	Clock, Preset

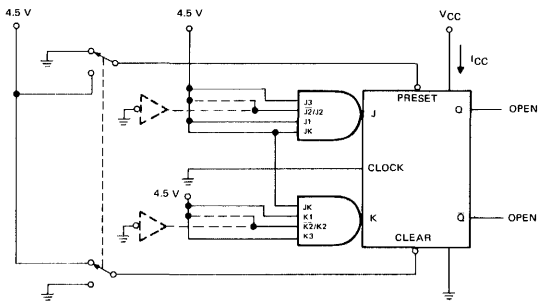
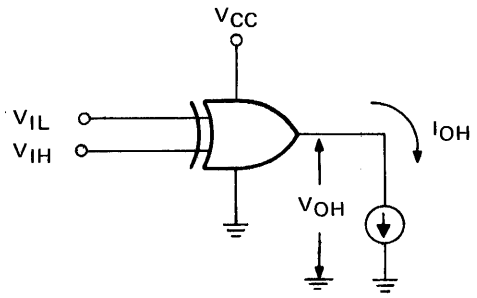


Fig. 97 I_{CC}

*Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

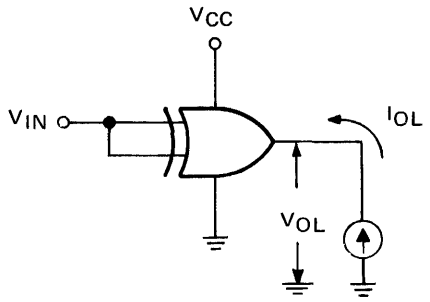
PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS* (Continued)



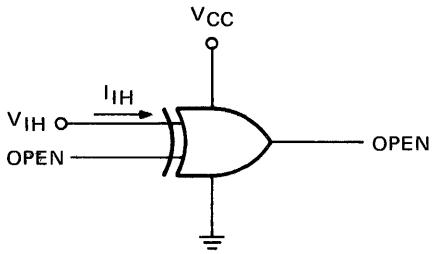
1. Each input is tested separately.

Fig. 98



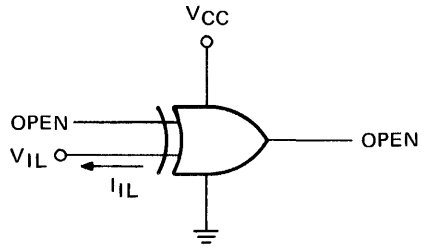
1. Low level and high level input conditions are tested.

Fig. 99



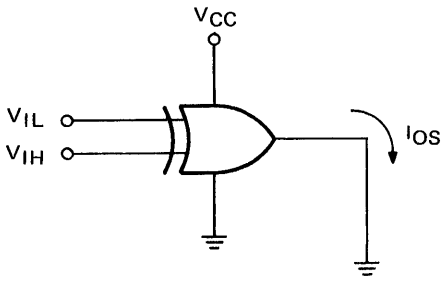
1. Each input is tested separately.

Fig. 100



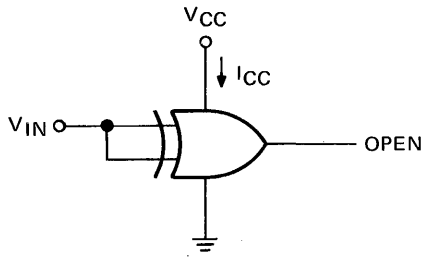
1. Each input is tested separately.

Fig. 101



1. Each gate is tested separately.

Fig. 102



1. Low level and high level input conditions are tested.

Fig. 103

*Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS*

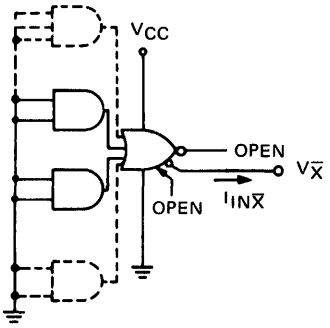
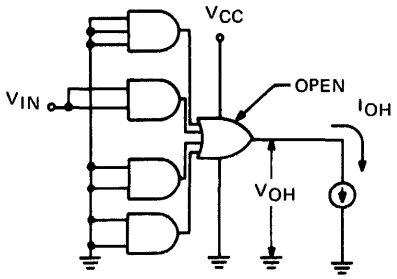
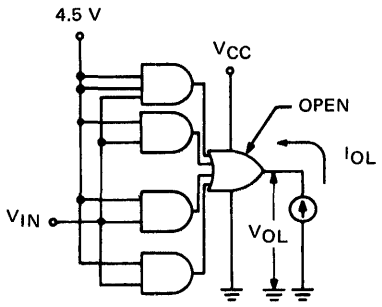


Fig. 104.



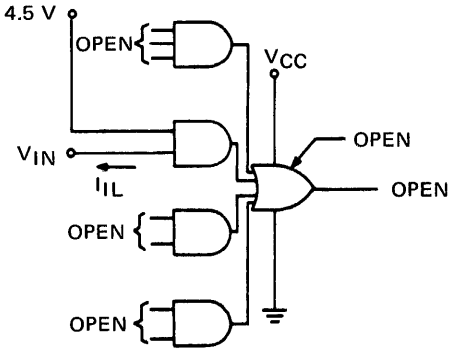
1. Each AND section is tested separately.

Fig. 105.



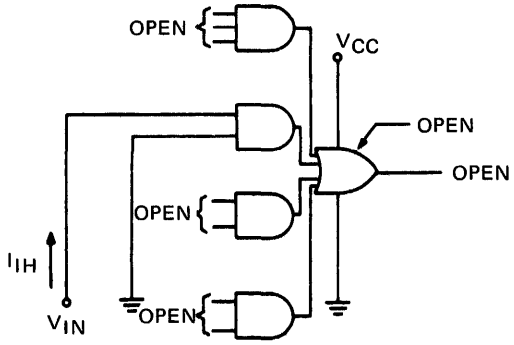
1. Each set of inputs is tested separately.

Fig. 106.



1. Each input of each AND section is tested separately.

Fig. 107.



1. Each input of each AND section is tested separately.

Fig. 108.

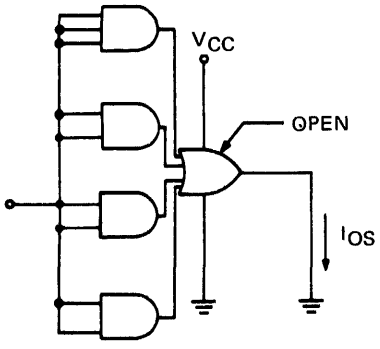
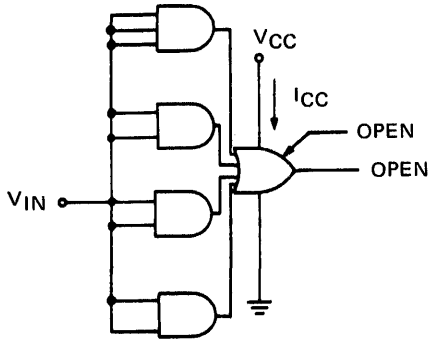


Fig. 109.



1. Logical 0 and logical 1 conditions are tested.

Fig. 110.

*Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS* (Continued)

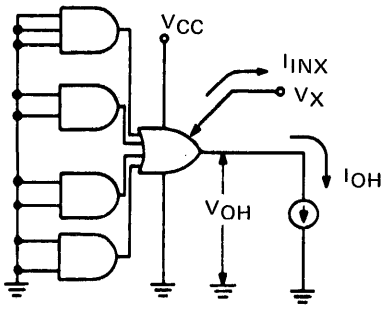


Fig. 111.

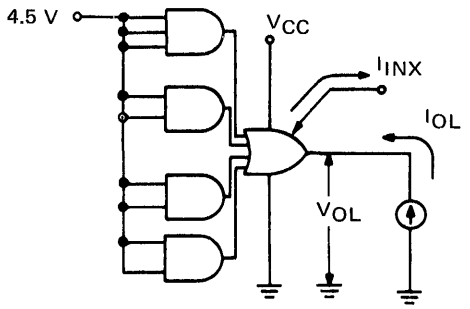
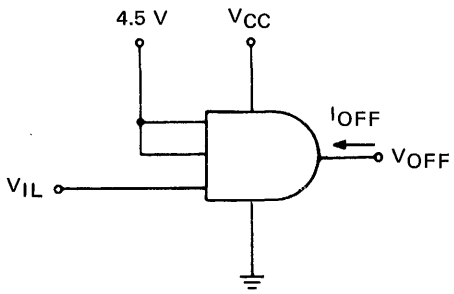
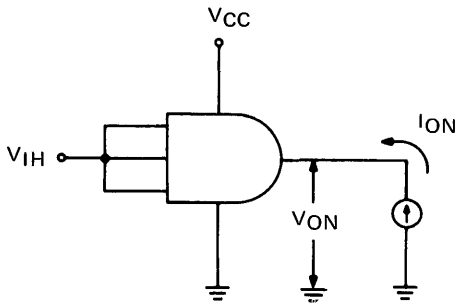


Fig. 112.



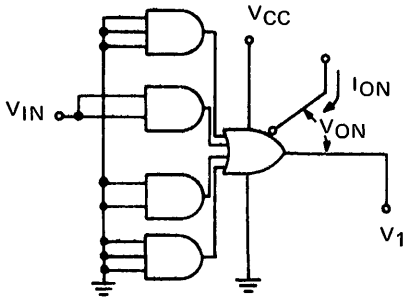
1. Each input is tested separately.

Fig. 113.



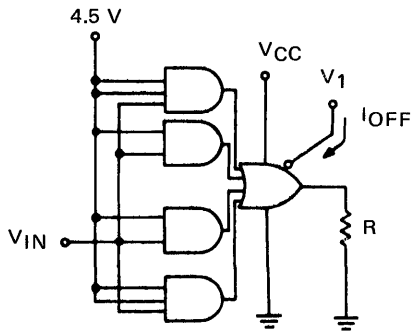
1. All inputs are tested simultaneously.

Fig. 114.



1. Each AND section is tested separately.

Fig. 115.



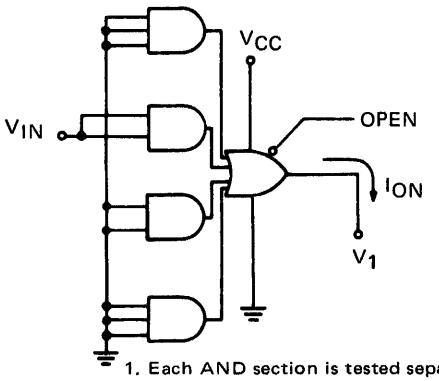
1. Each set of inputs is tested separately.

Fig. 116.

*Arrows indicate actual direction of current flow.

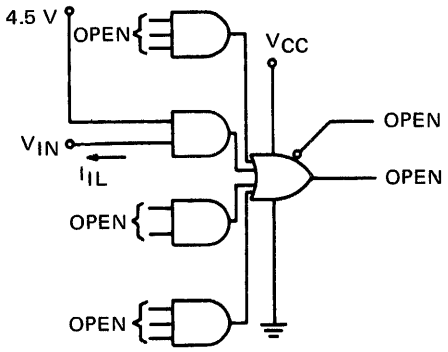
PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS* (Continued)



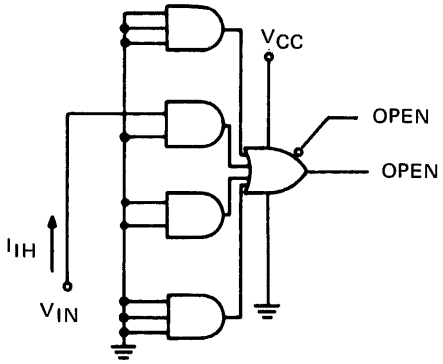
1. Each AND section is tested separately.

Fig. 117.



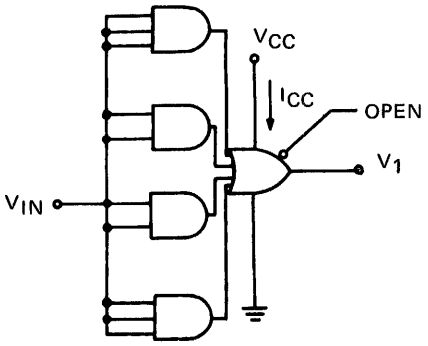
1. Each input is tested separately.

Fig. 118.



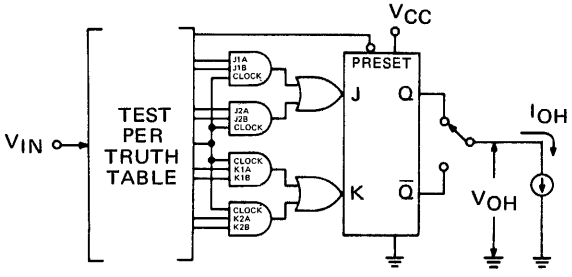
1. Each input is tested separately.

Fig. 119.



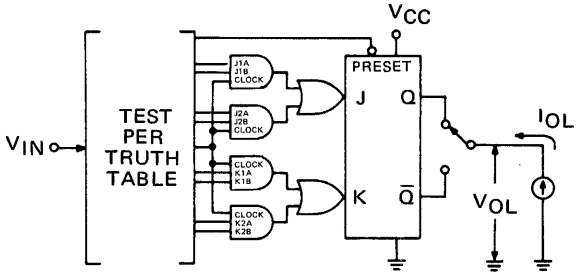
1. On and off conditions are tested separately.

Fig. 120.



1. Each output is tested separately.

Fig. 121.



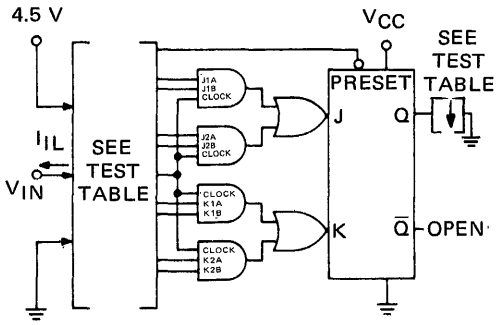
1. Each output is tested separately.

Fig. 122.

*Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS* (Continued)



1. Each input is tested separately.

TEST TABLES[a]

9H71/54H71, 74H71

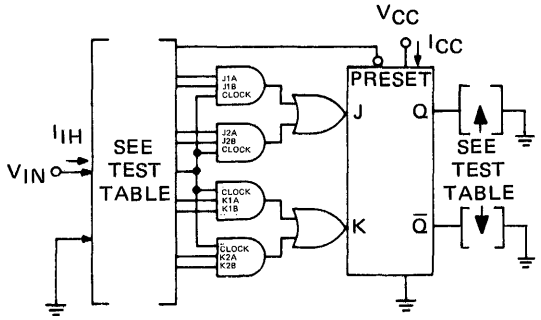
Apply V_{IN} (Test I_{IL})	Apply 4.5 V	Apply Momentary GND then 4.5 V	GND
Clock	J1A,J1B,J2A,J2B,K1A,K1B,K2A, and K2B	Preset	None
Clock[b]	J1A,J1B,J2A,J2B,K1A,K1B,K2A,K2B, and Preset	None	Q
Preset	J1A,J1B,J2A,J2B,K1A,K1B,K2A,K2B, and Clock	None	None
J1A[b]	J1B and Clock	None	Q
J1B[b]	J1A and Clock	None	Q
J2A[b]	J2B and Clock	None	Q
J2B[b]	J2A and Clock	None	Q
K1A	K1B and Clock	Preset	None
K1B	K1A and Clock	Preset	None
K2A	K2B and Clock	Preset	None
K2B	K2A and Clock	Preset	None

9H101/54H101, 74H101

Apply V_{IN} (Test I_{IL})	Apply 4.5 V	Ground
Clock	J1A, J1B, J2A, J2B, K1A, K1B, K2A, K2B	Preset
Preset	J1A, J1B, J2A, J2B, K1A, K1B, K2A, K2B, Clock	None
J1A[b]	J1B, J2A, J2B, K1A, K1B, K2A, K2B, Clock, Preset	Q
J1B[b]	J1A, J2A, J2B, K1A, K1B, K2A, K2B, Clock, Preset	Q
J2A[b]	J1A, J1B, J2B, K1A, K1B, K2A, K2B, Clock, Preset	Q
J2B[b]	J1A, J1B, J2A, K1A, K1B, K2A, K2B, Clock, Preset	Q
K1A	J1A, J1B, J2A, J2B, K1B, K2A, K2B, Clock	Preset
K1B	J1A, J1B, J2A, J2B, K1A, K2A, K2B, Clock	Preset
K2A	J1A, J1B, J2A, J2B, K1A, K1B, K2B, Clock	Preset
K2B	J1A, J1B, J2A, J2B, K1A, K1B, K2A, Clock	Preset

[a] Inputs and outputs not specified are open.
[b] Duration of this test should not exceed 1 second.

Fig. 123.



1. Each input is tested separately.
2. I_{CC} is measured for each of the following conditions: A) J1A = J1B = J2A = J2B = K1A = K1B = K2A = K2B = Preset = 4.5 V, and Clock = momentary 4.5 V, then Gnd.

TEST TABLES[a]

9H71/54H71, 74H71

Apply V_{IN} (Test I_{IH})	Ground
Clock	J1A,J1B,J2A,J2B,K1A,K1B,K2A,K2B, and Preset
Clock[b]	J1A,J1B,J2A,J2B,K1A,K1B,K2A,K2B, Preset and Q
Preset	K1A,K1B,K2A,K2B,Clock, and Q
J1A	J1B, Clock, and Preset
J1B	J1A, Clock, and Preset
J2A	J2B, Clock, and Preset
J2B	J2A, Clock, and Preset
K1A[b]	K1B, Clock, Preset, and Q
K1B[b]	K1A, Clock, Preset, and Q
K2A[b]	K2B, Clock, Preset, and Q
K2B[b]	K2A, Clock, Preset, and Q

9H101/54H101, 74H101

Apply V_{IN} (Test I_{IH})	Ground	Apply 4.5 V
Clock	J1A, J1B, J2A, J2B, K1A, K1B, K2A, K2B, Preset	None
Preset[b]	J1A, J1B, J2A, J2B, K1A, K1B, K2A, K2B, $\bar{Q}$	Clock
J1A	J1B, J2A, J2B, Preset, Clock	K1A, K1B, K2A, K2B
J1B	J1A, J2A, J2B, Preset, Clock	K1A, K1B, K2A, K2B
J2A	J1A, J1B, J2B, Preset, Clock	K1A, K1B, K2A, K2B
J2B	J1A, J1B, J2A, Preset, Clock	K1A, K1B, K2A, K2B
K1A	K1B, K2A, K2B, Clock	Preset J1A, J1B, J2A, J2B
K1B	K1A, K2A, K2B, Clock	Preset J1A, J1B, J2A, J2B
K2A	K1A, K1B, K2B, Clock	Preset J1A, J1B, J2A, J2B
K2B	K1A, K1B, K2B, Clock	Preset J1A, J1B, J2A, J2B

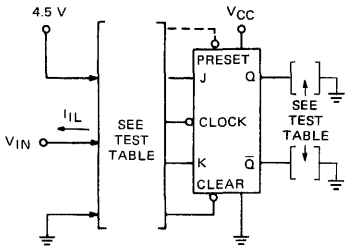
[a] Inputs and outputs not specified are open.
[b] Duration of this test should not exceed 1 second.

Fig. 124.

*Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS* (Continued)



1. Each flip-flop is tested separately.
2. Apply momentary ground, then 4.5 V.
3. After application of momentary ground (<1 second), Q and $\bar{Q}$ are left floating.
4. Ground all inputs of the unused flip-flop.
5. Preset is not applicable for 9H73/54H73, 74H73.
6. Apply the same conditions simultaneously to both flip-flops when testing the 9H108/54H108, 74H108.

TEST TABLES

9H73/54H73, 74H73
9H76/54H76, 74H76
9H78/54H78, 74H78

Apply V_{IN} (Test I_{IL})	Apply Momentary GND	Apply 4.5 V
Clock	Clear (See Note 2)	J and K
Clear	None	Clock and J
Preset	None (See Note 5)	Clock and K
J	Q (See Note 3)	Clock and Clear
K	$\bar{Q}$ (See Note 3)	Clock and Clear

9H103/54H103, 74H103

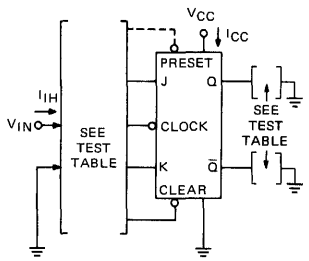
Apply V_{IN} (Test I_{IL})	Apply GND	Apply 4.5 V
Clock	Clear	J, K
Clear	None	Clock, J, K
J	Clear	Clock, K
K†	Q	Clock, Clear, J

†Duration of this test should not exceed 1 second.

9H106/54H106, 74H106
9H108/54H108, 74H108

Apply V_{IN} (Test I_{IL})	Apply GND	Apply 4.5 V
Clock	Clear	J, K, Preset, (Note 6)
Clock	Preset	J, K, Clear, (Note 6)
Clear	None	Clock, Preset, J, K, (Note 6)
Preset	None	Clock, Clear, J, K
J	Clear	Clock, K Preset
K	Preset	Clock, Clear, J

Fig. 125.



1. Preset is not applicable to 9H73/54H73, 74H73; 9H103/54H103, 74H103.
2. I_{CC} is measured (simultaneously for both flip-flops) for the following conditions:
   a. J = K = Clock = Clear = Gnd. Preset (when applicable) = 4.5 V.
   b. For 9H73/54H73, 74H73 and 9H103/54H103, 74H103. J = Clear = 4.5 V, K = Gnd, and apply momentary 4.5 V, then Gnd, to Clock. For 9H76/54H76, 74H76; 9H78/54H78, 74H78; 9H108/54H108, 74H108: J = K = Clock = Preset = Gnd, and Clear = 4.5 V.
3. Each flip-flop is tested separately except where Note 4 is referenced.
4. Apply the same conditions to both flip-flops when testing the 9H108/54H108, 74H108.

TEST TABLES

9H73/54H73, 74H73
9H76/54H76, 74H76
9H78/54H78, 74H78

Apply V_{IN} (Test I_{IH})	Ground	Apply Momentary GND, then 4.5 V
Clock	Clear, J, and K	None
Clear	Clock and J	None
Preset (See Note 1)	Clock and K	None
J (See Note 1)	Clock and Clear	Preset
K (See Note 1)	Clock and Preset	Clear

9H103/54H103, 74H103

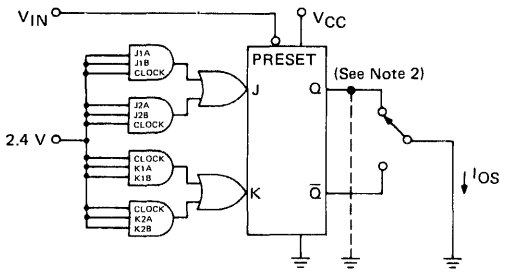
Apply V_{IN} (Test I_{IH})	Apply GND	Apply 4.5 V
Clock	Clear, J, K	None
Clear†	Q, J, K	Clock
J	Clock	Clear, K
K	Clock, Clear	J

9H106/54H106, 74H106
9H108/54H108, 74H108

Apply V_{IN} (Test I_{IH})	Apply GND	Apply 4.5 V
Clock	Clear, J, K	Preset, (Note 4)
Clock	Preset, J, K	Clear, (Note 4)
Clear†	Q, J, K	Preset, Clock (Note 4)
Preset†	$\bar{Q}$, J, K	Clear, Clock
J	Clock, Preset	Clear, K
K	Clock, Clear	Preset, J

†Duration of this test should not exceed 1 second.

Fig. 126.

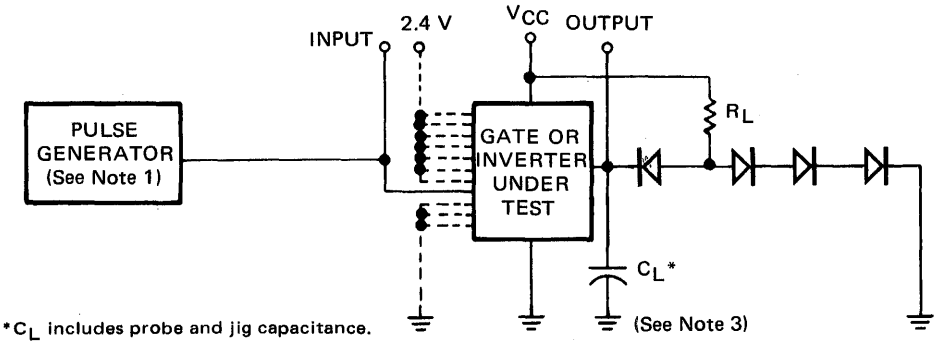


1. Each output is tested separately.
2. Test circuit shows setup for testing Q. When testing $\bar{Q}$, apply 2.4 V to Preset, ground Q, and limit duration of test to 100 ms.

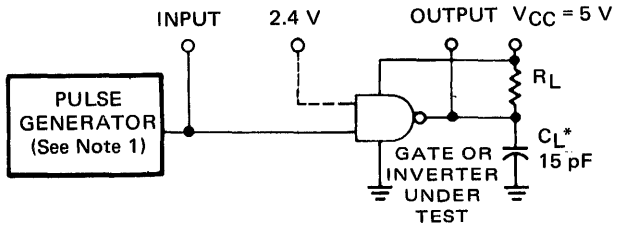
Fig. 127.

PARAMETER MEASUREMENT INFORMATION

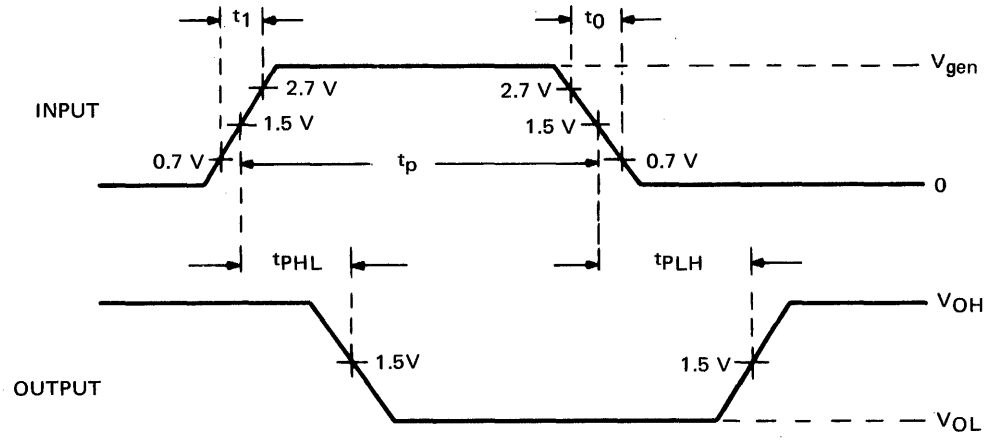
SWITCHING CHARACTERISTICS



TEST CIRCUIT FOR 9N00/5400, 7400; 9N02/5402, 7402; 9N04/5404, 7404; 9N10/5410, 7410; 9N20/5420, 7420; 9N30/5430, 7430; 9N40/5440, 7440; 9N50/5450, 7450; 9N51/5451, 7451; 9N53/5453, 7453 and 9N54/5454, 7454



TEST CIRCUIT FOR 9N01/5401, 7401; 9N03/5403, 7403; 9N05/5405, 7405; 9N39/5439, 7439



VOLTAGE WAVEFORMS

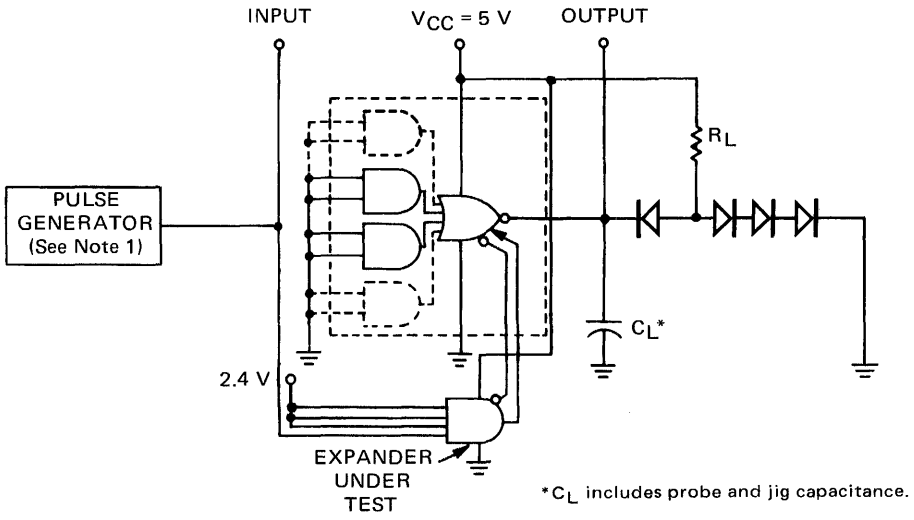
NOTES:

1. The generator has the following characteristics: V_{gen} = 3.5 V, t_0 = 5 ns, t_1 = 10 ns, t_p = 0.5 μs, PRR = 1 MHz, $Z_{out} \approx 50\Omega$.
2. Propagation Delay = $\frac{t_{PHL} + t_{PLH}}{2}$
3. When testing 9N00/5400, 7400 through 9N40/5440, 7440 (except 9N02/5402, 7402), connect all unused inputs to 2.4 V. When testing the 9N02/5402, 7402 or 9N50/5450, 7450 through 9N54/5454, 7454, apply the input pulse to one input of one AND section and 2.4 V to all unused inputs of that AND section. All inputs or unused AND sections are grounded.

Fig. A GATE PROPAGATION DELAY TIMES

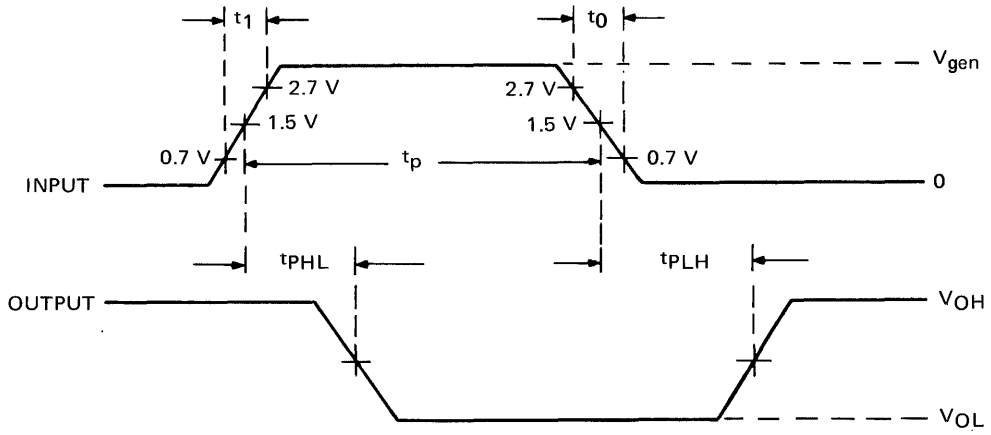
PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Continued)



*C_L includes probe and jig capacitance.

TEST CIRCUIT



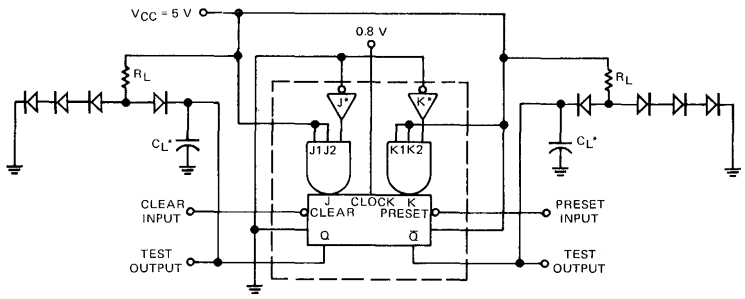
VOLTAGE WAVEFORMS

NOTES:
1. The generator has the following characteristics: V_{gen} = 3.5 V, t_0 = 5 ns, t_1 = 10 ns, t_p = 0.5 μs, PRR = 1 MHz, $Z_{out} \approx 50\Omega$.
2. Propagation Delay = $\frac{t_{PHL} + t_{PLH}}{2}$

Fig. B EXPANDER PROPAGATION DELAY TIMES

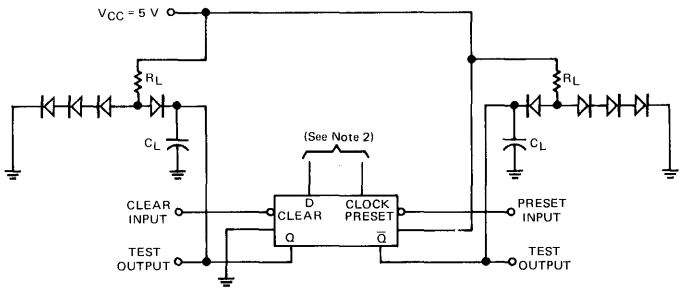
PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Continued)



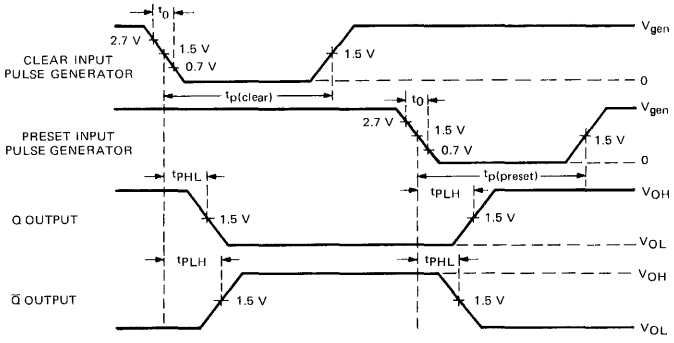
*C_L includes probe and jig capacitance.

9N70/5470, 7470 TEST CIRCUIT



9N74/5474, 7474 TEST CIRCUIT

NOTES:
1. Preset or clear function of the 9N70/5470, 7470 can occur only when clock input is low. Gated inputs are inhibited.
2. Clear and preset inputs of the 9N74/5474, 7474 dominate regardless of the state of clock or D inputs.



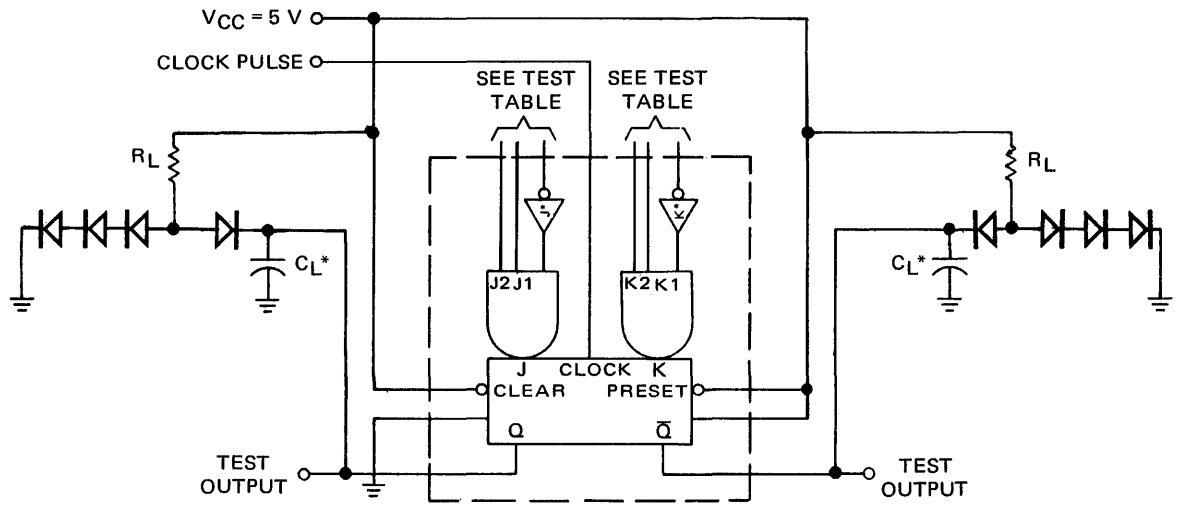
VOLTAGE WAVEFORMS

NOTE:
3. Clear or preset input pulse characteristics: V_{gen} = 3.5 V, t_0 = 5 ns, t_p = 25 ns for the 9N70/5470, 7470 and t_p = 30 ns for 9N74/5474, 7474.

Fig. C 9N70/5470, 7470 and 9N74/5474, 7474 PRESET/CLEAR PROPAGATION DELAY TIMES

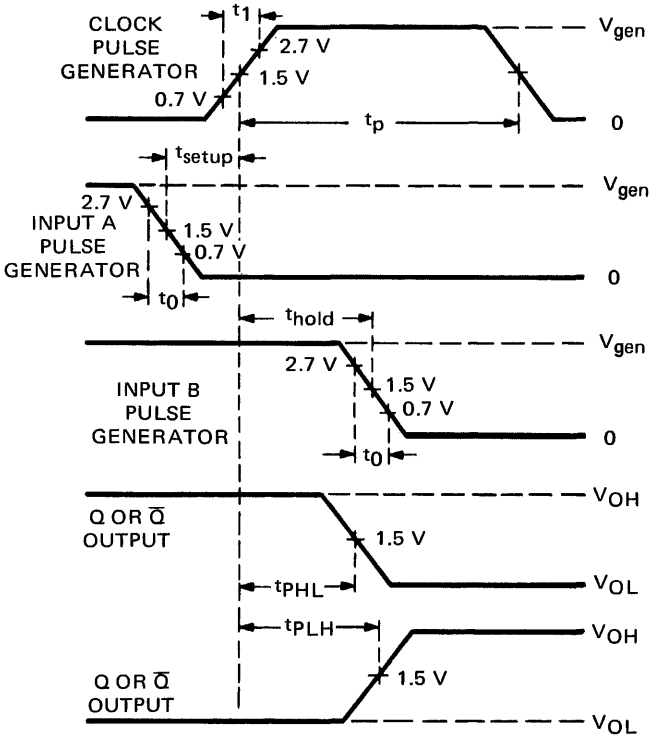
PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Continued)



*C_L includes probe and jig capacitance.

TEST CIRCUIT



VOLTAGE WAVEFORMS

TEST TABLE

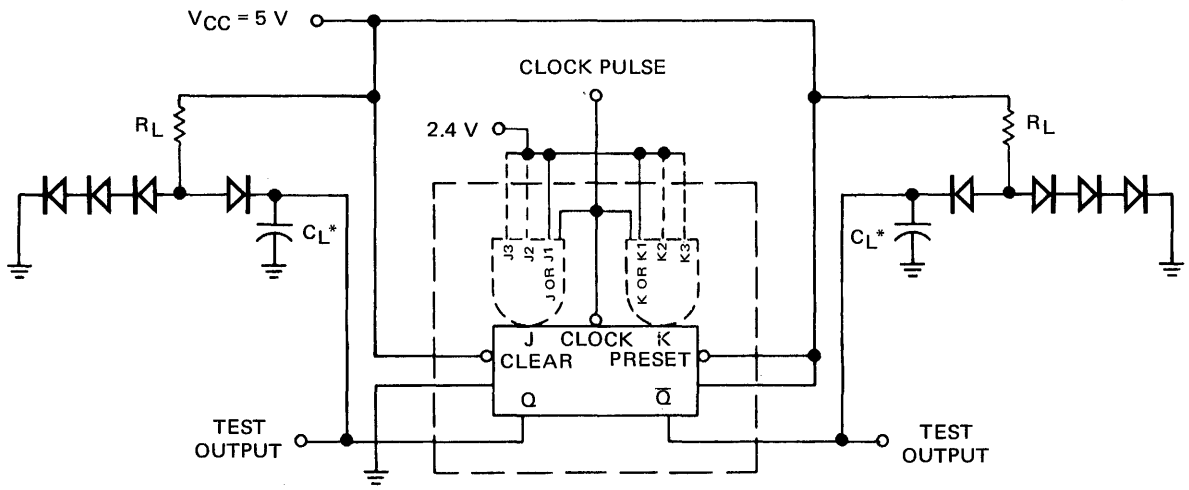
Test No.	Test	Input A	Input B	Apply 2.4 V	GND
1	t_{setup} at J*	J*	None	J1, J2, K1, K2	K*
2	t_{hold} at J1, J2	None	J1, J2	K1, K2	J* and K*
3	t_{setup} at K*	K*	None	J1, J2, K1, K2	J*
4	t_{hold} at K1, K2	None	K1, K2	J1, J2	J* and K*

NOTES:
1. Clock pulse (see note 3), input A, and input B are used to measure t_{setup} and t_{hold}.
2. Clock frequency, t_{PLH} and t_{PHL} (from clock to output) are measured in the toggle mode. Hold J = K = high level per truth table and apply clock pulse (see note 3).
3. Clock pulse characteristics: V_{gen} = 3.5 V, t_1 = 10 ns, t_p = 20 ns, and PRR = 1 MHz. When testing f_{max}, vary PRR.
4. Input pulse characteristics: V_{gen} = 3.5 V, t_0 = 5 ns.

Fig. D 9N70/5470, 7470 FLIP-FLOP SWITCHING TIMES

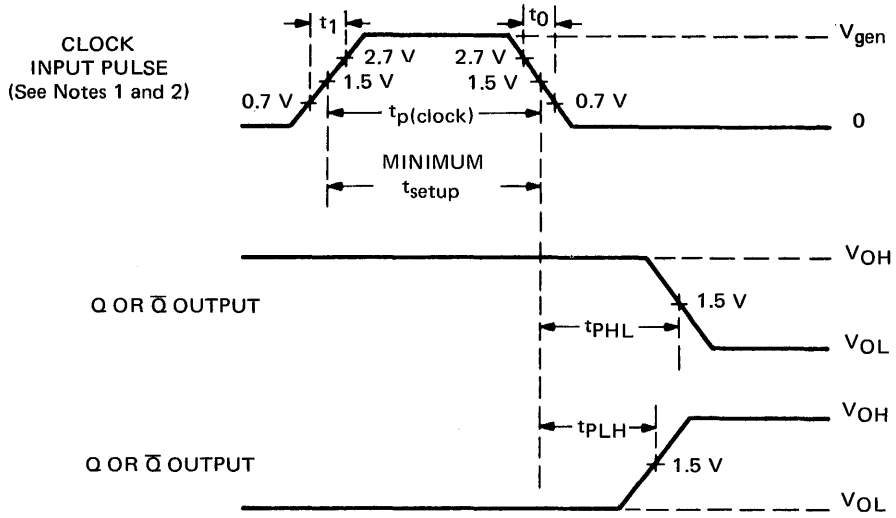
PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Continued)



*C_L includes probe and jig capacitance.

TEST CIRCUIT



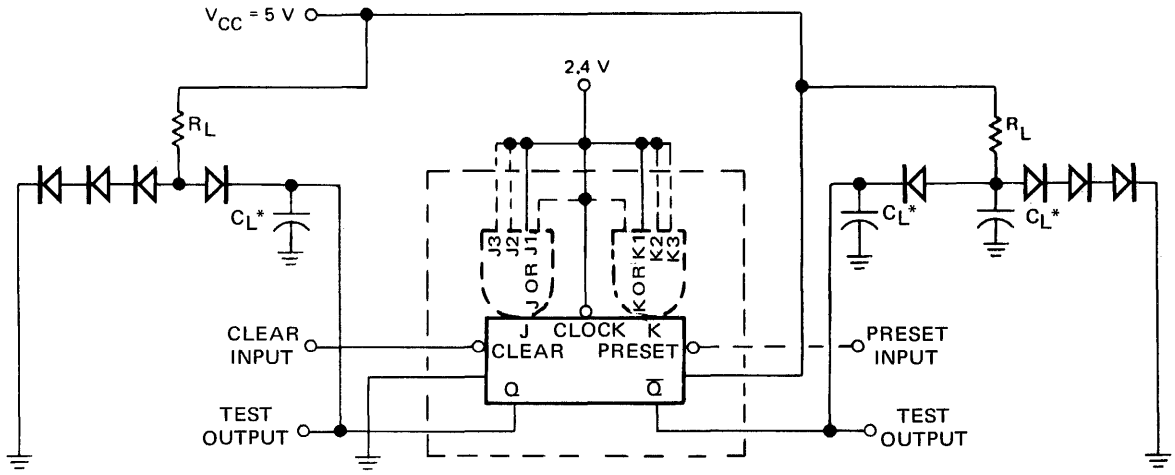
VOLTAGE WAVEFORMS

NOTES:
1. Clock, J, and K input pulse characteristics: V_{gen} = 3.5 V, t_0 = 10 ns, t_1 = 10 ns, t_p = 20 ns, and PRR = 1 MHz. When testing f_{max}, vary PRR.
2. For 9N72/5472, 7472, J = J1 · J2 · J3; and K = K1 · K2 · K3.
3. Gated inputs (shown with dotted lines) are for the 9N72/5472, 7472 only. The 9N73/5473, 7473; 9N107/54107, 74107 and 9N76/5476, 7476. Dual Flip-Flops have direct J and K inputs, and preset is not available on the 9N73/5473, 7473 and 9N107/54107, 74107.

Fig. E 9N72/5472, 7472; 9N73/5473, 7473; 9N76/5476, 7476; 9N107/54107, 74107 FLIP-FLOP SWITCHING TIMES

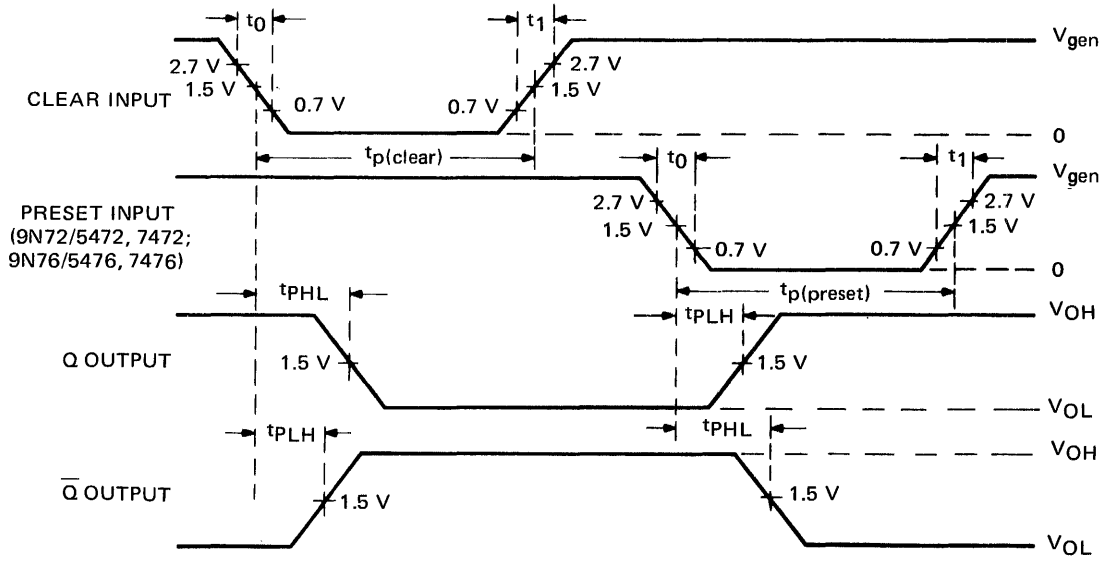
PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Continued)



*C_L includes probe and jig capacitance

TEST CIRCUIT



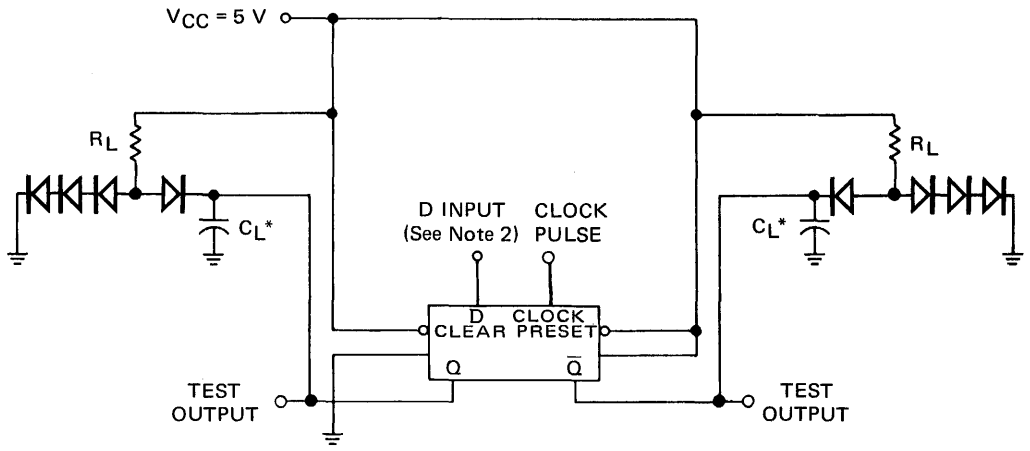
VOLTAGE WAVEFORMS

NOTES:
1. Clear or preset inputs dominate regardless of the state of clock or J-K inputs.
2. Clear or preset input pulse characteristics: V_{CC} = 3.5 V, t_0 = 5 ns, t_1 = 10 ns, $t_{p(clear)} = t_{p(preset)}$ = 25 ns, PRR = 1 MHz, and $Z_{out} \approx 50\Omega$.
3. Gates inputs (shown with dotted lines) are for the 9N72/5472, 7472 only. The 9N73/5473, 7473; 9N76/5476, 7476 and 9N107/54107, 74107 Dual Flip-Flops have direct J and K inputs, and preset is not available on the 9N73/5473, 7473 or 9N107/54107, 74107.

Fig. F 9N72/5472, 7472; 9N73/5473, 7473; 9N76/5476, 7476; 9N107/54107, 74107 PRESET/CLEAR PROPAGATION DELAY TIMES

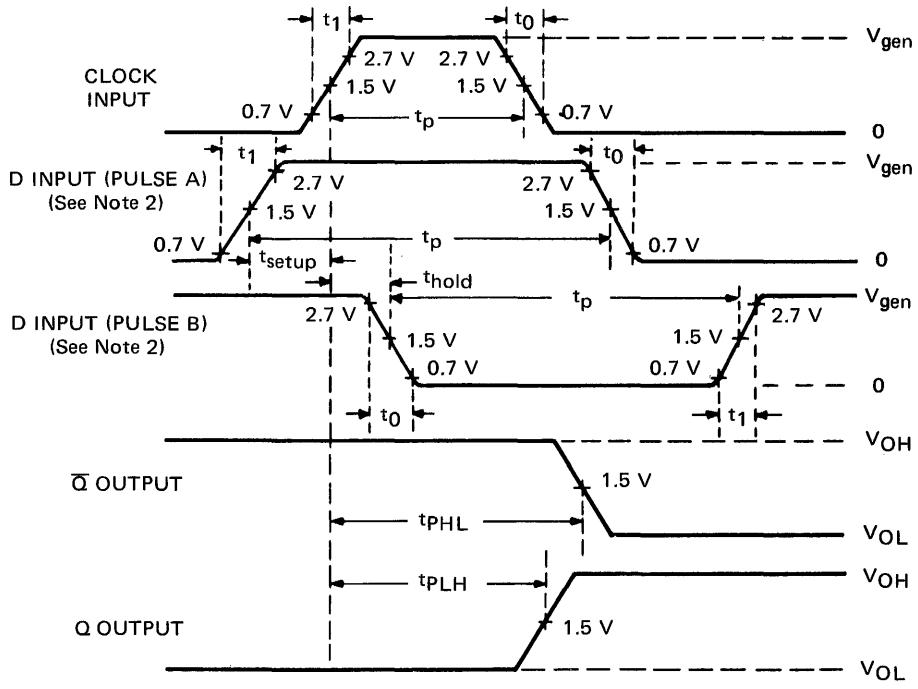
PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Continued)



*C_L includes probe and jib capacitance

TEST CIRCUIT



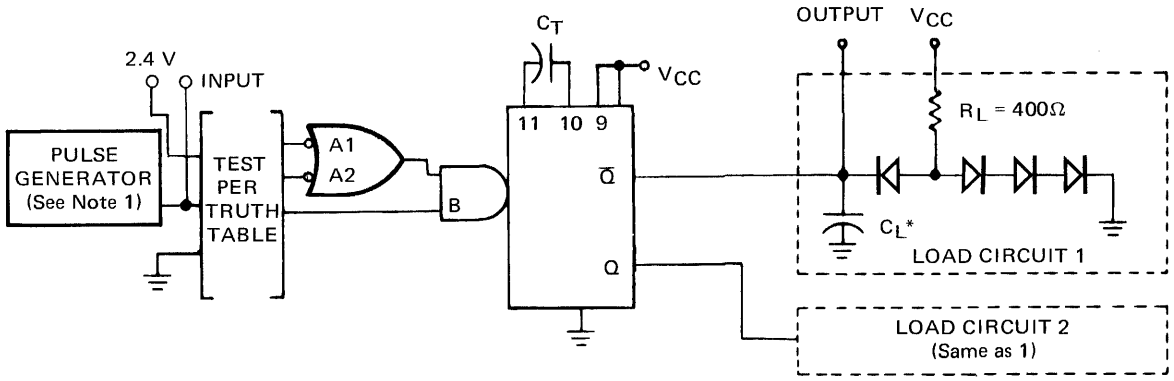
VOLTAGE WAVEFORMS

NOTES:
1. Clock input pulse has the following characteristics: V_{gen} = 3.5 V, t_0 = 10 ns, t_1 = 10 ns, t_p = 30 ns, and PRR = 1 MHz. When testing f_{max}, vary PRR.
2. D input (pulse A) has the following characteristics: V_{gen} = 3.5 V, t_0 = 10 ns, t_1 = 10 ns, t_{setup} = 20 ns, t_p = 60 ns, and PRR is 50% of the clock PRR. D input (pulse B) has the following characteristics: V_{gen} = 3.5 V, t_0 = 10 ns, t_1 = 10 ns, t_{hold} = 5 ns, t_p = 60 ns, and PRR is 50% of the clock PRR.

Fig. G 9N74/5474, 7474 FLIP-FLOP SWITCHING TIMES

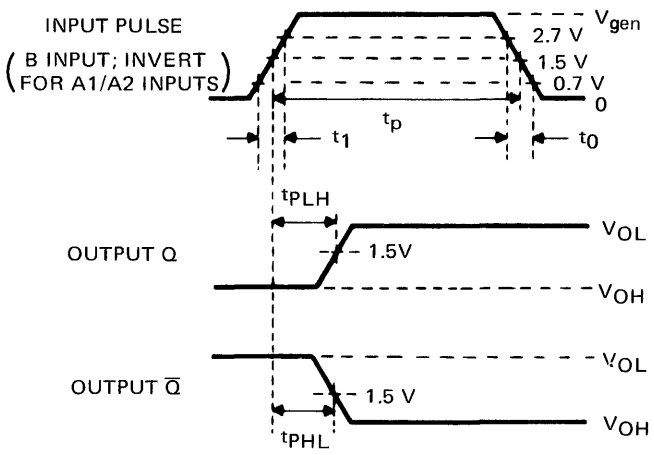
PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Continued)



*C_L includes probe and jig capacitance

TEST CIRCUIT



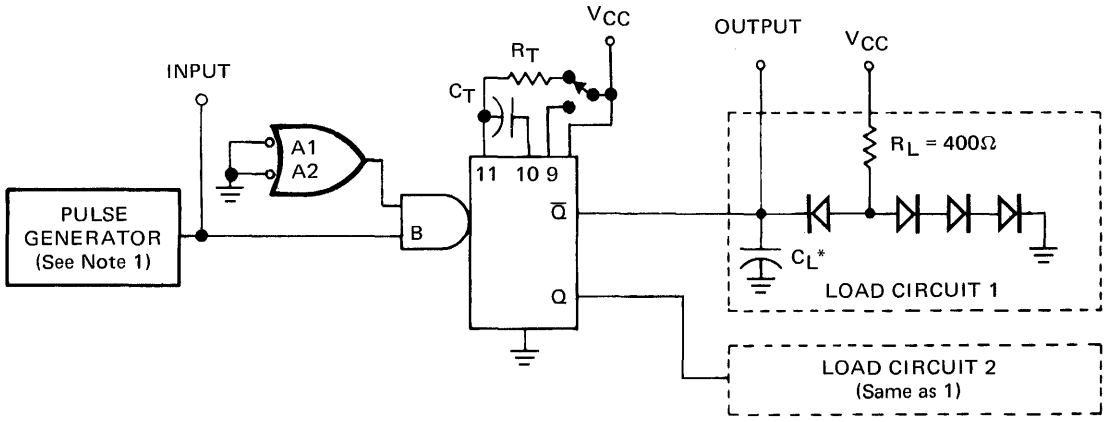
VOLTAGE WAVEFORMS

NOTE:
1. The pulse generator has the following characteristics: V_{gen} = 3.5 V, t_0 = 5 ns, t_1 = 10 ns, $t_p \geq$ 50 ns, PRR = 1 MHz, and $Z_{out} \approx 50\Omega$.

Fig. H 9N121/54121, 74121 SWITCHING TIMES

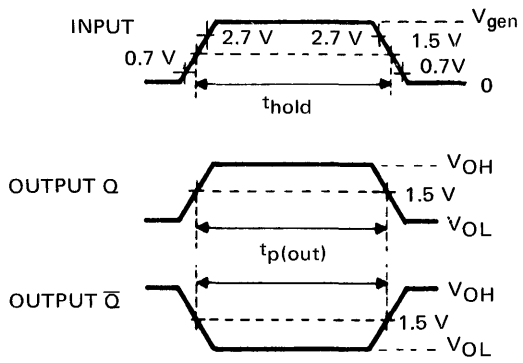
PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Continued)



*C_L includes probe and jig capacitance

TEST CIRCUIT



VOLTAGE WAVEFORMS

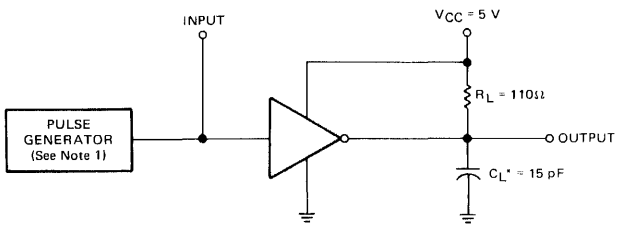
NOTE:

1. The pulse generator has the following characteristics: V_{gen} = 3.5 V, t_0 = 5 ns, t_1 = 10 ns, t_p = 50 ns, PRR = 1 MHz, and $Z_{out} \approx 50\Omega$.

Fig. I $t_{p(out)}$ (internal/minimum), t_{hold}

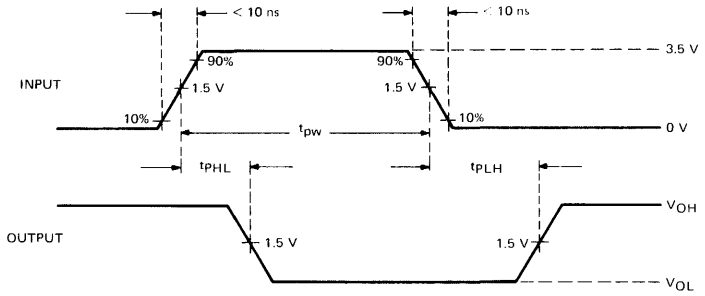
PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Continued)



*C_L includes probe and jig capacitance

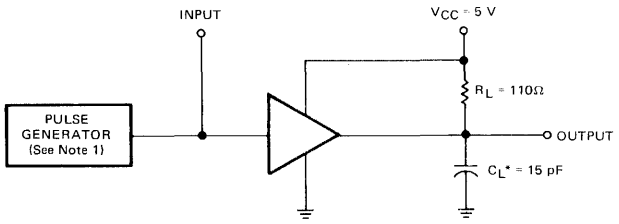
TEST CIRCUIT



VOLTAGE WAVEFORMS

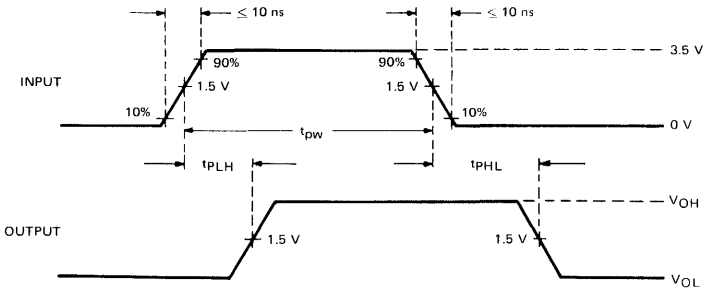
NOTE:
1. The generator has the following characteristics: t_{pw} = 0.5 μs, PRR = 1 MHz, $Z_{out} \approx 50\Omega$.

Fig. J PROPAGATION DELAY TIMES



*C_L includes probe and jig capacitance.

TEST CIRCUIT



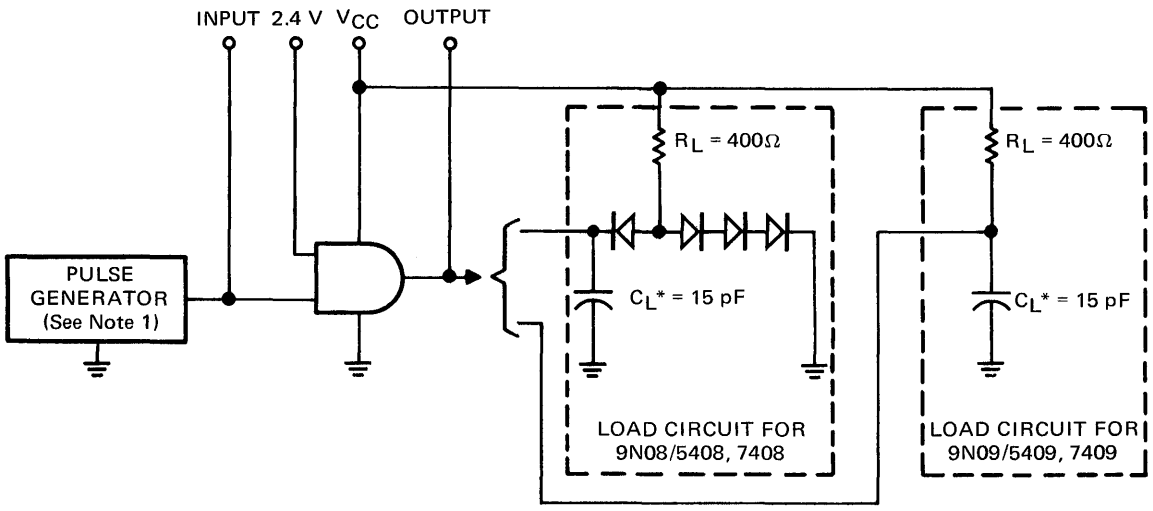
VOLTAGE WAVEFORMS

NOTE:
1. The generator has the following characteristics: t_{pw} = 0.5 μs, PRR = 1 MHz, $Z_{out} \approx 50\Omega$.

Fig. K PROPAGATION DELAY TIMES

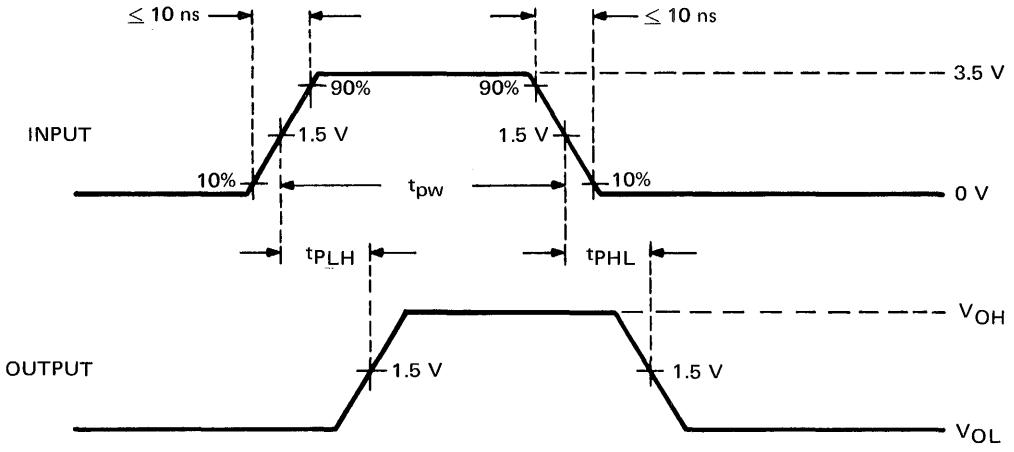
PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Continued)



*C_L includes probe and jig capacitance.

TEST CIRCUIT



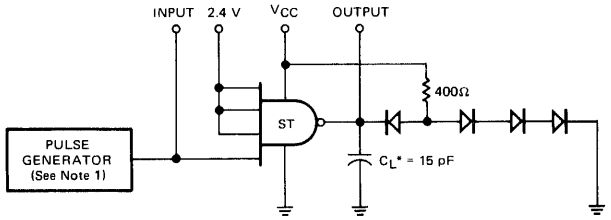
VOLTAGE WAVEFORMS

NOTE:
1. The generator has the following characteristics: t_{pw} = 0.5 μs, PRR = 1 MHz, $Z_{out} \approx 50\Omega$.

Fig. L PROPAGATION DELAY TIMES

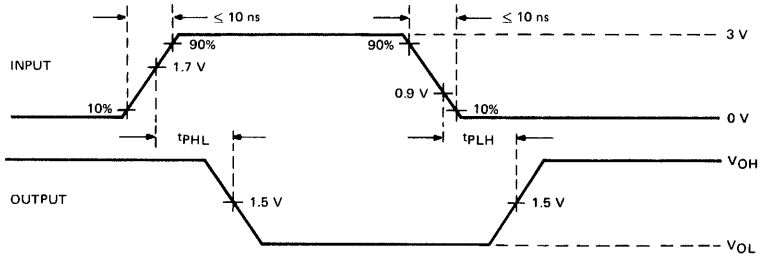
PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Continued)



*C_L includes probe and jig capacitance

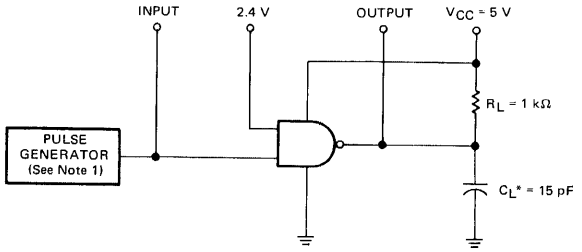
TEST CIRCUIT



VOLTAGE WAVEFORMS

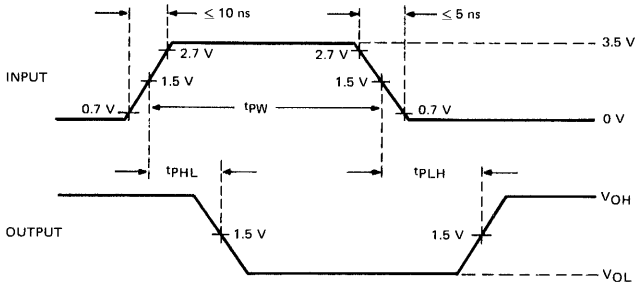
NOTE:
1. The pulse generator has the following characteristics: t_{pw} = 0.5 μs, PRR = 1 MHz, $Z_{out} \approx 50\Omega$.

Fig. M PROPAGATION DELAY TIMES



*C_L includes probe and jig capacitance.

TEST CIRCUIT



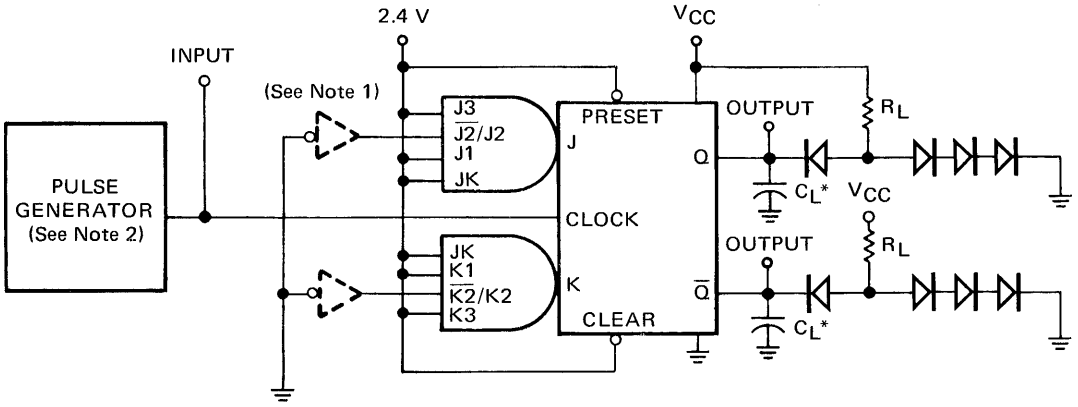
VOLTAGE WAVEFORMS

NOTE:
1. The generator has the following characteristics: t_{pw} = 0.5 μs, PRR = 1 MHz, $Z_{out} \approx 50\Omega$.

Fig. N PROPAGATION DELAY TIMES

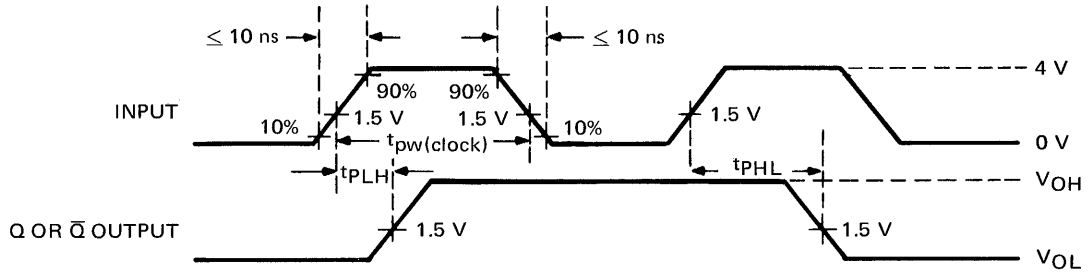
PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Continued)



*C_L includes probe and jig capacitance.

TEST CIRCUIT



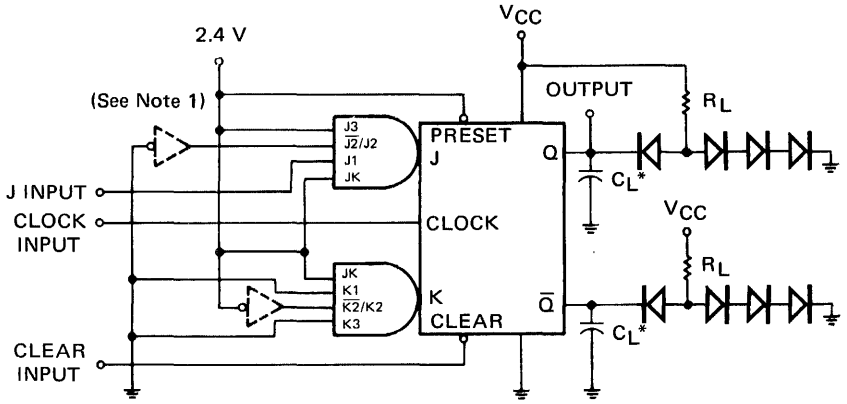
VOLTAGE WAVEFORMS

NOTES:
1. Test circuit shown is for the 9N105/54105, 74105. When testing 9N104/54104, 74104, the J2 and K2 inputs are connected in parallel with the other J and K inputs.
2. The pulse generator has the following characteristics: $t_{pw(clock)}$ = 250 ns, PRR = 1 MHz, $Z_{out} \approx 50\Omega$.

Fig. O PROPAGATION DELAY TIMES

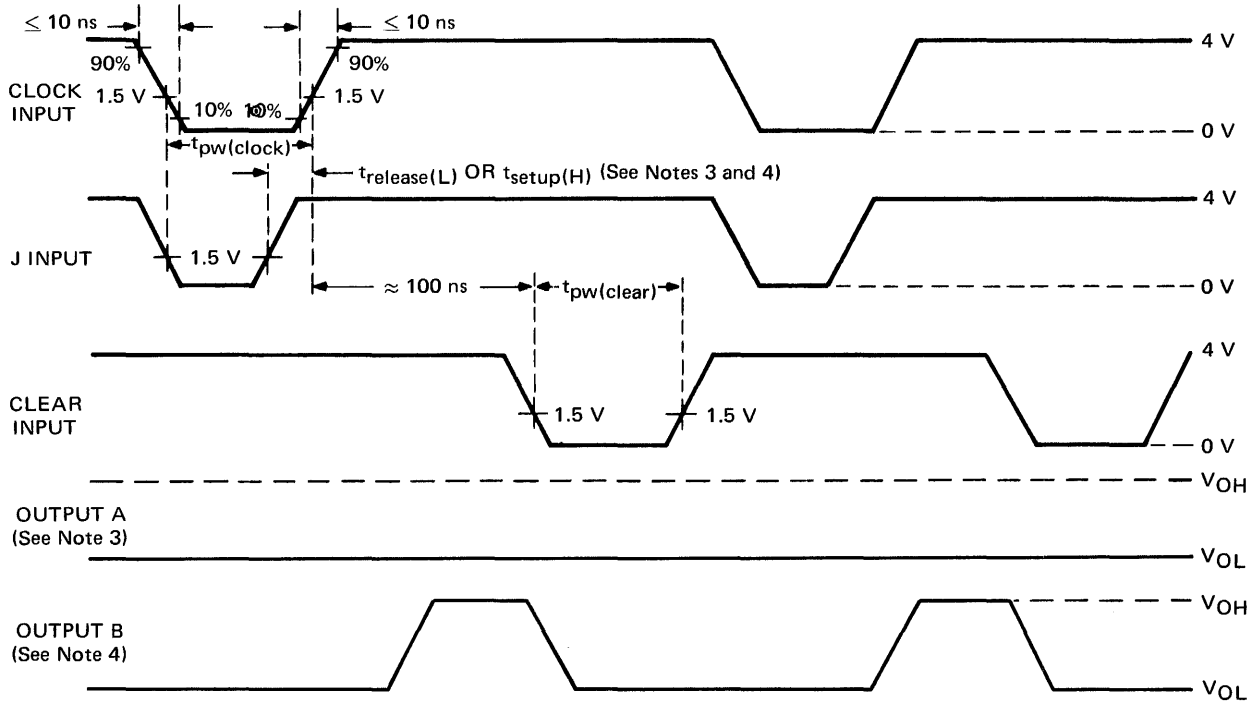
PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Continued)



*C_L includes probe and jig capacitance

TEST CIRCUIT



VOLTAGE WAVEFORMS

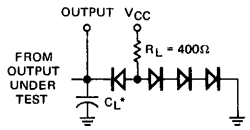
NOTES:

1. Test circuit shown is for the 9N105/54105, 74105. When testing 9N104/54104, 74104, the J2 input is connected in parallel with the other J inputs and K2 is grounded.
2. The input pulses have the following characteristics: PRR = 1 MHz, $t_{pw(clock)}$ = 100 ns, and $t_{w(clear)}$ = 100 ns. For duration of the J-input pulse, see Notes 3 and 4.
3. Output A is valid for: 9N104/54104, 74104, $t_{release(L)} \leq 10$ ns; 9N105/54105, 74105, $t_{release(L)} \leq 1$ ns.
4. Output B is valid for: 9N104/54104, 74104, $t_{setup(H)} \geq 35$ ns; 9N105/54105, 74105, $t_{setup(H)} \geq 10$ ns.

Fig. P INPUT SETUP/RELEASE TIMES

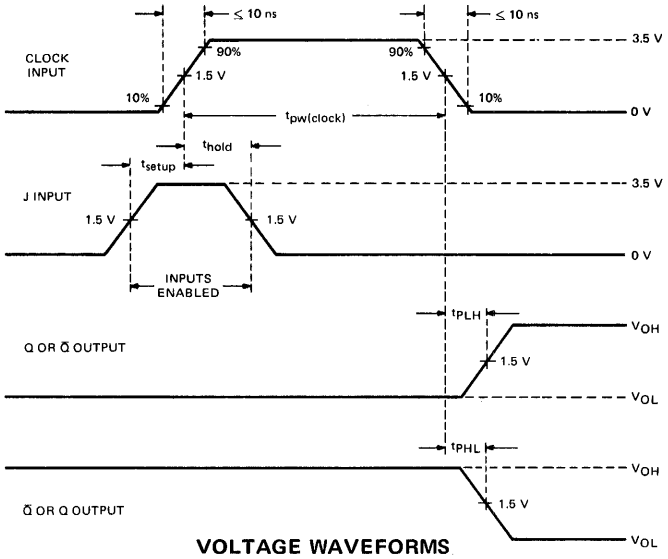
PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Continued)



*C_L includes probe and jig capacitance.

LOAD FOR OUTPUT UNDER TEST

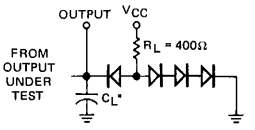


VOLTAGE WAVEFORMS

NOTE:

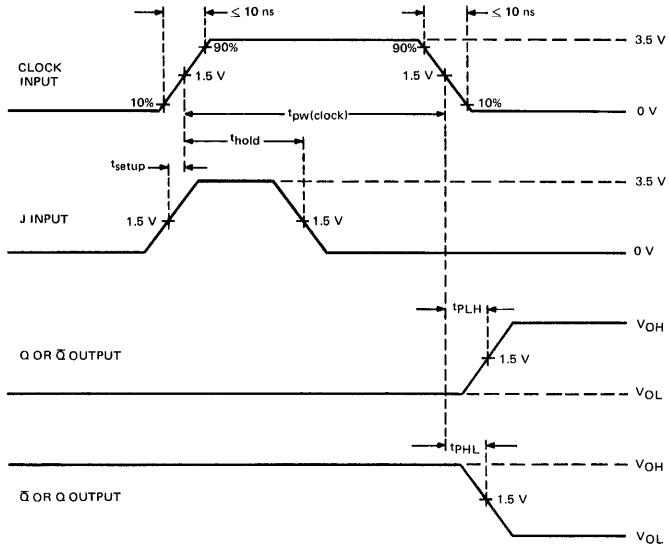
1. Both input pulses are supplied by generators with the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\Omega$. Clock duty cycle = 50%.

Fig. Q



*C_L includes probe and jig capacitance.

LOAD FOR OUTPUT UNDER TEST



VOLTAGE WAVEFORMS

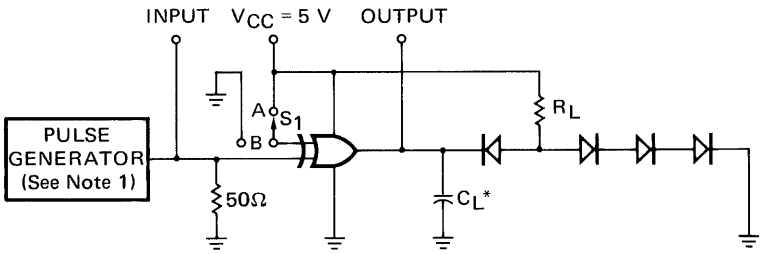
NOTE:

1. Both input pulses are supplied by generators with the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\Omega$, clock duty cycle = 50%.

Fig. R

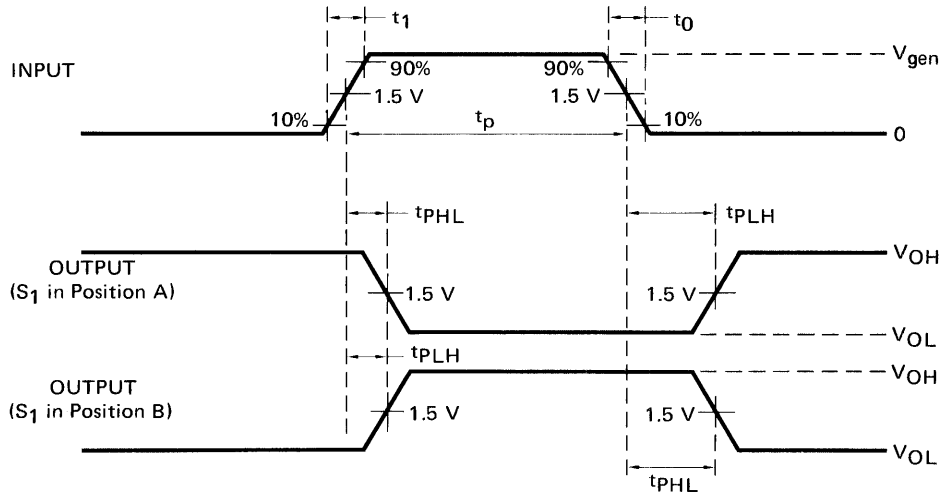
PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Continued)



*C_L includes probe and jig capacitance

TEST CIRCUIT



VOLTAGE WAVEFORMS

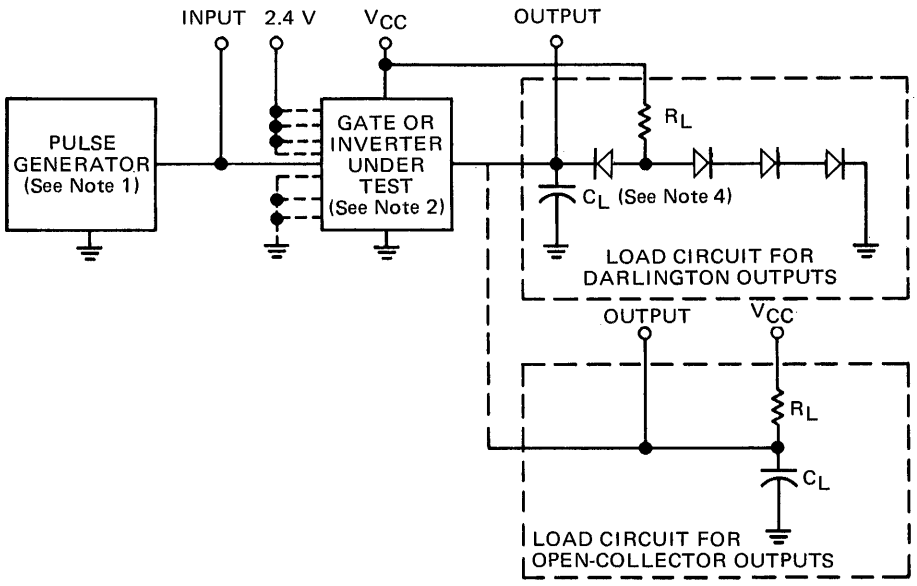
NOTES:

1. The generator has the following characteristics: V_{gen} = 3.0 V, $t_0 = t_1 \leq 15$ ns t_p = 0.5 μs, PRR = 1 MHz, $Z_{out} \approx 50\Omega$.
2. Propagation Delay = $\frac{t_{PHL} + t_{PLH}}{2}$
3. Each gate tested separately.

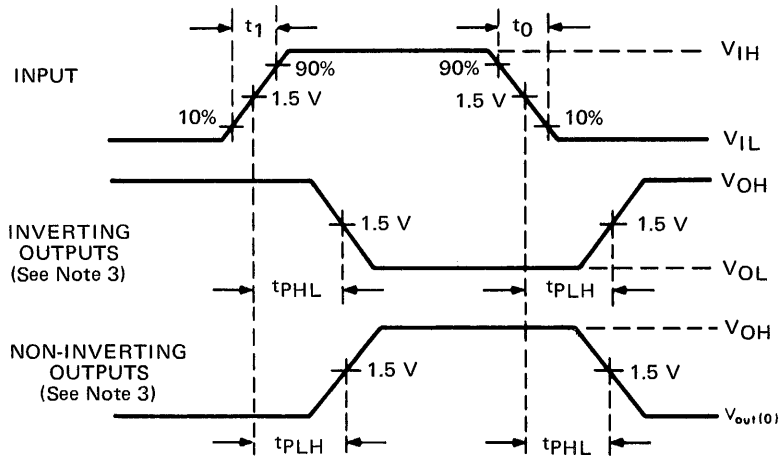
Fig. S

PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS



TEST CIRCUIT



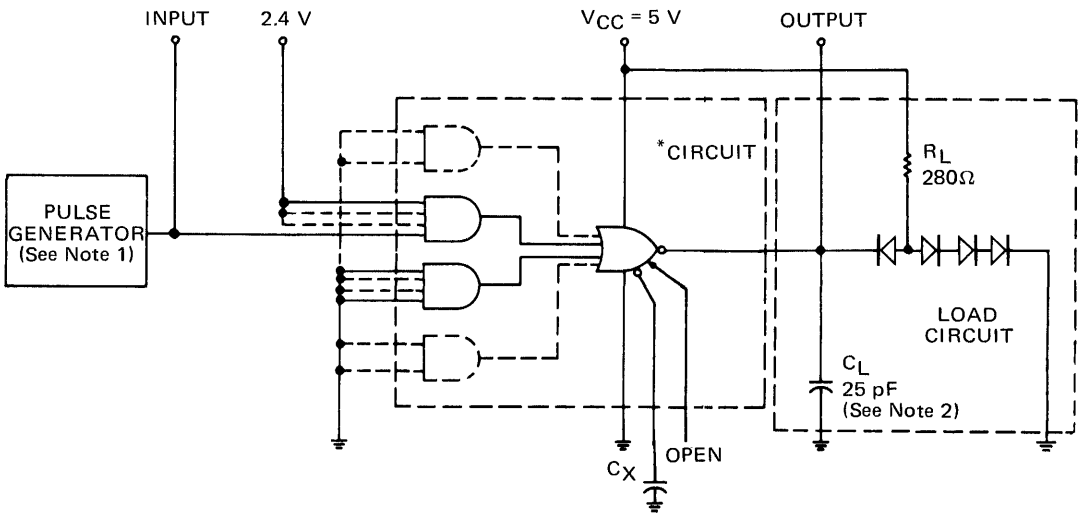
VOLTAGE WAVEFORMS

NOTES:
1. The pulse generator has the following characteristics: V_{IH} = 3 V, V_{IL} = 0 V, $t_1 = t_0$ = 7 ns, PRR = 1 MHz, duty cycle = 50%, and $Z_{OUT} \approx 50\Omega$.
2. Input conditions are established for each gate as follows:
   a. Input pulse is applied to one input and 2.4 V is applied to all unused inputs of the 9H00/54H00, 74H00; 9H01/54H01, 74H01; 9H04/54H04, 74H04; 9H05/54H05, 74H05; 9H10/54H10, 74H10; 9H11/54H11, 74H11; 9H20/54H20, 74H20; 9H21/54H21, 74H21; 9H22/54H22, 74H22; 9H30/54H30, 74H30; or 9H40/54H40, 74H40 gate.
   b. Input pulse is applied to one input of one AND section, and 2.4 V is applied to all unused inputs of that AND section of the 9H50/54H50, 74H50; 9H51/54H51, 74H51; 9H52/54H52, 74H52; 9H53/54H53, 74H53; 9H54/54H54, 74H54; or 9H55/54H55, 74H55 gate. All inputs of all unused AND sections are grounded.
3. All gates are inverting except the 9H11/54H11, 74H11; 9H21/54H21, 74H21; and 9H52/54H52, 74H52 only.
4. C_L includes probe and jig capacitance.

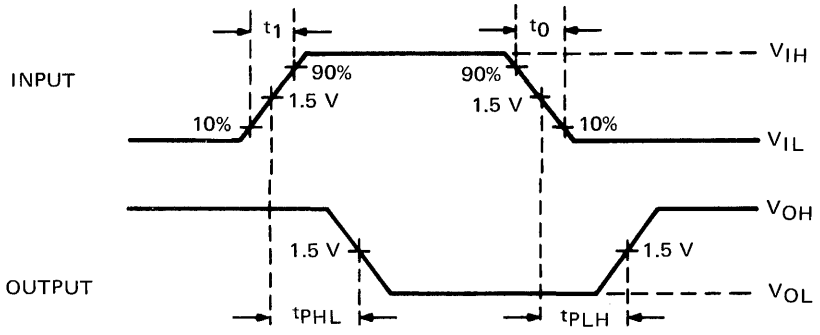
Fig. T GATE PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

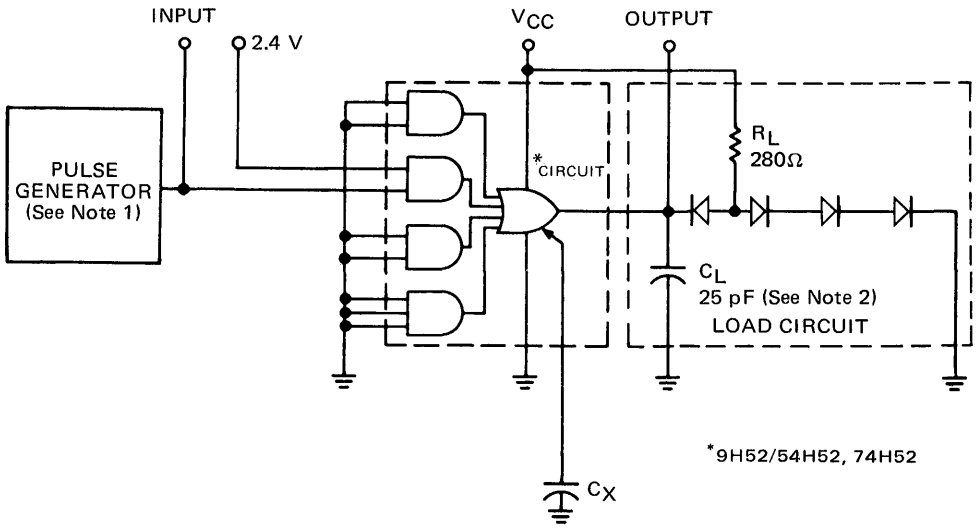
NOTES:
1 The generator has the following characteristics: V_{IH} = 3 V, V_{IL} = 0 V, $t_0 = t_1$ = 7 ns, duty cycle = 50%, PRR = 1 MHz $Z_{OUT} \approx 50\Omega$.
2 C_L includes probe and jig capacitance
3 C_X includes jig capacitance.

*9H50/54H50, 74H50; 9H53/54H53, 74H53; 9H55/54H55, 74H55

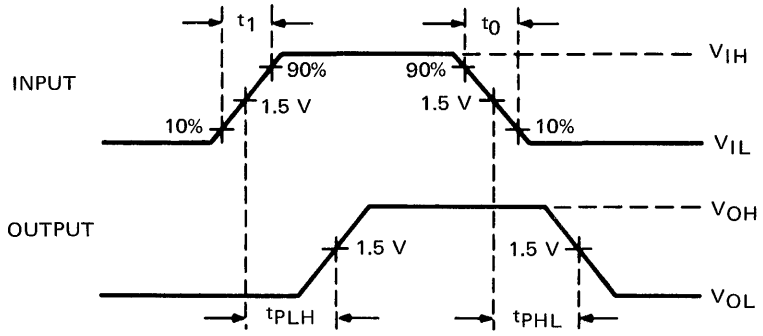
Fig. U PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Continued)



TEST CIRCUIT



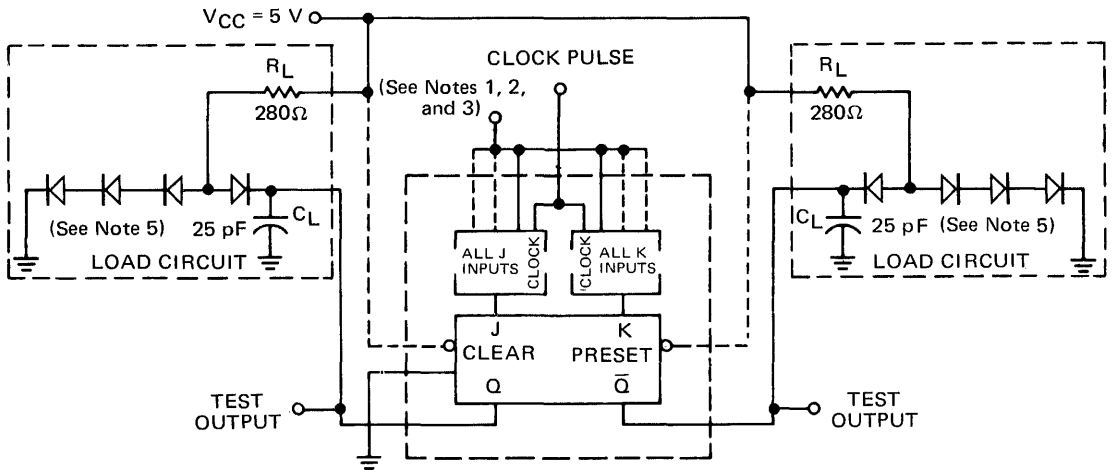
VOLTAGE WAVEFORMS

NOTES:
1. The generator has the following characteristics: V_{IH} = 3 V, V_{IL} = 0 V, $t_0 = t_1$ = 7 ns, duty cycle = 50%, PRR = 1 MHz, $V_{OUT} \approx 50\Omega$.
2. C_L includes probe and jig capacitance.
3. C_X includes jig capacitance.

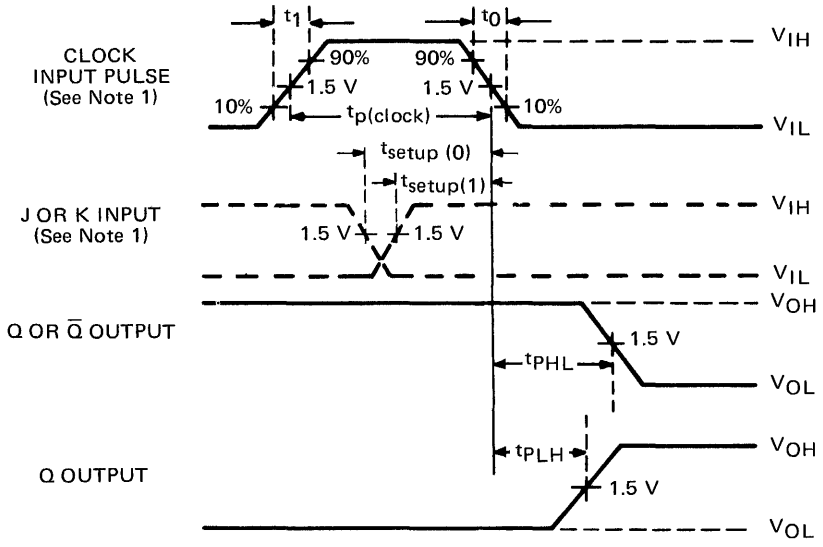
Fig. V PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

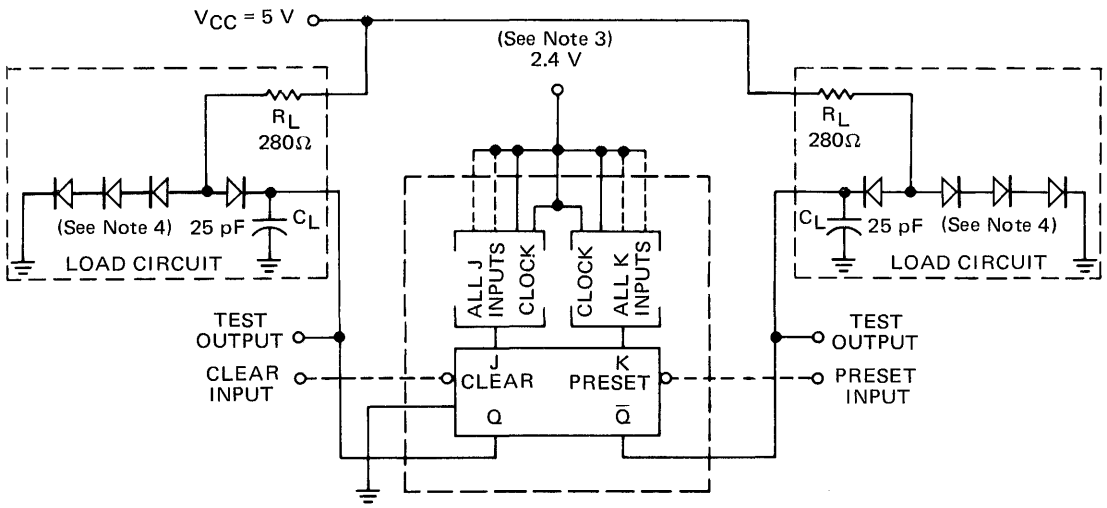
NOTES:

1. When testing t_{PHL} and t_{PLH} (all types), the clock input pulse characteristics are: V_{IH} = 3 V, V_{IL} = 0 V, $t_1 = t_0$ = 7 ns, $t_{p(clock)}$ = 20 ns, and PRR = 1 MHz. When testing 9H71/54H71, 74H71; 9H72/54H72, 74H72; 9H73/54H73, 74H73; 9H76/54H76, 74H76 and 9H78/54H78, 74H78 all J and K inputs are at 2.4 V. When testing 9H101/54H101, 74H101; 9H102/54H102, 74H102; 9H103/54H103, 74H103; 9H106/54H106, 74H106 and 9H108/54H108, 74H108 conditions are established to ensure that minimum setup times are verified.
2. When testing f_{clock} of 9H71/54H71, 74H71; 9H72/54H72, 74H72; 9H73/54H73, 74H73; 9H76/54H76, 74H76 and 9H78/54H78, 74H78, the clock input characteristics are: V_{IH} = 3 V, V_{IL} = 0 V, $t_1 = t_0$ = 3 ns, $t_{p(clock)}$ = 12 ns, and PRR = 25 MHz. All J and K inputs are at 2.4 V.
3. When testing f_{clock} of 9H101/54H101, 74H101; 9H102/54H102, 74H102; 9H103/54H103, 74H103; 9H106/54H106, 74H106 and 9H108/54H108, 74H018, the clock input characteristics are: V_{IH} = 3 V, V_{IL} = 0, $t_1 = t_0$ = 3 ns, $t_{p(clock)}$ = 10 ns and PRR = 40 MHz. All J and K inputs are at 2.4 V.
4. See applicable circuit type for actual J and K input configuration and presence of preset or clear functions.
5. C_L includes probe and jig capacitance.

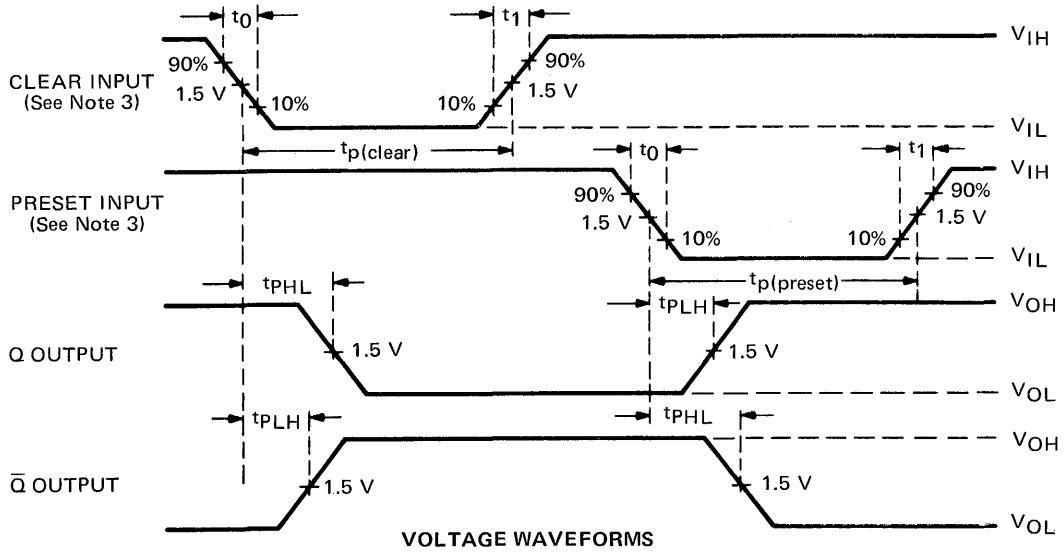
Fig. W FLIP-FLOP PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Continued)



TEST CIRCUIT



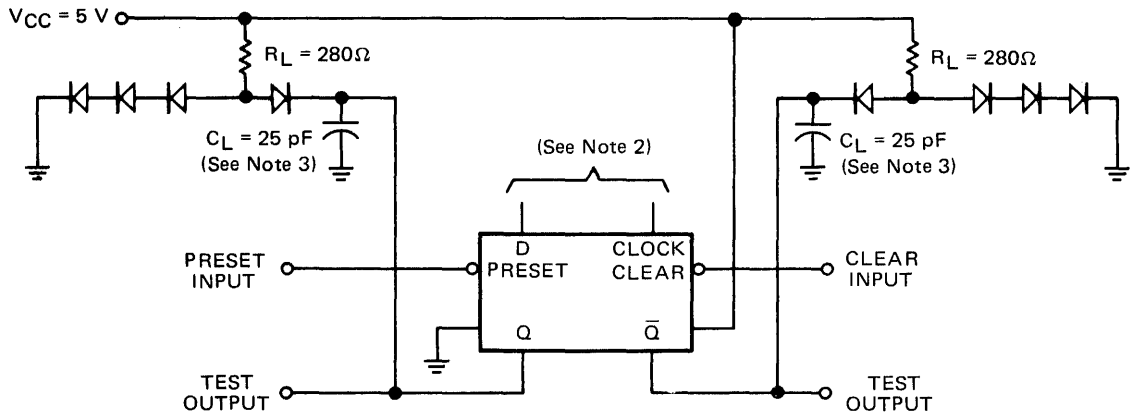
VOLTAGE WAVEFORMS

NOTES:
1 Clear or Preset inputs dominate regardless of the state of Clock or J-K inputs.
2 Clear or Preset input pulse characteristics: V_{IH} = 3 V, V_{IL} = 0 V, $t_1 = t_0$ = 7 ns, $t_{p(clear)} = t_{p(preset)}$ = 16 ns, and PRR = 1 MHz.
3 See applicable circuit type for actual J and K input configuration and presence of Preset or Clear functions.
4 C_L includes probe and jig capacitance.

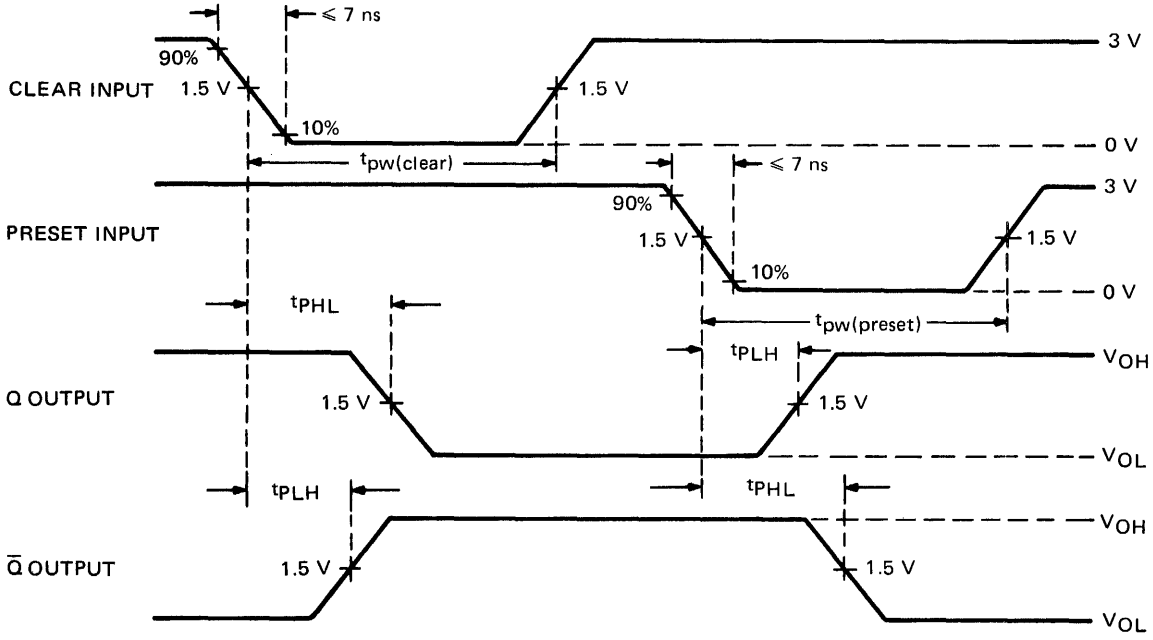
Fig. X FLIP-FLOP PRESET/CLEAR PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Continued)



TEST CIRCUIT



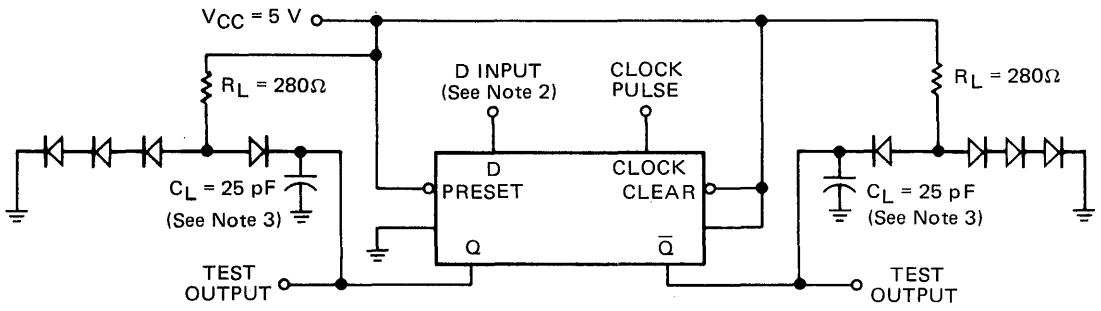
VOLTAGE WAVEFORMS

NOTES:
1 Clear or Preset input pulse characteristics: $t_{pw(clear)} = t_{pw(preset)}$ = 25 ns, PRR = 1 MHz.
2 Clear and Preset inputs dominate regardless of the state of Clock or D inputs.
3 C_L includes probe and jig capacitance.

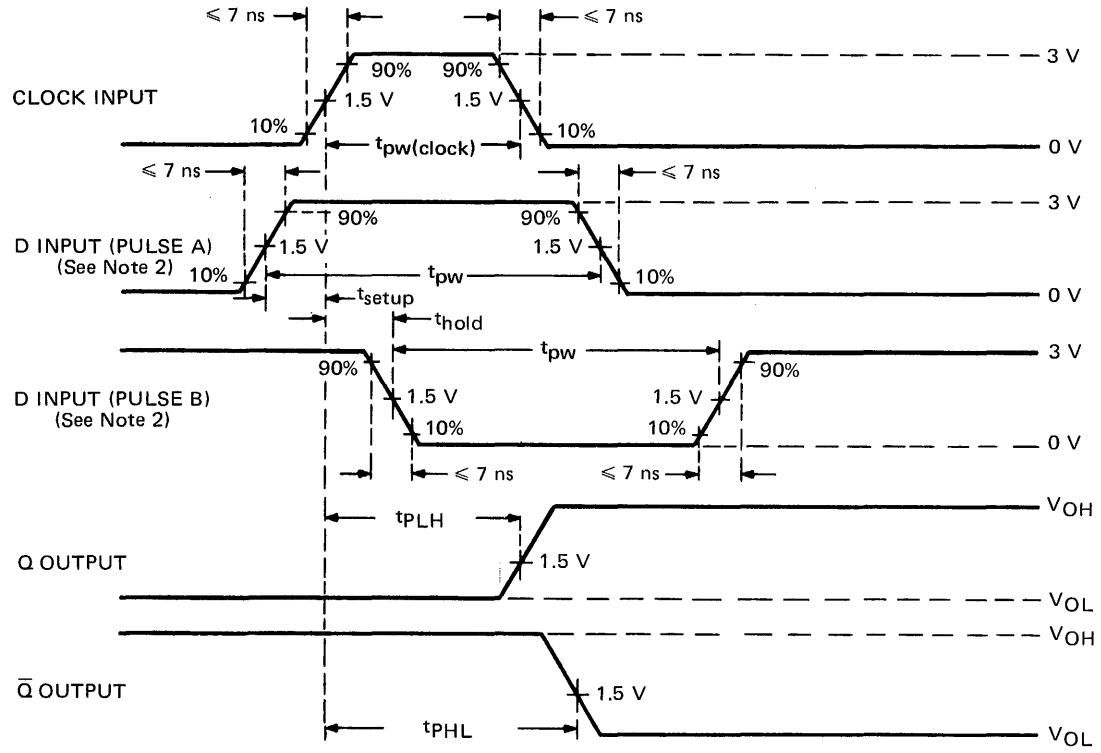
Fig. Y ASYNCHRONOUS INPUTS SWITCHING CHARACTERISTICS

PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Continued)



TEST CIRCUIT



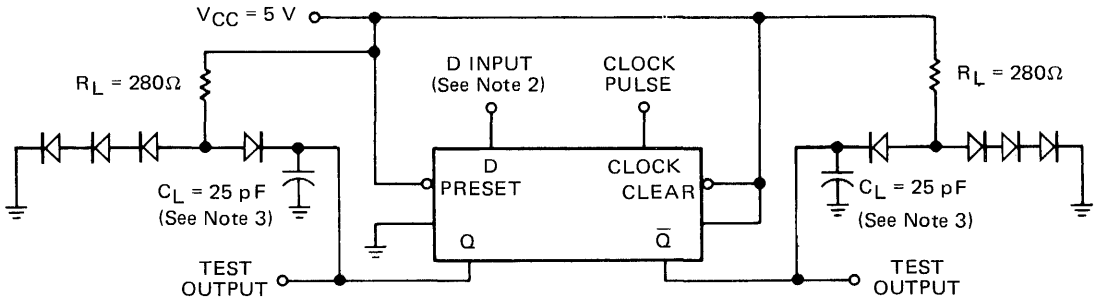
VOLTAGE WAVEFORMS

NOTES:
1. Clock input pulse has the following characteristics: $t_{pw(clock)}$ = 20 ns and PRR = 1 MHz. When testing f_{clock}, vary PRR.
2. D input (pulse A) has the following characteristics: t_{setup} = 10 ns, t_{pw} = 60 ns, and PRR is 50% of the clock PRR. D input (pulse B) has the following characteristics: t_{hold} = 0 ns, t_{pw} = 60 ns, and PRR is 50% of the clock PRR.
3. C_L includes probe and jig capacitance.

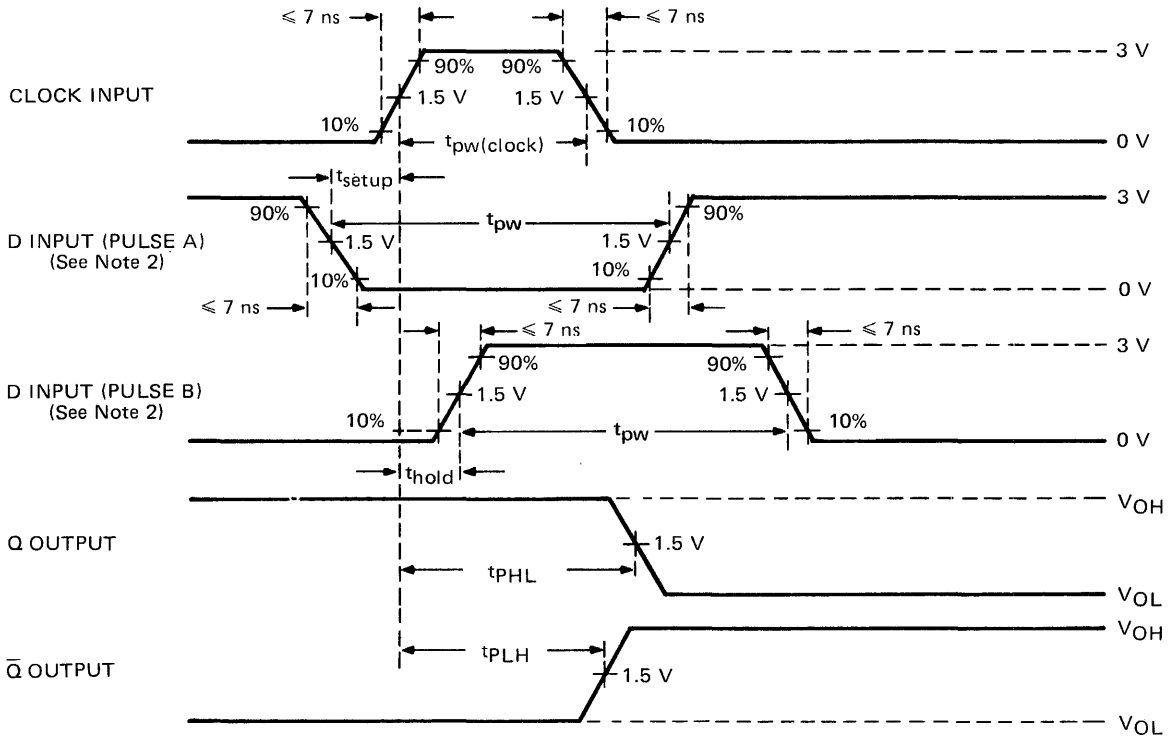
Fig. Z SWITCHING CHARACTERISTICS, CLOCK AND SYNCHRONOUS INPUTS (HIGH-LEVEL DATA)

PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Continued)



TEST CIRCUIT



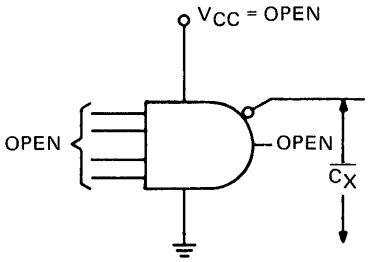
VOLTAGE WAVEFORMS

NOTES:
1. Clock input pulse has the following characteristics: t_{pw} = 20 ns and PRR = 1 MHz. When testing f_{clock}, vary PRR.
2. D input (pulse A) has the following characteristics: t_{setup} = 15 ns, t_{pw} = 60 ns, and PRR is 50% of the clock PRR. D input (pulse B) has the following characteristics: t_{hold} = 0 ns, t_{pw} = 60 ns, and PRR is 50% of the clock PRR.
3. C_L includes probe and jig capacitance.

Fig. AA SWITCHING CHARACTERISTICS, CLOCK AND SYNCHRONOUS INPUTS (LOW-LEVEL DATA)

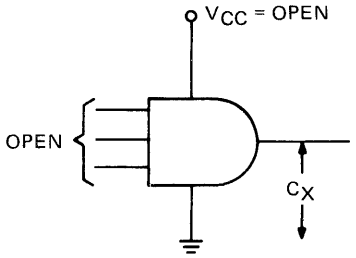
PARAMETER MEASUREMENT INFORMATION

SWITCHING TIME DATA TEST CIRCUITS



1. Each output is tested separately.

Fig. BB

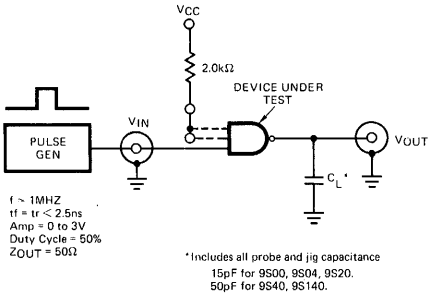


1. Each output is tested separately.

Fig. CC

SWITCHING CHARACTERISTICS

TEST CIRCUIT AND WAVEFORM FOR 9S00, 9S04, 9S20, 9S40 AND 9S140



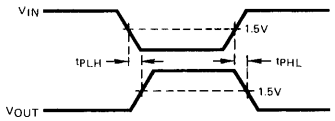
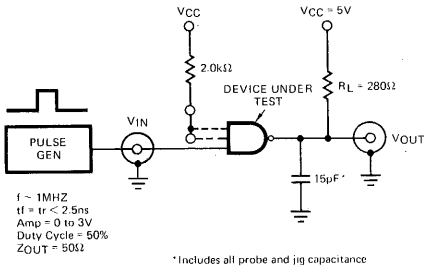


Fig. DD

TEST CIRCUIT AND WAVEFORM FOR 9S03, 9S05 AND 9S22



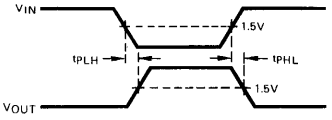
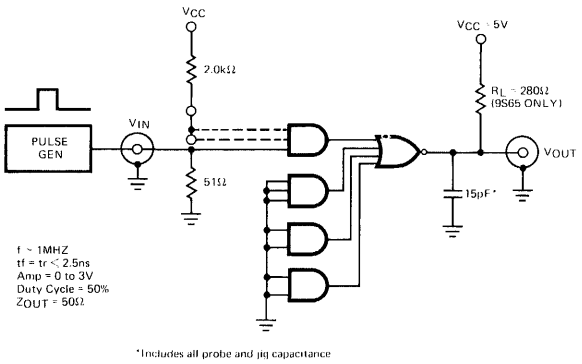


Fig. EE

SWITCHING CHARACTERISTICS (cont.)

TEST CIRCUIT AND WAVEFORM FOR 9S64, 9S65



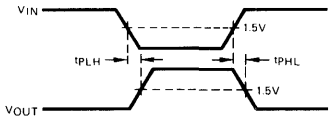


Fig. FF

TYPICAL CHARACTERISTICS

ADDED PROPAGATION DELAY TIME vs EXPANDER-NODE CAPACITANCE

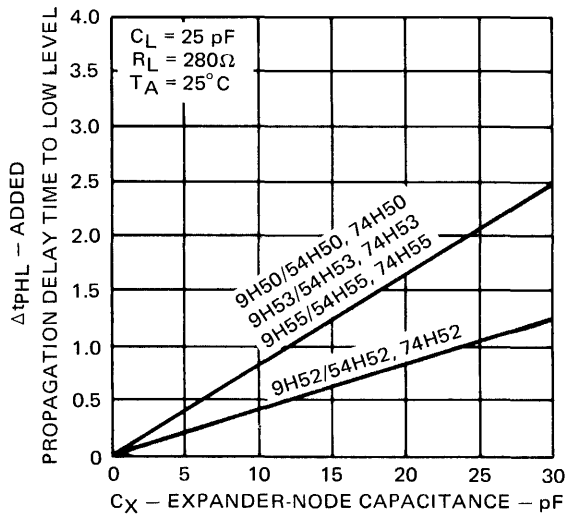


Fig. MM

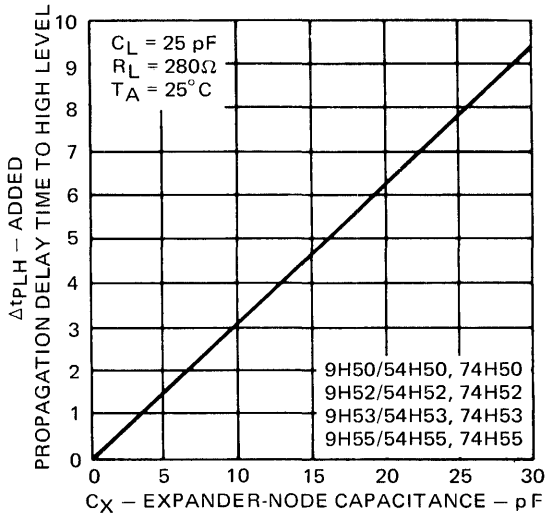


Fig. NN