FEATURES

- Single-chip IBM® Personal System/2® MCA Interface Chip for the Micro Channel conserves space, saves power, lowers board cost, lowers board failure rate, and simplifies development of add-on boards by decreasing design time and effort
- Provides full interface for IBM Personal System/2 models that implement the Micro Channel™ bus architecture; 100% compatible with IBM's Micro Channel specification
- Requires only one external data transceiver chip and a POS (Programmable Option Select) identification device, leaving 94% of Personal System/2 adapter board space for user circuits
- Low power HCMOS technology requires only 100mA (max) of +5V power
- Complete DMA interface
  - Two complete, independent DMA controllers for simultaneous operation on two channels
  - Individual POS-programmable arbitration level and Fairness for each channel
  - Burst mode DMA performs at least 1 to 8 transfers per bus grant
- POS interface included, with programmable I/O base address and six bits for user-assigned adapter configuration options
- Synchronous or asynchronous extended command cycles provide flexible adapter timing

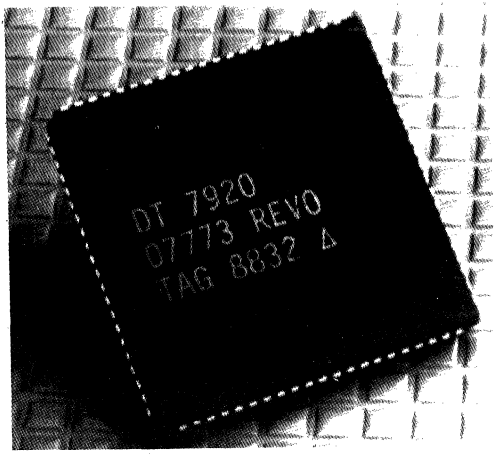

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Figure 1. The DT7920 MCA Interface Chip contains virtually all the interface circuitry required for a Micro Channel adapter in a single 84-pin PLCC.

- 84-pin PLCC (Plastic Leaded Chip Carrier) package for socket or surface mounting
- Available with Development Board (DT2981) for adapter prototype development

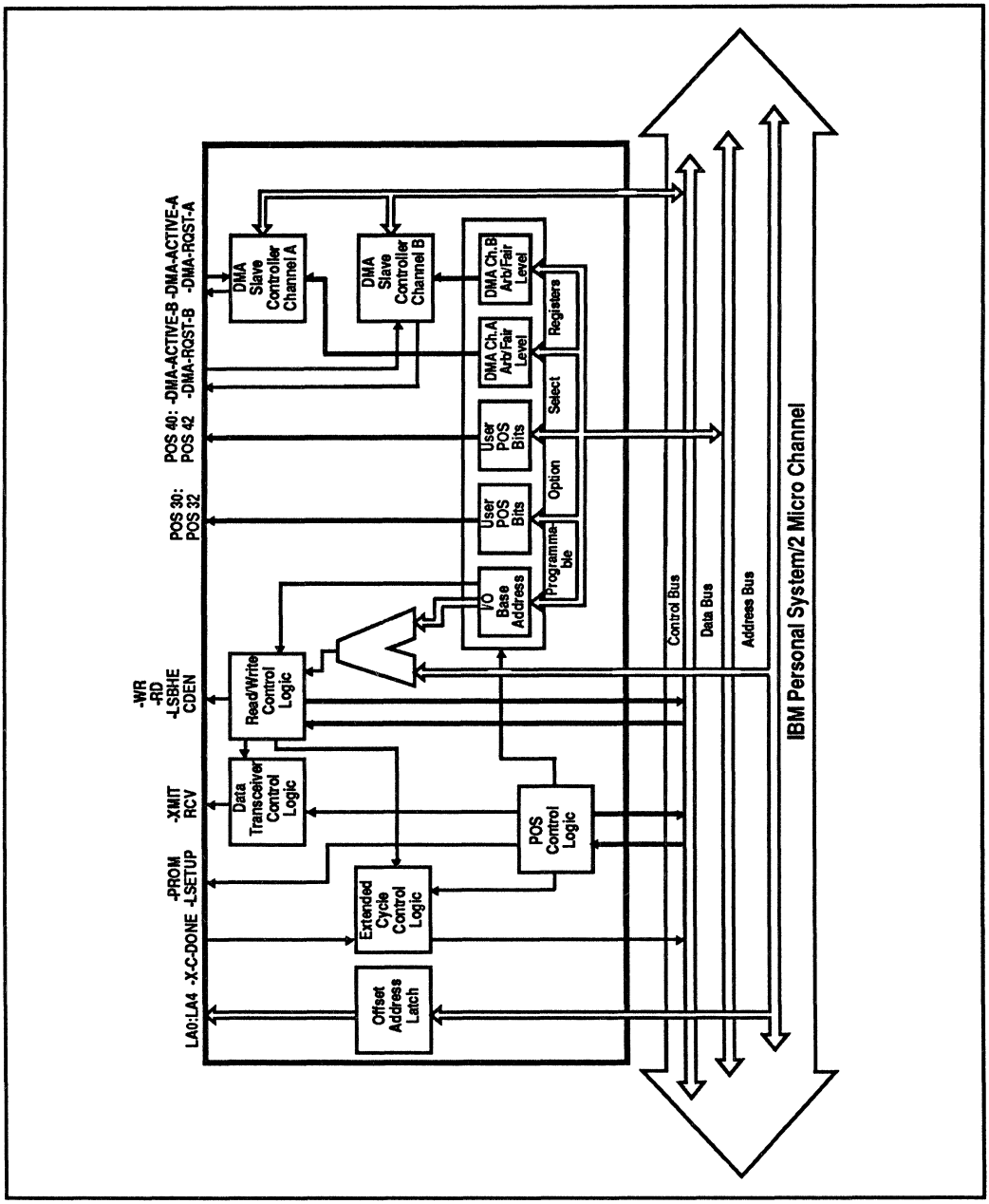

Figure 2. DT7920 Block Diagram

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GENERAL DESCRIPTION

The DT7920 MCA Interface Chip is an HCMOS integrated circuit that contains virtually all the interface circuitry required for IBM Personal System/2 Micro Channel add-on boards and peripheral controllers. Designed to save Micro Channel adapter designers time, board space, cost, and power, the DT7920 leaves 34 square inches (of 36 square inches) of the Micro Channel board area and over 90% of allotted power for adapter designs.

The DT7920 requires only one external data transceiver chip and a POS identification device to perform all Micro Channel interface functions for a DMA adapter. The DT7920 contains POS registers, decodes and drives address lines directly, and controls data transfers to and from the Micro Channel, in addition to decoding, driving, and interfacing with key bus control lines.

DMA OPERATION

The DT7920 contains complete control circuitry for two independent DMA channels. Arbitration level and Fairness are set independently for each channel via POS registers. I/O base address of the adapter is also POS-selected. The DT7920 reserves 32 contiguous I/O locations, permitting the adapter designer to create up to 16 16-bit (32 8-bit) input, output, or I/O registers to control adapter operations. Control lines are made available to the adapter designer to initiate a DMA request and to terminate it.

Each of the DT7920's DMA channels is designed for Burst Mode operation, although single DMA transfers can also be accommodated. Once the DT7920 receives DMA channel control, it allows the adapter to transfer from one to eight data values in Burst Mode. At the end of eight transfers, the DT7920 looks at the bus to see if any other adapter is seeking control. If so, the DT7920 goes through another arbitration/Fairness cycle. If not, the DT7920 transfers another one to eight data values. The DT7920 thus handles Micro Channel arbitration and Fairness operations, requiring only that the adapter keep the DMA request active as long as there is data to be transferred.

If single DMA transfers only will be performed, Burst Mode can be disabled and the DT7920 is fully compatible with the Personal System/2 Single Transfer DMA operations.

The DT7920 provides six user-definable POS bits. These are defined and brought out on DT7920 pins to control adapter functions defined by the user. The DT7920 also supports extended command cycles, either synchronous with -CMD or asynchronous, to match adapter timing to Micro Channel command cycles.

DUAL DMA CHANNELS

The DT7920's dual DMA channels support a variety of sophisticated adapter designs. First, two DMA channels support multiple functions on a single adapter (such as a printer port and an RS-232-C port). This DMA architecture also supports adapters that require simultaneous input and output such as analog and digital I/O, or simultaneous input and output communications for IEEE 488 or RS-232-C interfaces.

Two DMA channels also allow real-time continuous data transfers in an environment plagued by system latencies and overhead. The Personal System/2 can process DMA transfers up to a maximum of 64 Kwords per DMA controller. Upon completing transfers to or from a buffer, the DMA controller must be reprogrammed for the next transfer—an operation that can halt data transfers for hundreds of microseconds. With dual DMA channels two controllers can be used at once. At the end of one buffer, data transfers are simply directed to the second controller while the first controller is reprogrammed.

SEPARATE DATA BUS

The DT7920 provides signals to implement a separate data bus on the adapter, thus isolating the adapter's data lines from the Micro Channel. This keeps the Micro Channel data lines from inducing noise on the adapter, by allowing the Micro Channel data lines to be connected to the adapter's data bus only when

data is actually being transferred by the adapter to or from the Micro Channel. When the adapter is not being addressed, the Micro Channel data lines are disconnected from the adapter's internal data bus, and system noise is kept away from adapter circuitry. This can be especially beneficial to adapters using noise-sensitive analog circuits, where bus noise can propagate over the board.

DT2981 DEVELOPMENT BOARD

The DT7920 can be ordered with a Micro Channel-compatible prototype development board to further speed adapter development. The DT2981 consists of a circuit board, a DT7920 and socket, data transceivers, a POS ID device and socket, startup software including an Adapter Description File (ADF), a 50-pin I/O connector, and a large breadboard area to develop adapter circuits. All user signals are provided on wirewrap pins for easy user access.

DT7920 OPERATIONS

The following sections describe the use of the DT7920. Discussions cover Micro Channel bus connections, POS register functions, PIO and DMA operations, and extended command cycles.

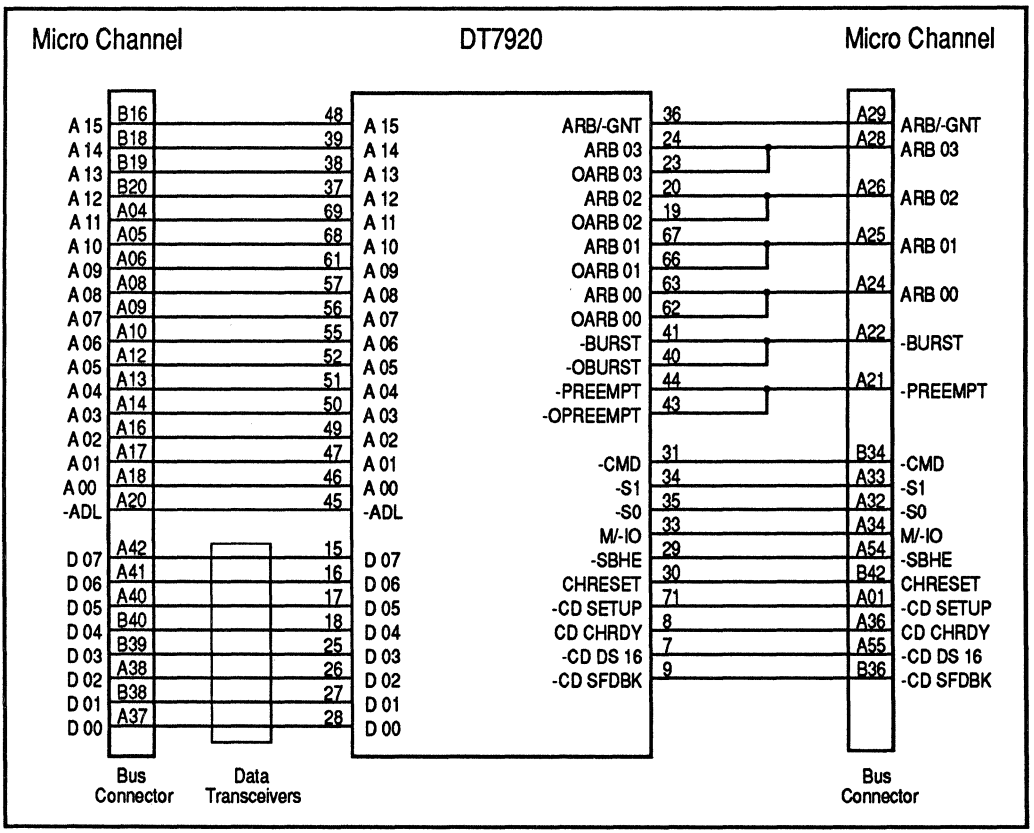

Figure 3. DT7920 Bus Connections

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DT7920 CONNECTIONS

Many DT7920 signals are designed for direct connection to the Micro Channel bus. Others require some external circuitry for bus interface or chip operation. Data transceivers are required to provide an interface to the Micro Channel data lines. In addition, an external ID device (PROM, ROM, or PAL) is required to provide setup information.

Bus Connections

Various signals in the DT7920 are normally connected to signals on the Micro Channel. Figure 3 summarizes these connections.

DATA TRANSCEIVERS

In I/O operations, the DT7920 gates data to and from the Micro Channel using outputs RCV (Receive, pin 54) and -XMIT (-Transmit, pin 79). Figure 4 shows how these signals are implemented to control 74ALS623 transceivers.

By generating both RCV and -XMIT signals, the DT7920 implements an internal adapter data bus that isolates the adapter from noise caused by data bus activity on the Micro Channel bus. The internal bus connects to the Micro Channel bus only when RCV or -XMIT

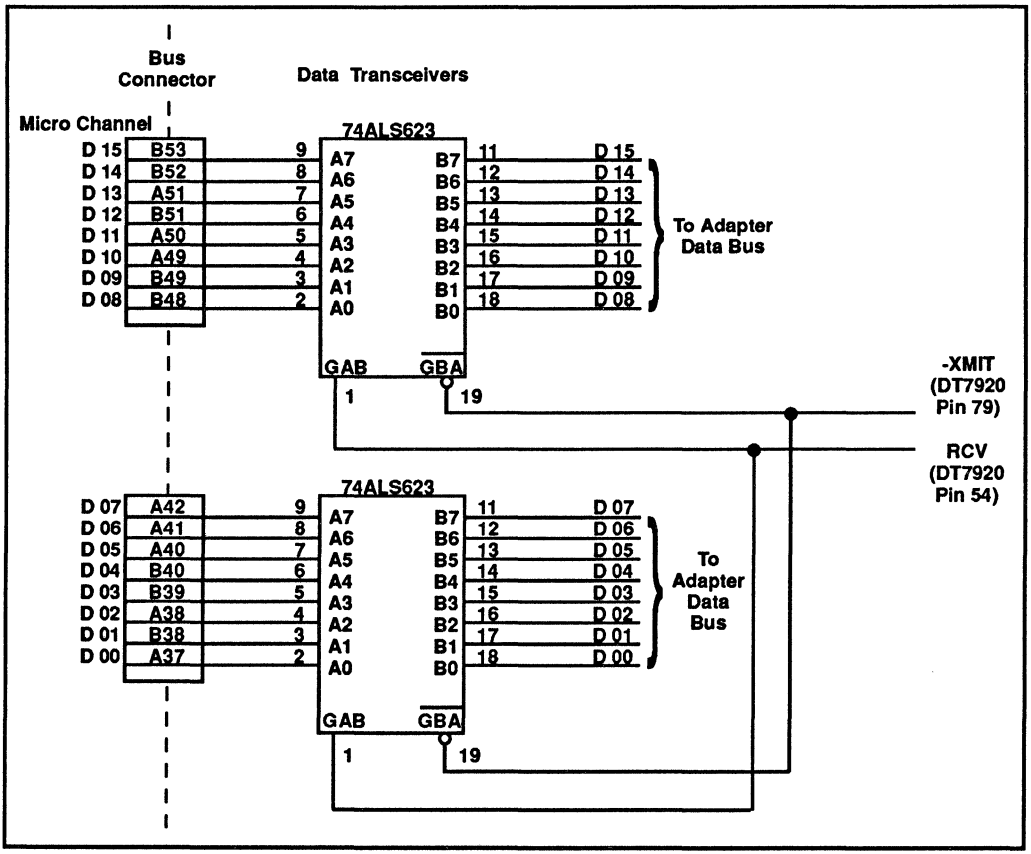

Figure 4. DT7920 signals RCV and -XMIT gate data on and off the Micro Channel bus.

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is asserted—that is, only when data is being read from or written to the Micro Channel bus. At other times, the Micro Channel data lines are disconnected from the adapter's data bus, and system noise is kept away from adapter circuitry.

PROGRAMMABLE OPTION SELECT

The IBM Personal System/2's Programmable Option Select (POS) is intended to eliminate switches and jumpers from adapters by replacing their functions with programmable registers. The Personal System/2's system configuration utility obtains adapter information from Adapter Description Files and uses I/O addresses hex 0100 through 0107 in Setup Mode to address the POS bytes of an adapter.

POS locations hex 0100 and 0101 must read back an adapter ID when addressed during system Setup Mode. This occurs when the Personal System/2 computer system is configured, and again for verification each time the system is powered up. The file name for each Adapter Description File contains a unique 16-bit board ID that corresponds to the board ID generated by the adapter. Each channel position is allocated two bytes for each board ID and four bytes for POS data.

External Identification Device

The DT7920 signal -PROM (-PROM Enable, pin 72) is used to enable a user-supplied programmable read-only device that contains the adapter ID. Latched address output bits LA0 to LA2 (DT7920 pins 14:12) select locations in the external identification device, while data is transferred to the Micro Channel bus via data transceivers. In addition to the board ID, the external identification device can be used to store adapter revision information, date codes, or other user-defined information. Figure 5 shows circuit connections to a typical identification device.

POS Registers

The POS is made up of eight 8-bit registers. The registers are byte-accessible only and must be accessed in the Setup Mode as selected when the slot-specific -CD SETUP line is asserted. Each Micro Channel adapter slot has its own -CD SETUP signal.

The DT7920 contains POS locations hex 0102, 0103, and 0104. The chip's POS interface circuitry permits selection of adapter I/O base address, of adapter card enable, and of arbitration level and Fairness enable for two DMA channels. Six bits (POS locations hex 0103 and 0104, bits 0:2) are left for user-programmable features. These bits are associated with signals POS30, POS31, and POS32 (pins 4:2); and with signals POS40, POS41, and POS42 (pins 58:60). The adapter designer can use these register locations and signals to implement user-selectable options on the adapter.

POS locations hex 0100, 0101, 0105, 0106, and 0107 are not implemented in the DT7920, but are directed to an external read-only identification device, such as a PROM, PAL, or ROM. When the adapter is selected by the -CD SETUP signal, the least significant three address lines (address inputs A 00, A 01, and A 02; pins 46, 47, and 49) are transparently latched in the chip on -ADL (-Address Decode Latch, pin 45) and provided as outputs via signals LA0 to LA2 (Latched Address outputs, pins 12:14) along with the signal -PROM (-PROM Enable, pin 72).

Table 1 summarizes the DT7920's implementation of POS registers.

POS 0100:0101–Adapter Identification

Bytes at POS locations hex 0100 and 0101 comprise the Adapter Identification field for any particular adapter design. An adapter identification is a 16-bit code available from IBM which uniquely identifies an adapter. The Personal System/2 BIOS software queries this field to determine the adapter type at system configuration time. LA0, LA1, and LA2 (Latched Address, pins 12, 13, and 14) are used to select the POS address; and the DT7920's -PROM signal (-PROM Enable, pin 72) is used to enable the external device storing the POS Adapter Identification data while the DT7920's -XMIT signal (-Transmit, pin 79) is used to gate the data onto the Micro Channel data bus (D 00:D 07) via the data transceivers.

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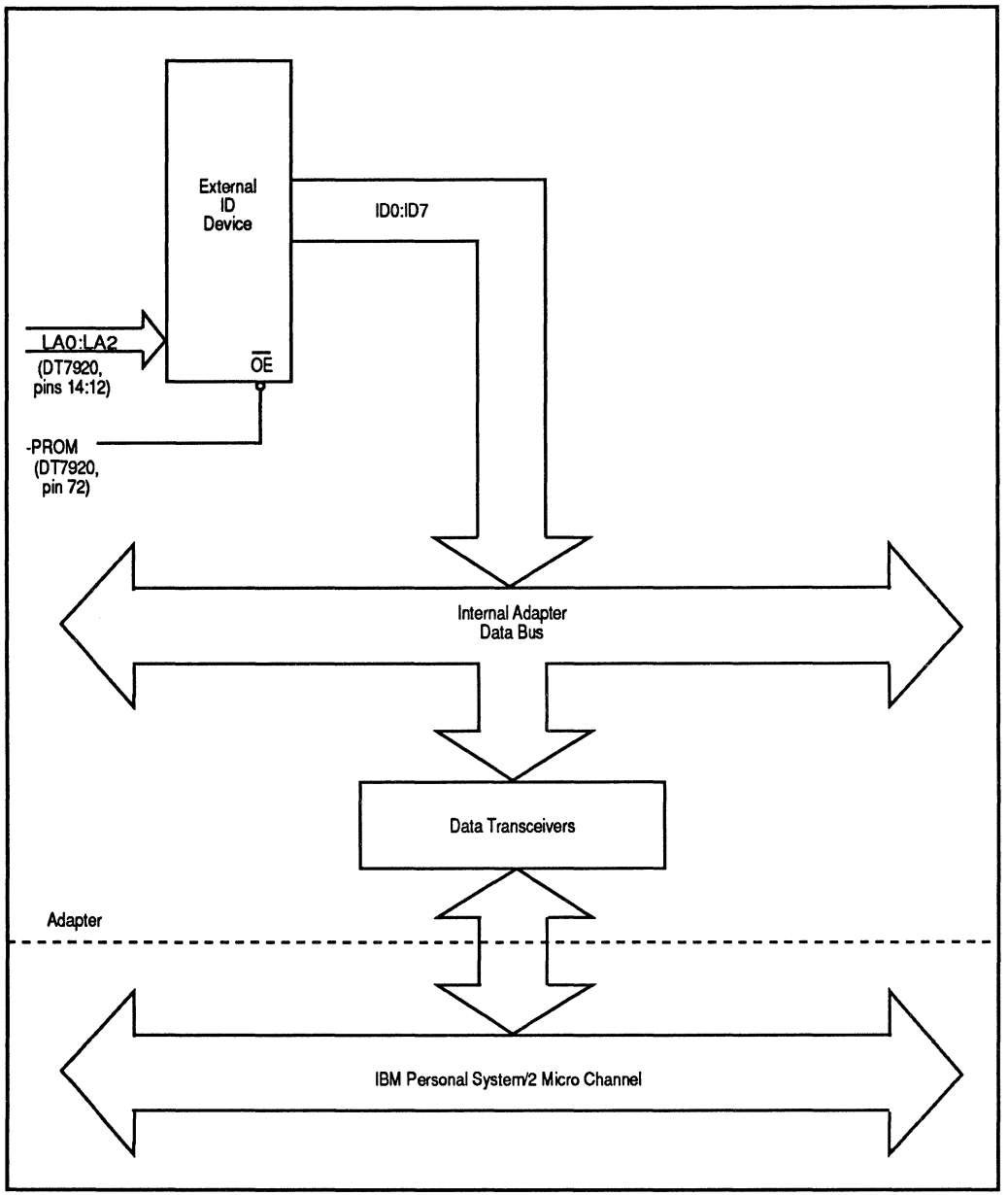
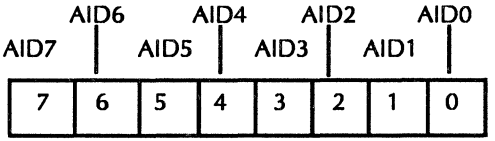


Figure 5. The DT7920 -PROM output is used to enable an external read-only identification (ID) device.

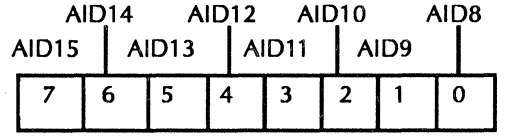
POS LOCATION 0100



Bits 7:0—Adapter ID, Least Significant Byte (AID7:AID0), Read Only

These bits comprise the least significant byte of the adapter identification field. They are not implemented in the DT7920, and must be provided in an external identification device.

POS LOCATION 0101



Bits 7:0—Adapter ID, Most Significant Byte (AID15:AID8), Read Only

These bits comprise the most significant byte of the adapter identification field. They are not implemented in the DT7920, and must be provided in an external identification device.

POS 0102—I/O Address Selection and Card Enable

POS location hex 0102 is implemented in the DT7920. This location is used to select the I/O Base Address and Card Enable.

Bit 0 is the Card Enable bit. When Card Enable is clear, the DT7920 signals -RD (-Read, DT7920 pin 81) and -WR (-Write, pin 80) are disabled; also, any external circuitry must be disabled from responding to or driving the Micro Channel bus (this occurs via DT7920 signal CDEN, pin 6, which is controlled by bit 0). The only exception is during Setup Mode where the POS information must be provided as required by responding to Setup Mode I/O read and write command cycles. As part of the setup process, the host executes the Adapter Description File, sets the parameters for the adapter, and turns the Card Enable bit on.

Bits 1:7 of POS location hex 0102 are used to select the Base I/O address. The DT7920 provides seven programmable address match bits to permit relocating the adapter within the

TABLE 1. DT7920 POS REGISTERS

POS Location (Hex)	Function	Implementation
0100	Adapter Identification, Low Byte	External ID
0101	Adapter Identification, High Byte	External ID
0102	Card Enable (0)	DT7920
	I/O Base Address Selection (7:1)	DT7920
0103	User-Programmed (2:0)	DT7920
	DMA Channel A Fairness Enable (3)	DT7920
	DMA Channel A Arbitration (7:4)	DT7920
0104	User-Programmed (2:0)	DT7920
	DMA Channel B Fairness Enable (3)	DT7920
	DMA Channel B Arbitration (7:4)	DT7920
0105	User-Programmed (5:0)	External ID
	Not Implemented (7:6)	Optional External
0106	Not Applicable	–
0107	Not Applicable	–

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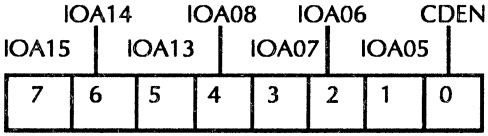
Micro Channel I/O space. The range of available addresses excludes the low order 4 Kbytes (hex 0000 to 0FFF) of I/O address space; this space is normally used by hardware on the system board. The range of base addresses is spread over the remaining 60 Kbytes of I/O address space, permitting a wide range of address locations. This gives the user great flexibility in locating the I/O address range even in systems where large sections of contiguous address space are reserved by other I/O devices.

POS LOCATION 0102



Bits 7:1—I/O Address (IOA15:IOA13, IOA08:IOA05), R/W

These bits comprise seven bits of the I/O base address for the external control registers on the adapter. Setting a bit causes the DT7920 to match to 1 on the corresponding I/O base address bit. Clearing a bit causes the chip to match to 0 on the corresponding I/O base address bit.

Of the remaining I/O address bits, bit 12 always matches to 1; bits 11, 10, and 9 always match to 0. Bits 0 to 4 are not decoded in the DT7920; they are latched in the chip, and provided externally to select up to 32 address locations decoded on the adapter. Figure 6 indicates the bit assignments of the DT7920's I/O base address. Table 2 shows typical I/O base addresses.

TABLE 2. TYPICAL I/O BASE ADDRESSES

POS Location Hex 0102 Bits							I/O Base
7	6	5	4	3	2	1	Address (hex)
0	0	0	0	0	0	0	1000
0	0	0	0	0	0	1	1020
0	0	0	0	0	1	0	1040
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
0	0	0	1	1	1	0	11C0
0	0	0	1	1	1	1	11E0
0	0	1	0	0	0	0	3000
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
0	1	1	1	1	1	1	71E0
1	0	0	0	0	0	0	9000
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
1	1	0	1	1	1	1	D1E0
1	1	1	0	0	0	0	F000

Bit 0—Card Enable (CDEN), R/W

This bit is the card enable for the adapter. When clear, DT7920 signals -RD (-Read, DT7920 pin 81) and -WR (-Write, pin 80) are disabled, and external adapter circuitry must

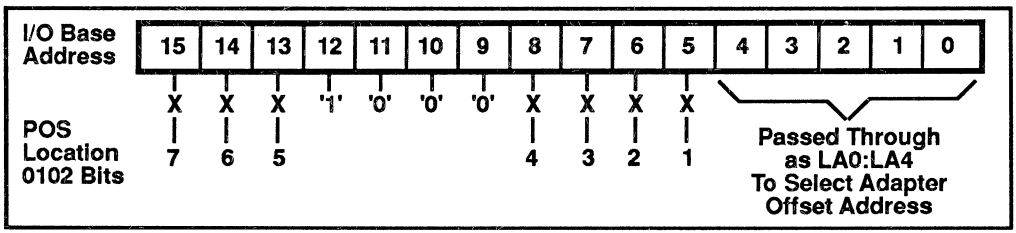


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Figure 6. DT7920 I/O Base Address Bit Assignments

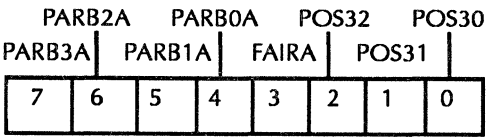
be disabled from responding to any I/O or memory read or write command, and must not generate any interrupt requests. The data bus transceivers, however, must respond to Setup Mode I/O read and write commands. When set, this bit enables normal adapter operations. This bit is cleared on powerup. This signal is brought out for the adapter designer as CDEN (Card Enable, pin 6).

POS 0103—DMA Channel A Control

The DT7920 provides complete control for two Personal System/2 DMA channels (termed channels A and B). All control logic for these DMA channels is built into the DT7920. POS location hex 0103 specifies arbitration level and Fairness for DMA channel A. Bits 4:7 select the local arbiter level used by the channel A arbitration logic included in the DT7920. Bit 3 enables or disables Fairness for DMA channel A. The Fairness feature on the Micro Channel allows the system to service all arbitrating devices in order of priority before the same device can gain control of the channel again.

Bits 0:2 of POS location hex 0103 are user-programmable output control bits. They are latched in the DT7920 and given to the adapter designer to use as desired. They are provided as POS30 (pin 4), POS31 (pin 3), and POS32 (pin 2). (See the applications section for a design that uses POS30, POS31, and POS32 to select the adapter interrupt level.)

POS LOCATION 0103



Bits 7:4—DMA Channel A Arbitration Level (PARB3A:PARB0A), R/W

These bits select the arbitration level for DMA Channel A. PARB0A (bit 4) is the LSB. Arbitration level 0 is the highest arbitration level. Arbitration applies to both Burst and Single Transfer DMA modes. These bits are cleared on powerup.

Bit 3—DMA Channel A Fairness Enable (FAIRA), R/W

When set, this bit enables the Fairness feature for Burst DMA mode. When cleared, this bit disables the Fairness feature. This bit is cleared on powerup.

Bits 2:0—User-Definable Bits (POS32:POS30), R/W

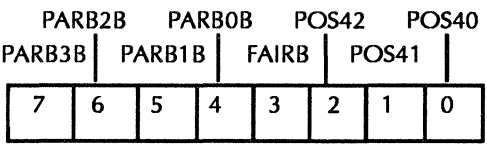
These bits can be defined for user operations. The information stored in these bits is available on DT7920 pins pins 4 to 2 (POS30, POS31, and POS32).

POS 0104—DMA Channel B Control

POS location hex 0104 specifies arbitration level and Fairness for DMA channel B. Bits 4:7 select the local arbiter level used by the channel B arbitration logic included in the DT7920. Bit 3 enables or disables Fairness for DMA channel B.

Bits 0:2 of POS location hex 0104 are user-programmable control bits. They are latched in the DT7920 and given to the adapter designer to use as desired. They are provided as POS40 (pin 58), POS41 (Pin 59), and POS 42 (Pin 60).

POS LOCATION 0104



Bits 7:4—DMA Channel B Arbitration Level (PARB3B:PARB0B), R/W

These bits select the arbitration level for DMA Channel B. PARB0B (bit 4) is the LSB. Arbitration level 0 is the highest level. Arbitration applies to Burst and Single Transfer DMA modes. These bits are cleared on powerup.

Bit 3—DMA Channel B Fairness Enable (FAIRB), R/W

When set, this bit enables the Fairness feature for Burst DMA mode. When cleared, this bit disables the Fairness feature. This bit is cleared on powerup.

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Bits 2:0—User-Definable Bits (POS42:POS40), R/W

These bits can be defined for user operations. The information stored in these bits is available on DT7920 pins pins 58 to 60 (POS40, POS41, and POS42).

POS 0105 To 0107

Locations hex 0105 to hex 0107 are not implemented in the chip. They are directed to the external identification device via the DT7920 -PROM (-PROM Enable, pin 72) signal.

Location hex 0105 is user-programmable, read only, and can be used to read back any value specified by the user, except for bits 6 and 7. Bit 7 is defined by IBM as a Channel Check Active Indicator used for system memory and I/O functions to report a serious error. Bit 6 is defined by IBM as a Channel Check Status indicator. Channel check is not implemented in the DT7920, and both these bits must read back from the external identification device as set (1s).

POS locations hex 0106 and 0107 are defined by IBM as Subaddress Extension Bytes and are not implemented in the DT7920. These bytes are ignored for a write access and must read back from the external identification device as set (all 1s).

The adapter designer who wishes to implement channel check can do so using external circuitry to decode the appropriate POS locations and implement these functions. Subaddressing is not applicable to the DT7920.

PROGRAMMED I/O OPERATIONS

The DT7920 supports programmed I/O operations. The following signals are involved.

The DT7920 decodes Micro Channel signals M/-IO (Memory/-Input Output, DT7920 pin 33), -S0 (-Status Bit 0, pin 35), and -S1 (-Status Bit 1, pin 34) to produce chip outputs -WR (-Write, pin 80), and -RD (-Read, pin 81) when the internal I/O base address matches. The adapter designer uses DT7920 outputs -WR, -RD, the latched address bits LA0 to LA4 (pins 14 to 10), and -LSBHE (-Latched System Byte High Enable, pin 83) to decode I/O registers during PIO operations.

Table 3 summarizes the interaction of bus inputs and DT7920 outputs in I/O transfer operations. Table 4 shows the interaction of Micro Channel signal -SBHE (-System Byte High Enable, latched in the DT7920 and presented as -LSBHE on pin 83) and bus address A 00 (latched in the DT7920 and presented as LA0 on pin 14) in specifying byte or 16-bit word transfers.

TABLE 3. I/O TRANSFER SIGNALS

	Bus Signals			DT7920 Outputs	
Function	M/-IO	-S0	-S1	-WR	-RD
Reserved A	0	0	0	1	1
I/O Write	0	0	1	0	1
I/O Read	0	1	0	1	0
Reserved B	0	1	1	1	1
Reserved C	1	0	0	1	1
Reserved D	1	1	1	1	1

TABLE 4. BYTE OR WORD TRANSFER SELECTION

	DT7920 Outputs	
Valid Data On	-LSBHE	LA0
16-Bit Word (D 00:D 15)	0	0
Upper Byte (D 08:D 15)	0	1
Lower Byte (D 00:D 07)	1	0
Reserved	1	1

DMA OPERATIONS

The DT7920 has a pair of Micro Channel DMA Slave Controllers; it contains bus interface, arbitration, and Fairness control for two independent DMA channels. This permits the adapter to perform more than one function simultaneously under DMA control. The design also permits high performance applications (such as high speed continuous data transfers) to use both channels sequentially, and avoid data gaps.

The DT7920 is designed to operate in Burst (multiple transfer) mode, and can transfer at least 1 to 8 data values with each DMA channel grant.

If DMA transfers involve only one value, Single Transfer mode is preferred because it is easier to program and executes in somewhat less time than performing one transfer in Burst mode. The designer can operate the DT7920 in Single Transfer DMA mode by not connecting DT7920 -BURST (pin 41) and -OBURST (pin 40) signals to the Micro Channel -BURST line (bus connector pin A22).

When operated in Single Transfer mode, the DT7920 is used for gaining access to a DMA channel via arbitration. Once the adapter gains access to a DMA channel (when the corresponding -DMA-ACTIVE line on the DT7920 goes low), the adapter executes its single data transfer and then must terminate the request signal by deasserting the appropriate DT7920 -DMA-RQST signal with the -WR or -RD signal.

The adapter requests a DMA transfer by asserting the appropriate DMA Request line (-DMA-RQST-B, pin 76, for channel B; or -DMA-RQST-A, pin 78, for channel A). The request occurs asynchronously, and is translated into the appropriate Micro Channel bus signals by the chip. Upon receiving control of the Micro Channel, the DT7920 acknowledges by driving the appropriate DMA Active line (-DMA-ACTIVE-B, pin 75, for channel B; or -DMA-ACTIVE-A, pin 77, for channel A) active (low). This signifies that the adapter now has control of a Micro Channel DMA channel, and that data transfers begin with the next -WR or -RD signal. DMA channel A and DMA channel B are truly independent and therefore simultaneous requests are permitted.

For bursts of more than one (Burst mode only), the adapter does not terminate the DMA Request until all desired data transfers have occurred. After the first eight transfers have occurred, the DT7920 checks to see if any other device is requesting DMA service (checks to see if any other device is asserting -PREEMPT). If so, the chip relinquishes control of the bus to the Micro Channel arbitration logic, which grants bus control to the highest priority device. Note that if Fairness has been enabled for the DMA channel, the DT7920 eliminates that channel from arbitration until all requesting devices have been serviced once.

If no other device is requesting DMA service after the first eight transfers, the DT7920 performs an additional eight transfers and again checks -PREEMPT. This continues until all data values have been transferred, or until some other Micro Channel device asserts -PREEMPT. During this time, the adapter holds the DMA request until all the required data values are transferred.

EXTENDED COMMAND CYCLES

The DT7920 supports both synchronous and asynchronous extended command cycles. Extended command cycles permit an adapter to perform operations over more than the default command cycle, and thus can be used to accommodate relatively slow peripherals. The extended command cycles can either be terminated by the Micro Channel -CMD line (synchronous), or by the adapter (asynchronous).

TABLE 5. EXTENDED COMMAND CYCLE SELECTION

Command Cycle	DT7920 Input Line -X-C-DONE	DT7920 Output Line CD CHRDY
Extended Command Cycles Disabled	Tied Low	1
Extended I/O Command Cycles Enabled	1[1]	0[2]

Notes:

1. This is a dynamic input that controls the duration of extended command cycles.
2. When cleared (0), this output causes the Micro Channel to extend the command cycle.

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One chip input line controls these operations: -X-C-DONE (-Extended Cycle Done, pin 5). When extended command cycles are enabled (see Table 6), -X-C-DONE determines the duration of the command cycles, and is driven by the Micro Channel -CMD (-Command) line for synchronous transfers or by the adapter for asynchronous transfers. For adapters requiring only default command cycles, -X-C-DONE is tied low.

This input line is decoded by the DT7920 and drives CD CHRDY (Card Channel Ready, pin 8). This in turn is used to hold Micro Channel CD CHRDY inactive (low) to control the duration of the extended cycle.

Table 5 shows the relationship between the DT7920 input and extended command cycle operations.

Extended cycle control is provided by -X-C-DONE. To implement synchronous extended cycles, -X-C-DONE is driven by the Micro Channel -CMD (-Command) line. To implement asynchronous extended cycles, -X-C-DONE is held inactive (high) until the adapter is ready for a data transfer. At this point -X-C-DONE is driven active (low) for a minimum of 35ns. This causes the DT7920 to drive the Micro Channel CD CHRDY line inactive via DT7920 pin 8 (CD CHRDY).-RD or WR active to X-C-DONE active must not exceed 2.6µs.

DT7920 PIN FUNCTIONS

This section describes the pin functions of the DT7920 chip.

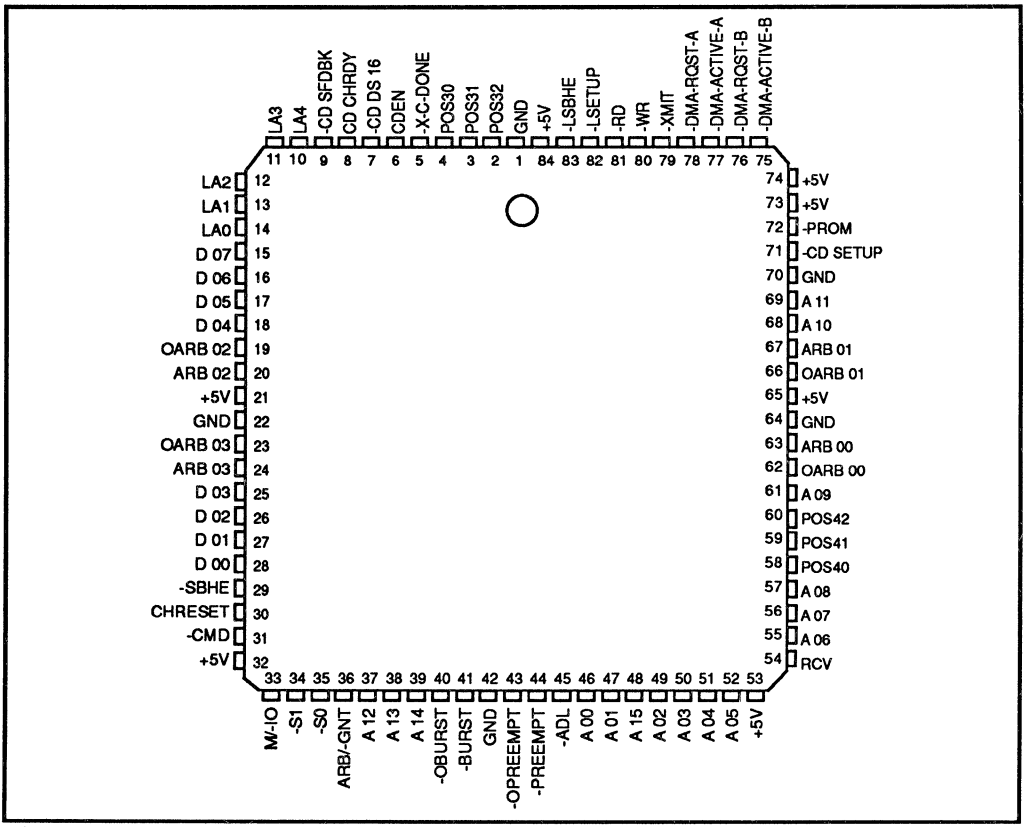

Figure 7. DT7920 Pin Functions

M-0083

TABLE 6. DT7920 PIN DESCRIPTIONS

Signal	Pin	Type	Output Drive (mA)	Description
-ADL	45	IM	—	-Address Decode Latch is an active low input driven by the Micro Channel.
-CMD	31	IM	—	-Command is an active low input driven by the Micro Channel. -CMD indicates that a channel cycle is in progress and is used to gate -WR, -RD, RCV, and -XMIT.
-S0 -S1	35 34	IM IM	— —	-Status Bit 0 and -Status Bit 1 are active low inputs driven by the Micro Channel. These are decoded in the chip to specify read or write operations (see Table 3).
M/-IO	33	IM	—	Memory/-Input Output is an input driven by the Micro Channel. M/-IO is high during a bus memory cycle, and low during an I/O cycle.
-SBHE	29	IM	—	-System Byte High Enable is an active low input driven by the Micro Channel. -SBHE enables transfer of data on the high data byte (D 08:D 15), and is used with A 00 to distinguish between high byte and low byte transfers. The chip latches this bit and presents it to the adapter designer as -LSBHE.
CHRESET	30	IM	—	Channel Reset is an active high input driven by the Micro Channel. The DT7920 disables all bus outputs after CHRESET rises, resets internal DMA controllers, and clears all internal registers. This also resets POS location hex 0102 bit 0 to disable the adapter via Card Enable (CDEN).
CD CHRDY	8	OM	8	Card Channel Ready is an output generated by the DT7920 that drives the Micro Channel. CD CHRDY is generated from input signal -X-C-DONE, and drives Micro Channel CD CHRDY low (not ready) to request an extended command cycle when required (see Table 5).
-CD DS 16	7	OM	8	-Card Data Size 16 is an output generated by the DT7920 that drives the Micro Channel. -CD DS 16 indicates to the Micro Channel that the adapter supports 16-bit data transfers by pulling Micro Channel -CD DS 16 low (active) during a valid channel address. Pin 7 should not be connected for 8-bit adapters.

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TABLE 6 (Continued). DT7920 PIN DESCRIPTIONS

Signal	Pin	Type	Output Drive (mA)	Description
-CD SFDBK	9	OM	8	-Card Selected Feedback is an output generated by the DT7920 that drives the Micro Channel. -CD SFDBK indicates that an adapter is present at the address specified during a channel cycle by pulling Micro Channel -CD SFDBK low during a valid channel address.
-CD SETUP	71	IM	—	-Card Setup is an active low input driven by the Micro Channel. -CD SETUP is used to place the DT7920 in Setup Mode to enable programming and read operations of the chip POS functions. -CD SETUP is latched and provided as -LSETUP, along with a read signal (-PROM) to enable read operations from selected POS locations in an external ID device. -PROM is asserted only during Setup Mode read operations to POS addresses hex 0100, 0101, 0105, 0106, and 0107.
-LSETUP	82	OA	8	-Latched Setup is an active low output driven by the DT7920 for use by the adapter designer. It is the latched -CD SETUP signal, and remains valid through the entire command cycle.
D 00:D 07	(28;27;26; 25;18;17; 16;15)	BIDM	4	Data Bits 0 through 7 are bidirectional data lines that interface via an external data transceiver chip to Micro Channel data lines D 00 to D 07 (see Figure 4).These lines drive and receive under DT7920 control during Setup Mode. When the DT7920 is not in Setup Mode, these lines are in tri-state, high impedance mode.
A 00:A 15	(46;47;49; 50;51;52; 55;56;57; 61;68;69; 37;38;39;48)	IM	—	Address bits A 00 to A 15 are inputs driven by the Micro Channel. These bits are used internally by the DT7920 in all I/O addressing. Low order bits are latched and made available on LA0:LA4. Other bits are decoded for an address match. A00 is LSB.
LA0:LA4	(14;13;12; 11;10)	OA	4	Latched Address bits 0 to 4 are outputs driven by the DT7920 for use by the adapter designer. They are used to select addresses on the adapter, and select POS locations in Setup Mode. LA0 is the LSB. They are valid through the entire command cycle.
-RD -WR	81 80	OA OA	8 8	-Read and -Write are active low outputs driven by the DT7920 for use on the adapter. -RD and -WR are used with -LSBHE, LA0:LA4, and -X-C-DONE to perform read and write cycles.

TABLE 6 (Continued). DT7920 PIN DESCRIPTIONS

Signal	Pin	Type	Output Drive (mA)	Description
-XMIT	79	OA	4	-Transmit is an active low output driven by the DT7920 for use by the adapter designer. -XMIT is used with RCV to control external data transceivers (see Figure 4). -XMIT is active during all valid I/O reads including reads in Setup Mode.
RCV	54	OA	4	Receive is an active high output driven by the DT7920 for use by the adapter designer. RCV is used with -XMIT to control external data transceivers (see Figure 4). RCV is active during all valid I/O writes including writes in Setup Mode. RCV is delayed from -WR to allow hold time to decode writes to adapter addresses.
-LSBHE	83	OA	8	-Latched System Byte High Enable is an active low output driven by the DT7920 for use by the adapter designer. -LSBHE is used in conjunction with LA0 to distinguish between byte and word transfers on the adapter (see Table 4). -LSBHE is controlled by -SBHE, is transparently latched by -ADL, and is valid through the entire command cycle.
CDEN	6	OA	8	Card Enable is an active high output driven by the DT7920 and is controlled by POS address hex 0102, bit 0. When inactive (low), all external adapter circuitry must be disabled from driving signals onto the Micro Channel. When inactive, the DT7920 disables the -RD and -WR control lines, as well as -DMA-RQST-A and -DMA-RQST-B. This bit is cleared on powerup.
-PROM	72	OA	4	-PROM Enable is an active low output driven by the DT7920 to enable reading of identification and other stored information from an external identification device such as a PROM, ROM, or PAL. This signal is active in Setup Mode reads of POS locations hex 0100 and 0101 (adapter identification), and locations 0105 to 0107.

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TABLE 6 (Continued). DT7920 PIN DESCRIPTIONS

Signal	Pin	Type	Output Drive (mA)	Description
-X-C-DONE	5	IA	—	-Extended Cycle Done is an active low input driven by external adapter circuitry. This line is used to extend the command cycle when required by the adapter on read or write operations (see Table 5). Where default command cycles (190ns) will be used, -X-C-DONE should be tied low to disable extended cycles. Where extended cycles are required, the adapter should hold this line inactive (high) until it is ready to transmit to or receive valid data from the Micro Channel. -RD or -WR active to -X-C-DONE active must not exceed 2.6µs.
POS30:POS32 POS40:POS42	(4;3;2) (58;59;60)	OA OA	4 4	POS30:POS32 and POS40:POS42 are outputs driven by the DT7920 to implement any function on the adapter that the designer wishes to program using the POS. These outputs are controlled by POS Location hex 0103, bits 0:2; and POS Location hex 0104, bits 0:2, respectively. These are intended to replace jumpers in adapter designs, and can be accessed only in Setup Mode. These outputs are cleared on powerup.
+5V	21;32;53; 65;73;74; 84	IM	—	+5V is the power input to the DT7920 from the Micro Channel. Connect all designated pins to Micro Channel +5V.
GND	1;22;42; 64;70	IM	—	GND is the power ground connection to the DT7920 from the Micro Channel. Connect all designated pins to Micro Channel GND.
-PREEMPT -OPREEMPT	44 43	BIDM,OC OM,OC	24 (both)	-PREEMPT is an active low, bidirectional open collector line generated by the DT7920 that drives Micro Channel -PREEMPT. It is asserted by the DT7920 to request a Micro Channel DMA transfer. It is controlled by the adapter via -DMA-RQST-A and/or -DMA-RQST-B. -PREEMPT is received by the DT7920 during a DMA request, and is used to monitor the Micro Channel for foreign DMA requests when supporting Fairness. -OPREEMPT is an active low open collector output that is used with -PREEMPT to supply the 24mA required to drive Micro Channel -PREEMPT. -PREEMPT and -OPREEMPT (pins 43 and 44) should be tied together at the chip.

TABLE 6 (Continued). DT7920 PIN DESCRIPTIONS

Signal	Pin	Type	Output Drive (mA)	Description
-BURST -OBURST	41 40	OM,OC OM,OC	24 (both)	-BURST is an active low open collector output generated by the DT7920. -BURST is tied to the Micro Channel -BURST line to enable Burst Mode DMA transfers. -BURST is left unconnected for Single Transfer DMA. -OBURST is an active low open collector output that is used with -BURST to supply the 24mA required to drive Micro Channel -BURST. -BURST and -OBURST (pins 40 and 41) should be tied together at the chip if Burst Mode DMA is desired.
ARB/-GNT	36	IM	—	Arbitrate/-Grant is an input driven by the Micro Channel. When high, ARB/-GNT indicates that an arbitration cycle is in progress; when low, it indicates that a grant has occurred.
-DMA-RQST-A -DMA-RQST-B	78 76	IA,PU IA,PU	— —	-DMA Request Channel A and -DMA Request Channel B are active low inputs driven by the adapter. Each is pulled up internally to +5V. Either is asserted asynchronously by the adapter to request a DMA transfer on channel A or channel B, and held low until the required number of transfers has occurred. In Single Transfer DMA, these signals should be deasserted on detecting a -RD or -WR qualified by the appropriate address (LA[n]) decode.
-DMA-ACTIVE-A -DMA-ACTIVE-B	77 75	OA OA	4 4	-DMA Active Channel A and -DMA Active Channel B are active low outputs driven by the DT7920 for use by the adapter designer. These outputs are asserted after the appropriate -DMA Request line has been asserted and has been granted channel control by the Micro Channel. These outputs are deasserted either by deasserting the appropriate -DMA Request line, or if control of the Micro Channel is lost to a foreign DMA request during Burst Mode DMA transfers.

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TABLE 6 (Continued). DT7920 PIN DESCRIPTIONS

Signal	Pin	Type	Output Drive (mA)	Description
ARB 00: ARB 03 OARB 00: OARB 03	(63;67; 20;24) (62;66; 19;23)	BIDM, OC OM, OC	24 (each pair)	Arbitration Priority Levels 0:3 are bidirectional, open collector outputs generated by the DT7920 that drive Micro Channel ARB0:ARB3. These lines are controlled by POS Location hex 0103 bits 4:7 for DMA Channel A, and POS Location hex 0104 bits 4:7 for DMA Channel B. These lines specify the arbitration level assigned to the designated DMA Channel. OARB0:OARB3 are open collector outputs that are used with ARB0:ARB3 to supply the 24mA drive required to drive Micro Channel ARB0:ARB3. Each ARB pin should be tied to the corresponding OARB pin at the chip.

Notes to Table 6:

1. IM = Input from Micro Channel
2. IA = Input from adapter
3. OM = Output to Micro Channel
4. OA = Output to adapter
5. OC = Open collector logic
6. PU = Pulled up internally to +5V
7. BIDM = I/O to/from Micro Channel

TABLE 7. ALPHABETICAL LISTING OF PIN SIGNALS

Pin Signal	Pin Number
+5V	21,32,53, 65 73,74,84
-ADL (Bus)	45
-BURST (Bus)	41
-CD DS 16 (Bus)	7
-CD SETUP (Bus)	71
-CD SFDBK (Bus)	9
-CMD (Bus)	31
-DMA-ACTIVE-A	77
-DMA-ACTIVE-B	75
-DMA-RQST-A	78
-DMA-RQST-B	76
-LSBHE	83
-LSETUP	82
-OBURST[3]	40
-OPREEMPT[3]	43
-PREEMPT (Bus)	44
-PROM	72
-RD	81
-S0 (Bus)	35
-S1 (Bus)	34
-SBHE (Bus)	29
-WR	80
-X-C-DONE	5
-XMIT	79
A 00 (Bus)	46
A 01 (Bus)	47
A 02 (Bus)	49
A 03 (Bus)	50
A 04 (Bus)	51
A 05 (Bus)	52
A 06 (Bus)	55
A 07 (Bus)	56
A 08 (Bus)	57
A 09 (Bus)	61
A 10 (Bus)	68
A 11 (Bus)	69
A 12 (BUS)	37

Pin Signal	Pin Number
A 13 (Bus)	38
A 14 (Bus)	39
A 15 (Bus)	48
ARB 00 (Bus)	63
ARB 01 (Bus)	67
ARB 02 (Bus)	20
ARB 03 (Bus)	24
ARB/-GNT (Bus)	36
CD CHRDY (Bus)	8
CDEN	6
CHRESET (Bus)	30
D 00[4]	28
D 01[4]	27
D 02[4]	26
D 03[4]	25
D 04[4]	18
D 05[4]	17
D 06[4]	16
D 07[4]	15
GND	1,22, 42,64,70
LA0	14
LA1	13
LA2	12
LA3	11
LA4	10
M/-IO (Bus)	33
OARB 00[3]	62
OARB 01[3]	66
OARB 02[3]	19
OARB 03[3]	23
POS30	4
POS31	3
POS32	2
POS40	58
POS41	59
POS42	60
RCV	54

Notes: 1. Signals with leading hyphens are active low.
2. Micro Channel bus signals are indicated.
3. These signals connect directly to the Micro Channel bus.
4. These signals connect to the bus via a data transceiver chip.

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SPECIFICATIONS

Following are maximum, recommended operating, and dc characteristics for the DT7920.

TABLE 8. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	With respect to Ground	-0.3	7.0	V
V_I	DC Input Voltage	–	-0.3	V_{CC}+0.3	V
I_{OUT}	DC Output Current per Output Pin	–	-25	+25	mA
P_D	Power Dissipation	–	–	500	mW
T_{STG}	Storage Temperature	No Bias	-40	+125	°C

TABLE 9. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	DC Supply Voltage	–	+3	+6	V
T_A	Ambient Operating Temperature	–	0	+70	°C

TABLE 10. DC OPERATING CHARACTERISTICS (V_{CC}=5V±5%, T_A=0-70°C)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH Level Input Voltage	–	2.0	–	–	V
V_{IL}	LOW Level Input Voltage	–	–	–	0.8	V
V_{OH}	HIGH Level Output Voltage	–	2.4	4.5	–	V
V_{OL}	LOW Level Output Voltage	–	–	0.2	0.4	V
I_I	Input Leakage Current	V_I=Ground-V_{CC}	–	±1	±10	µA
I_{OZ}	Output Hi-Z Leakage Current	V_O=Ground-V_{CC}	–	±1	±10	µA
I_{CC}	V_{CC} Supply Current	V_I=Ground-V_{CC}	–	5	100	mA

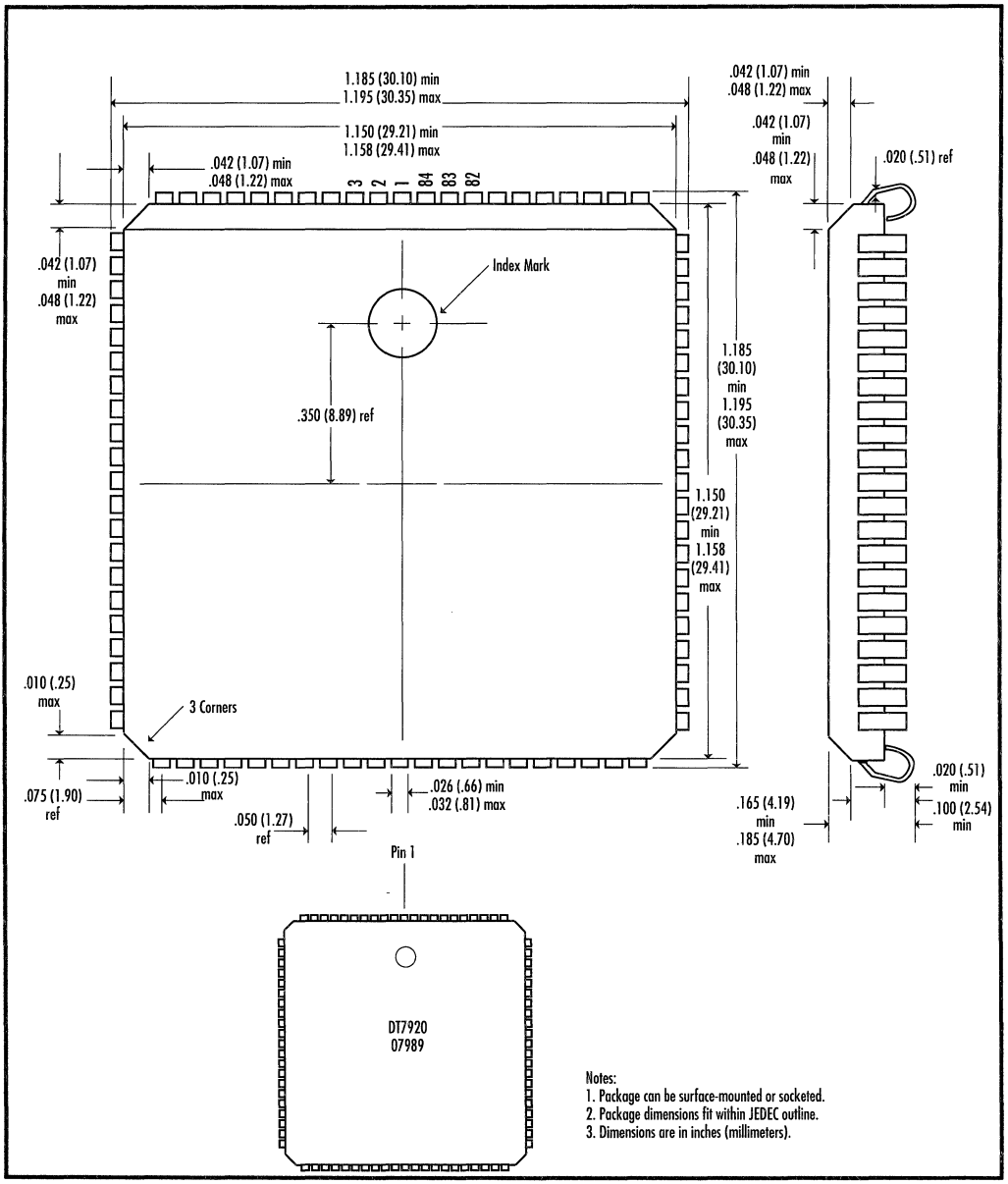

Figure 8. DT7920 Outline Dimensions

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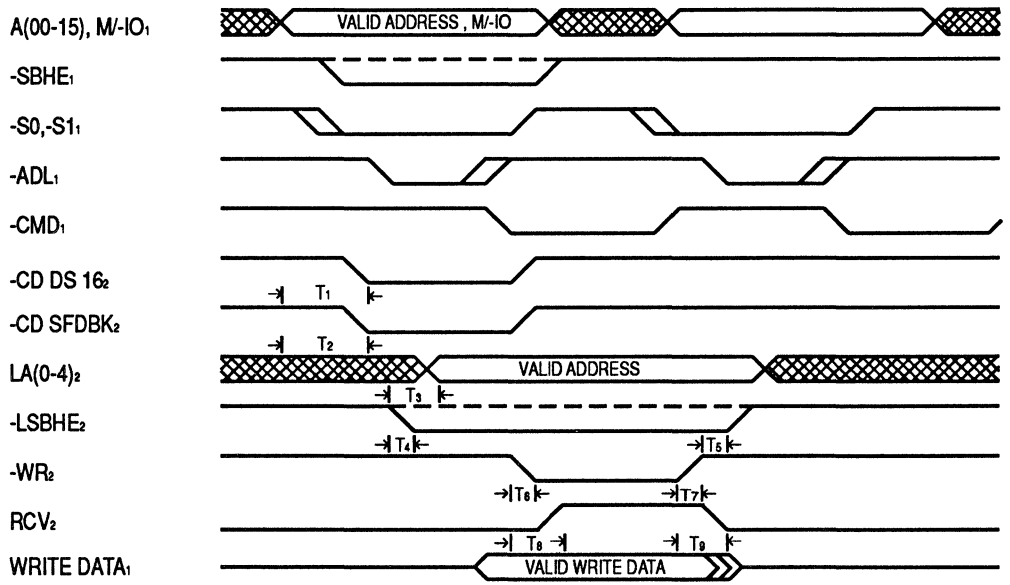
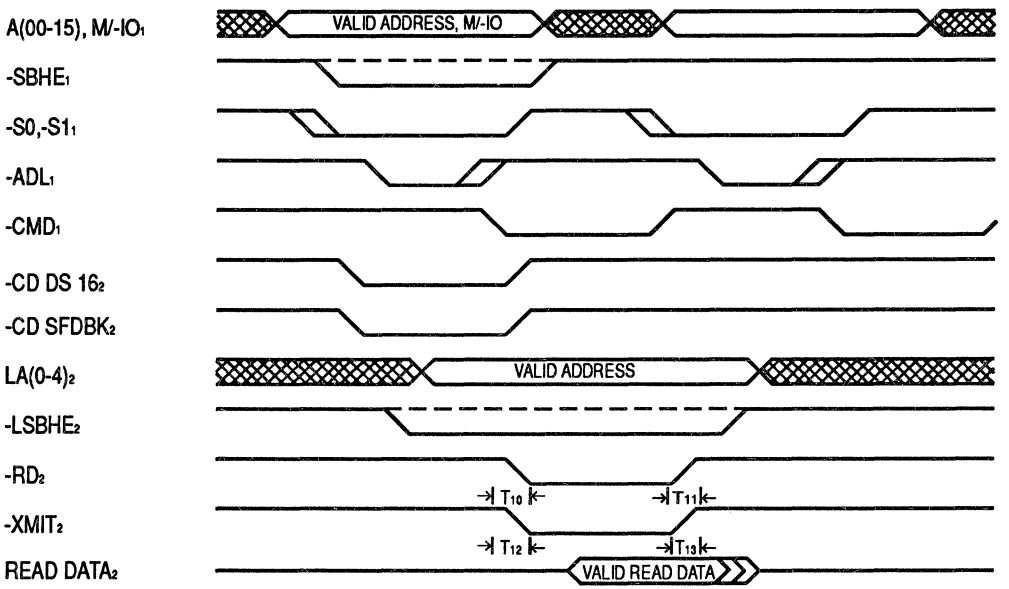


Timing Parameter	Min	Typ	Max	Unit
T_1 A(00-15),M/-IO_{VALID}—> -$CDDS16_{ACTIVE}$	—	25	40	ns
T_2 A(00-15),M/-IO_{VALID}—> -$CDSFDBK_{ACTIVE}$	—	25	40	ns
T_3 -ADL_{ACTIVE}—>$LA(0-4)_{VALID}$	—	18	37	ns
T_4 -ADL—> -$LSBHE_{ACTIVE}$	—	15	30	ns
T_5 -$WR_{INACTIVE}$—>$RCV_{INACTIVE}$	10	15	—	ns
T_6 -CMD_{ACTIVE}—> -WR_{ACTIVE}	—	15	25	ns
T_7 -$CMD_{INACTIVE}$—> -$WR_{INACTIVE}$	—	12	18	ns
T_8 -$CMD_{INACTIVE}$—>RCV_{ACTIVE}	—	25	40	ns
T_9 -$CMD_{INACTIVE}$—>RCV	11	27	45	ns

Figure 9. Basic Command Cycle: I/O Write

M-0093



Timing Parameter	Min	Typ	Max	Unit
T_{10} -CMD_{ACTIVE}—> -RD_{ACTIVE}	—	15	25	ns
T_{11} -$CMD_{INACTIVE}$—> -$RD_{INACTIVE}$	—	10	18	ns
T_{12} -CMD_{ACTIVE}—> -$XMIT_{ACTIVE}$	—	17	30	ns
T_{13} -$CMD_{INACTIVE}$—> -$XMIT_{INACTIVE}$	—	11	20	ns

Figure 10. Basic Command Cycle: I/O Read

M-0094

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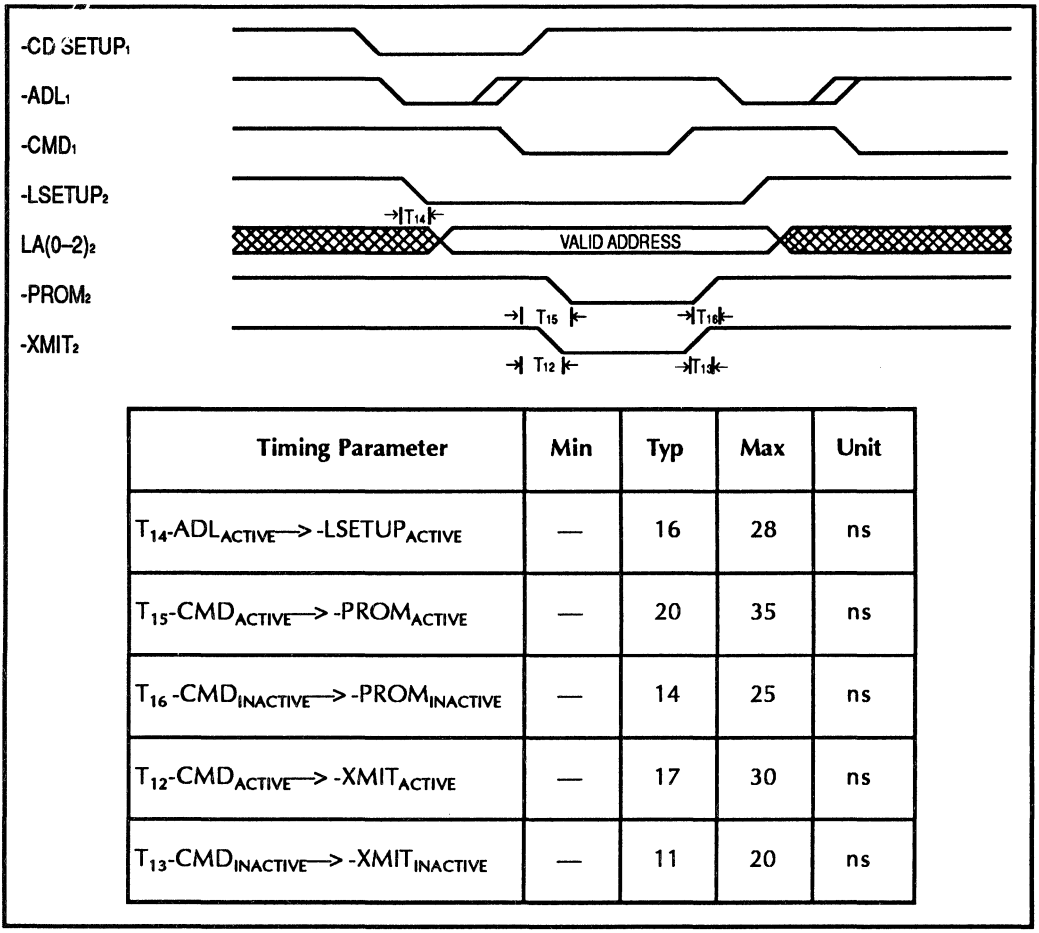
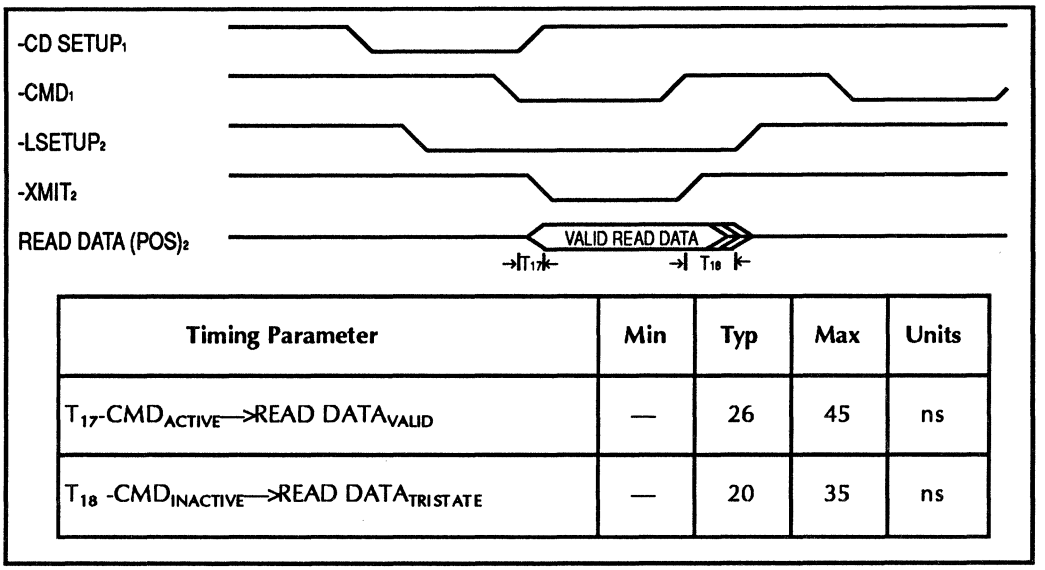


Timing Parameter	Min	Typ	Max	Unit
T_{14}-ADL_{ACTIVE}—> -$LSETUP_{ACTIVE}$	—	16	28	ns
T_{15}-CMD_{ACTIVE}—> -$PROM_{ACTIVE}$	—	20	35	ns
T_{16} -$CMD_{INACTIVE}$—> -$PROM_{INACTIVE}$	—	14	25	ns
T_{12}-CMD_{ACTIVE}—> -$XMIT_{ACTIVE}$	—	17	30	ns
T_{13}-$CMD_{INACTIVE}$—> -$XMIT_{INACTIVE}$	—	11	20	ns

Figure 11. Configuration Cycle: External POS ID Read Cycle

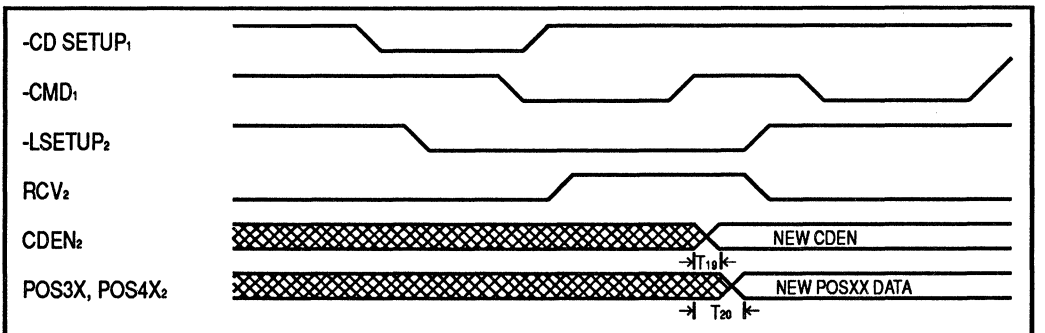
M-0095



Timing Parameter	Min	Typ	Max	Units
T_{17}-CMD_{ACTIVE}—>READ $DATA_{VALID}$	—	26	45	ns
T_{18} -$CMD_{INACTIVE}$—>READ $DATA_{TRISTATE}$	—	20	35	ns

Figure 12. Configuration Cycle: Internal POS Register Access, Read Cycle

M-0096



Timing Parameter	Min	Typ	Max	Units
T_{19} -$CMD_{INACTIVE}$—>$CDEN_{VALID}$	—	22	37	ns
T_{20} -$CMD_{INACTIVE}$—>$POSXX_{VALID}$	—	23	40	ns

Figure 13. Configuration Cycle: Internal POS Register Access, Write Cycle

M-0097

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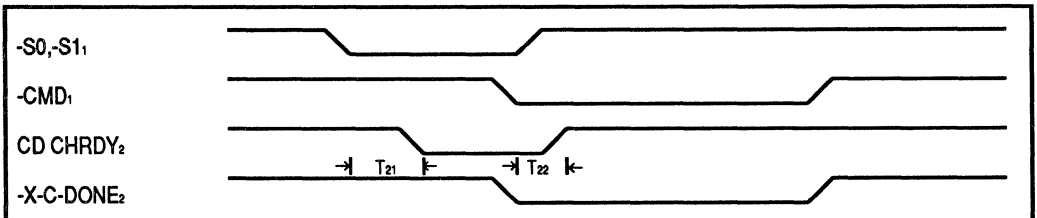
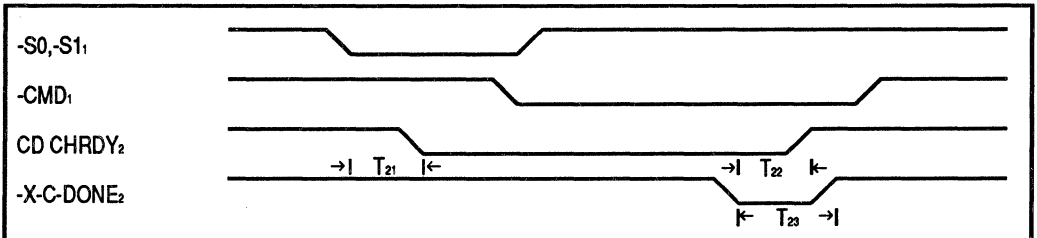


Timing Parameter	Min	Typ	Max	Units
T_{21} STATUS(-S0,-S1)$_{ACTIVE}$ —>CD CHRDY$_{INACTIVE}$	—	18	30	ns
T_{22} -X-C-DONE$_{ACTIVE}$ —>CD CHRDY$_{ACTIVE}$	—	14	25	ns

Note: For synchronous extended cycles, the DT7920 input signal "-X-C-DONE"is driven by the Microchannel signal "-CMD."

Figure 14. Extended Command Cycles: Synchronous Extended Cycles

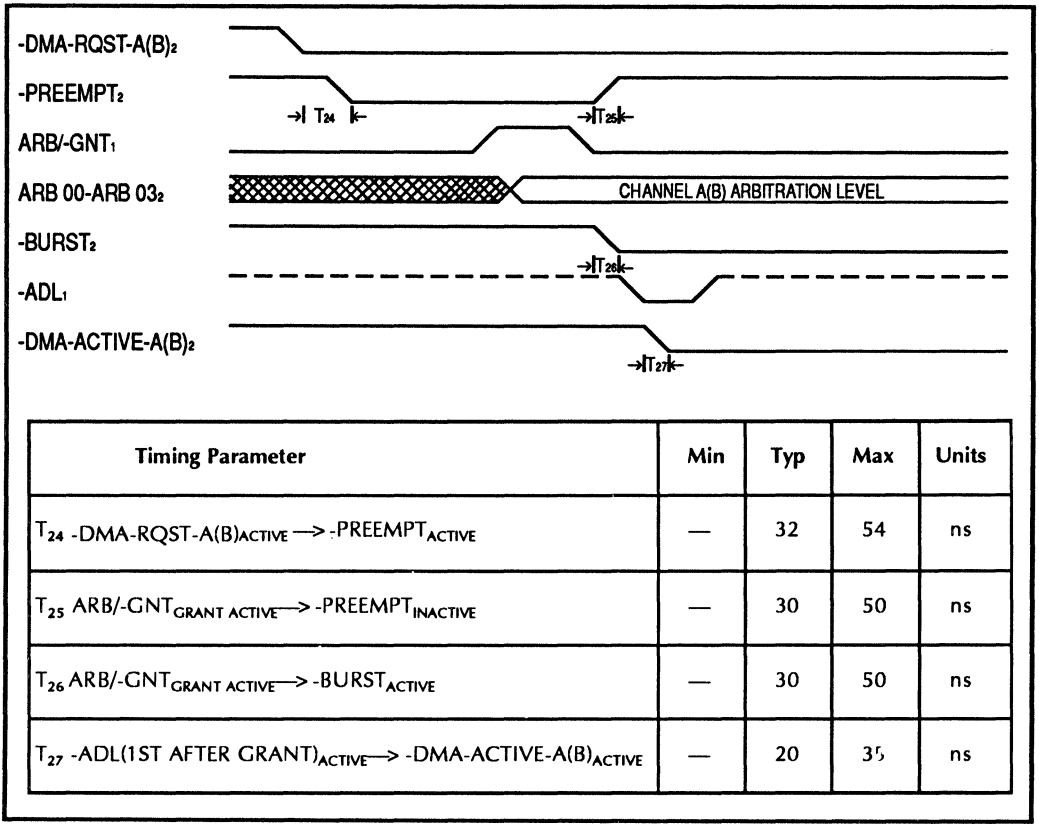
M-0098



Timing Parameter	Min	Typ	Max	Units
T_{23} -X-C-DONE$_{ACTIVE(tpw)}$	10	—	50	ns

Figure 15. Extended Command Cycles: Asynchronous Extended Cycles

M-0099



Timing Parameter	Min	Typ	Max	Units
T_{24} -DMA-RQST-A(B)$_{ACTIVE}$ —> -PREEMPT$_{ACTIVE}$	—	32	54	ns
T_{25} ARB/-GNT$_{GRANT\ ACTIVE}$—> -PREEMPT$_{INACTIVE}$	—	30	50	ns
T_{26} ARB/-GNT$_{GRANT\ ACTIVE}$—> -BURST$_{ACTIVE}$	—	30	50	ns
T_{27} -ADL(1ST AFTER GRANT)$_{ACTIVE}$—> -DMA-ACTIVE-A(B)$_{ACTIVE}$	—	20	35	ns

Figure 16. DMA: Grant Cycle

M-0100

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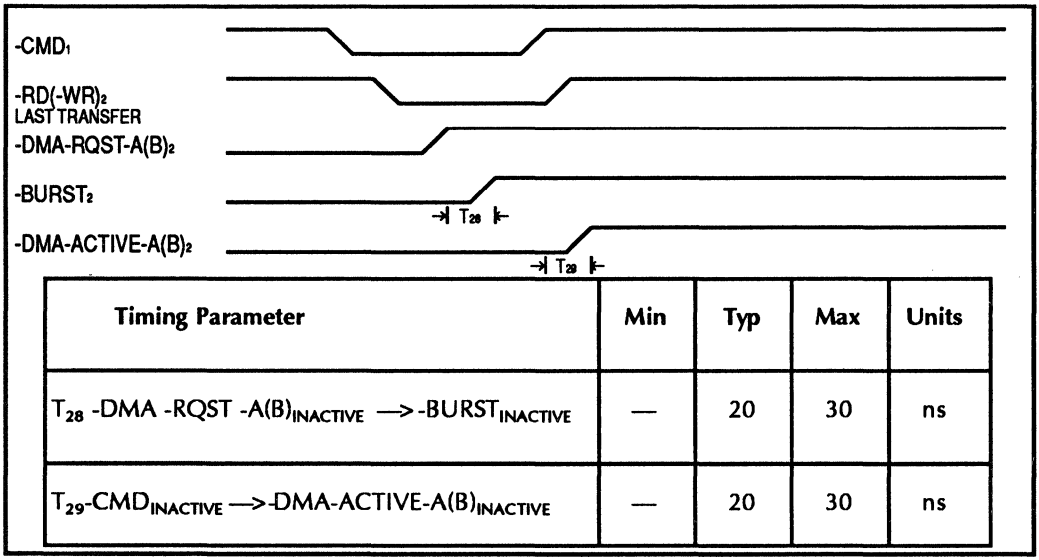

Timing Parameter	Min	Typ	Max	Units
T_{28} -DMA -RQST -A(B)$_{INACTIVE}$ —> -BURST$_{INACTIVE}$	—	20	30	ns
T_{29}-CMD$_{INACTIVE}$ —>-DMA-ACTIVE-A(B)$_{INACTIVE}$	—	20	30	ns

Figure 17. DMA: Slave Terminated Cycle M-0101

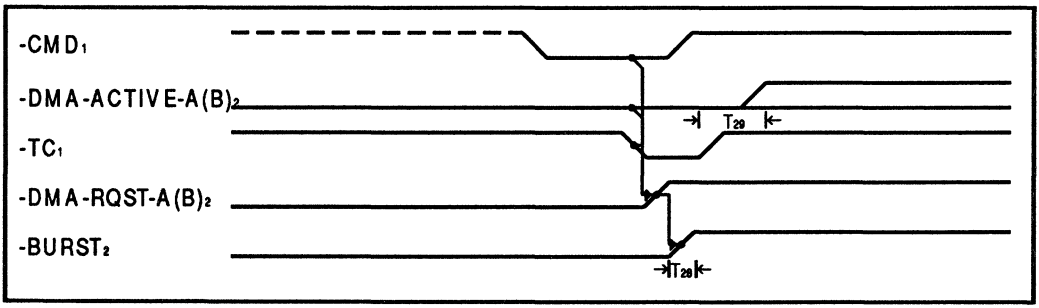

Figure 18. DMA: Controller Terminated Cycle M-0102

APPLICATIONS—INTERRUPTS

Using external circuitry, the DT7920 can be set to program-select the interrupt level on the Micro Channel. Figure 9 shows an application, using POS30 (pin 4), POS31 (pin 3), POS32 (pin 2), -READ (decoded Micro Channel -RD signal), and -WRITE (decoded Micro Channel -WR signal) to select an interrupt level for an adapter design. -IRQST (-Interrupt Request) is generated by the adapter control logic.

The flip-flop and latch make up a read/write register. Interrupt Status indicates the status of the interrupt. It reads as 1 (high) if no interrupt has occurred. It is set on powerup, whenever Micro Channel CHRESET is asserted, and by Clear Interrupt. After an interrupt has occurred, the software interrupt service routine will write a 0 to Clear Interrupt. This resets the interrupt pending latch.

Interrupt level selection is performed by POS30, POS31, and POS32 as outlined in Table 11. In the application shown, level 10 is the highest, followed by 11, 12, 3, 4, 5, 6, and 7 (the lowest). Note that specific adapter designs can select different Micro Channel interrupt request lines if different interrupt levels are desired.

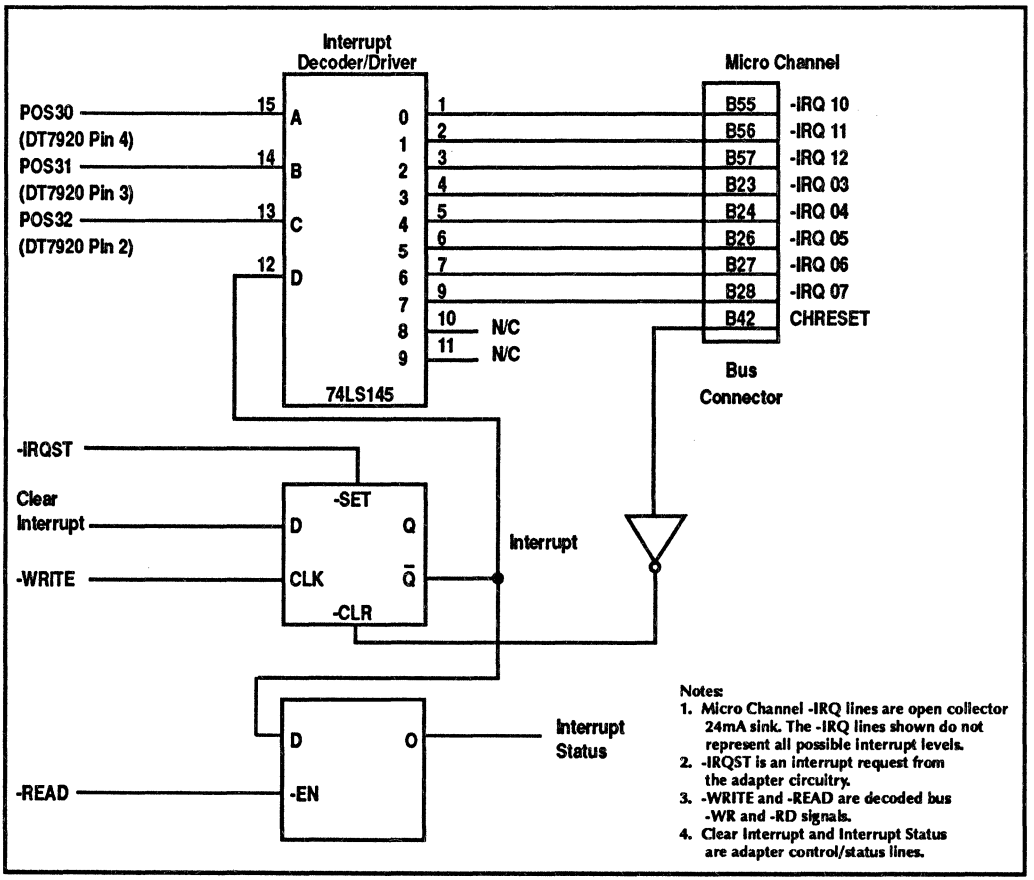

Figure 19. Interrupt Application Circuit

M-0085

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TABLE 11. INTERRUPT LEVEL SELECTION

Interrupt Level	POS 0103 Bits		
	2	1	0
10 (highest)	0	0	0
11	0	0	1
12	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

ORDERING GUIDE

DT7920

MCA Interface Chip for use on adapter boards for IBM Personal System/2 Micro Channel computers. The DT7920 implements POS registers, address and data line control for I/O transfers, complete DMA control circuitry for two independent DMA channels, and full compliance with Personal System/2 specifications. Several control lines are included for communication with adapter circuitry. The DT7920 is supplied in an 84-pin PLCC package for surface-mount or socket mounting.

DT2981

Micro Channel-compatible Development Board for adapter prototype development using the DT7920. The DT2981 is supplied with a DT7920 MCA Interface Chip mounted in a chip socket, data transceivers, a POS ID chip and socket, startup software including an Adapter Description File, a 50-pin I/O connector, and a large breadboard area for user-installed circuitry. All user signals are provided on wirewrap pins for easy access. DT7920 literature, board schematic, and application notes are also supplied.

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