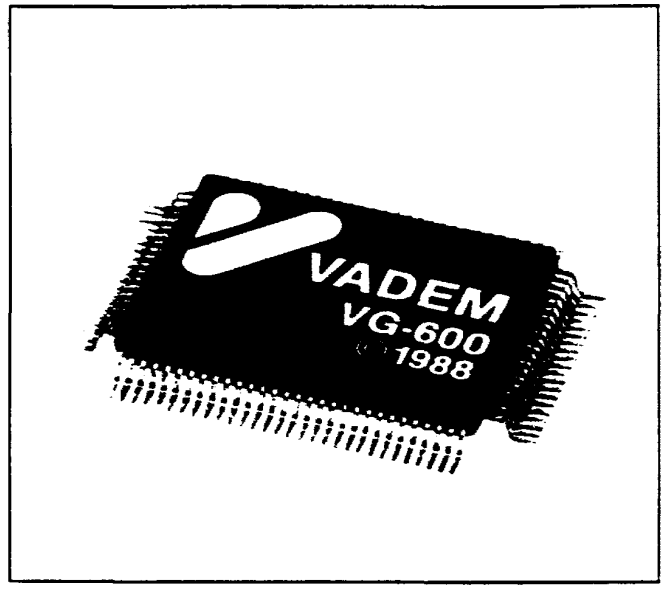
VADEM

VG-600
LCD CONTROLLER FOR PC ARCHITECTURE SYSTEMS

FEATURES

- Control for 640 x 200 or 640 x 400 LCD displays
- PC bus interface
- Single chip, requires no glue logic
- PC compatible graphics support for CGA, double scan CGA, MDA or ATT standards
- 6845 compatible I/O registers
- RAM based soft font
- ROM BIOS support for multiple character sets
- Eight level gray scale support
- Low power CMOS, single 5V supply
- 100 pin QFP package



DESCRIPTION

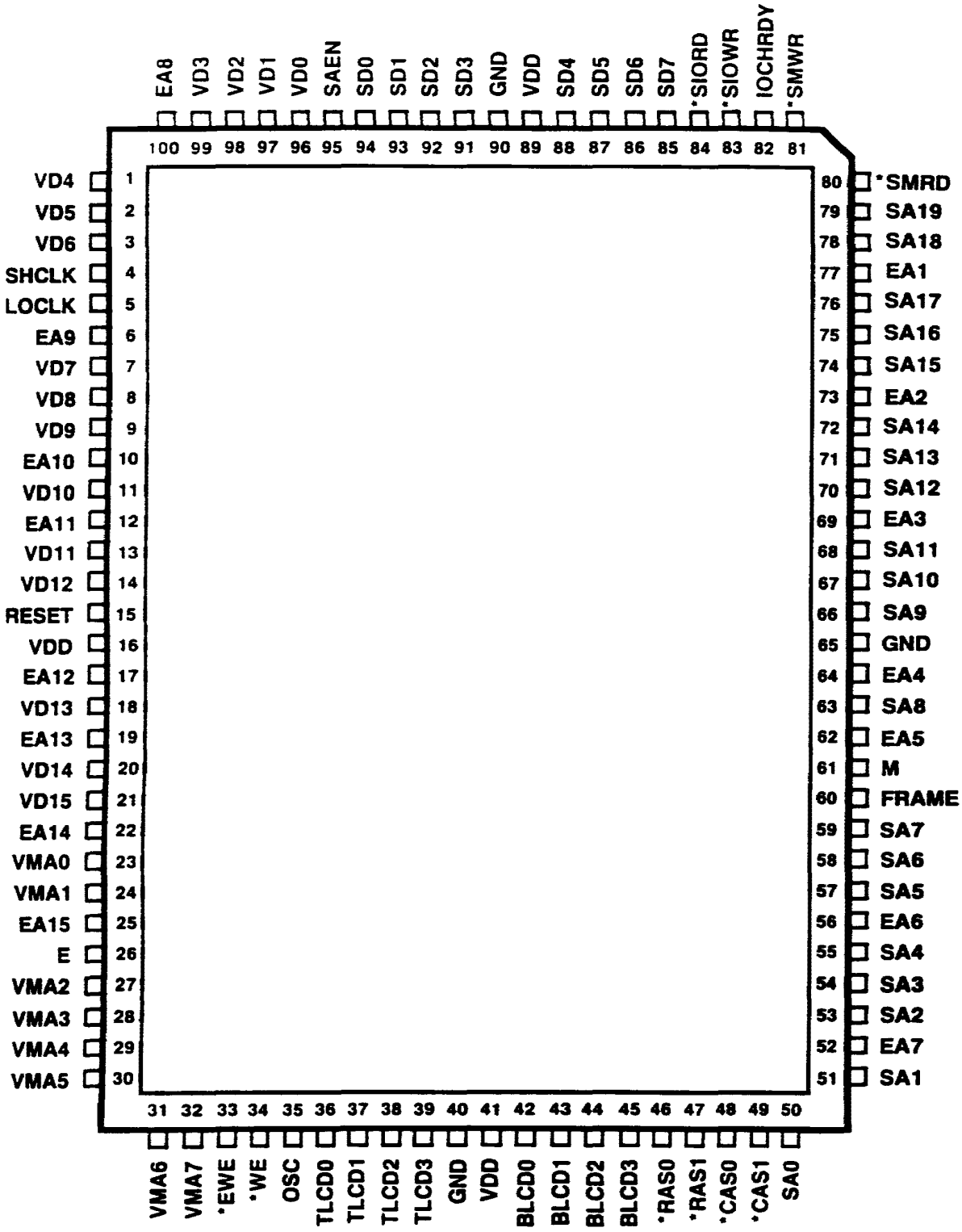
The VG-600 provides the easiest implementation and lowest cost single chip LCD controller for use in PC applications. The flexibility of the VG-600 allows use of many popular LCD displays of either 640 x 200 or 640 x 400 resolution (pin selectable). Popular PC display standards are provided, including MDA, double scan CGA, CGA and AT&T graphics standards.

The VG-600 is designed explicitly for PC applications of liquid crystal displays. And the VG-600 contains *ALL* logic necessary for the LCD interface. No external glue logic is required.

The VG-600 contains key additional features in dealing with character generation and fonts. The VG-600 provides for a soft font that is RAM based. The font is initialized by the BIOS from a font stored in ROM with the BIOS and can be easily changed to other fonts which may be loaded from disk by calling a BIOS provided utility. Support for font initialization and the utility for loading additional fonts is provided by the Vadem BIOS. In the event a non-Vadem BIOS is used, Vadem provides a small external display BIOS for font initialization and updating only.

Because the VG-600 provides LCD control with an absolute minimum component count and low power consumption, the VG-600 is the LCD controller of choice for a wide variety of applications in which size and power are critical elements. This includes all ranges of laptop personal computers and other types of dedicated, portable or handheld computer-based devices. In addition, the low cost of implementation with the VG-600 makes it ideal for other applications of LCD control, regardless of form factor or power requirements.

VG-600 PIN CONFIGURATION



VG-600 PIN DESCRIPTION

NAME	PIN	I/O	FUNCTION
SA[0..19]	50–51 53–55 57–59 63, 66–68 70–72 74–76 78–79	I	System Address bus. Selects register and memory addresses for data transfer to and from the host CPU.
SD[0..7]	94–91 88–85	I/O	System Data bus. Carries data being transferred between VG600 and host CPU.
*SMRD	80	I	Memory read strobe. When low, the VG600 places the contents of the video memory addressed by SA[0..19] onto the SD bus.
*SMWR	81	I	Memory write strobe. When low, the VG600 writes the data on SD[0..7] into video memory addressed by SA[0..19].
*SIORD	84	I	I/O read strobe. When low, the VG600 places the contents of the I/O port addressed by SA[0..9] onto the SD bus.
*SIOWR	83	I	I/O write strobe. When low, the VG600 writes the data on SD[0..7] into the I/O port addressed by SA[0..9].
IOCHRDY	82	O	I/O channel ready. Goes low during host CPU accesses to video memory to request CPU wait states as needed.
SAEN	95	I	Address enable. The host CPU drives this line high to indicate a DMA cycle is in process.
OSC	35	I	14–16.7 MHz clock. Continuous clock determines all VG600 timing. Need not be synchronous with host CPU clock.
RESET	15	I	Power on reset. Driven high by host system to initialize all internal logic and registers.
VD[0..15]	96–99 1–3 7–9 11, 13–14 18, 20–21	I/O	Video RAM data bus. Carries data being transferred between video RAM and VG600. VD[8..15] not used in 200 line mode. VD15 must be grounded to put VG600 in 200 line mode.
VMA[0..7]	23–24 27–32	O	Video DRAM address bus. Multiplexed row and column address bus for 64K×4 DRAM. Selects video memory address.
*RAS[0..1]	46–47	O	Row address strobes. When low, strobe row address on VMA[0..7] into video DRAM. RAS0 for even bank, RAS1 for odd.
*CAS[0..1]	48–49	O	Column address strobe. When low, strobe column address on VMA[0..7] into video DRAM. CAS0 for even bank, CAS1 for odd.
*WE	34	O	Write enable. When low, indicates that video memory cycle in progress is a write cycle.
TLCD[0..3]	36–39	O	LCD upper data bus. Carries pixel data for upper half of dual screen displays, or for single screen displays, from VG600 to LCD unit.
BLCD[0..3]	42–45	O	LCD lower data bus. Carries pixel data for lower half of dual screen displays from VG600 to LCD unit.
SHCLK	4	O	LCD data shift clock. On the falling edge, clocks data on TLCD [0..3] and/or BLCD[0..3] into LCD unit.
LOCLK	5	O	LCD line load clock. Indicates one line of pixels has been transferred into LCD unit.
FRAME	60	O	LCD frame sync. Indicates that line of pixels just transferred is the first line of a new frame.
M	61	O	AC drive to LCD. Square wave output required by some LCDs. Period equals two frame times.
E	26	O	Clock to LCD. Clock required by some LCDs. Frequency is 1/20 SHCLK rate.
V_{CC}	41, 89 16		+5 volt power
V_{SS}	90, 65 40		Ground
EA[1..15]	77, 73, 69 64, 62, 56 52, 100, 6 10, 12, 17 19, 22, 25	O	Even bank address bus. This is a demultiplexed VMA bus to be connected to the address lines of the even bank of video RAMs when static RAM is used instead of DRAM.
*EWE	33	O	Even bank write enable. This is a latched write enable to be connected to the write enable line of the even bank of video RAMs when static RAM is used instead of DRAM.

DISPLAY TYPES AND CLOCK RATES

Four basic display types are supported, with variations among those types. These types are 1) 400 line dual screen (1/200 multiplexing) with Sharp-type timing, 2) 400 line dual screen with generic timing, 3) 200 line dual screen (1/100) and 4) 200 line single screen (1/200). The display type is selected by the programmable LCDTYP bit and jumper selected 200LINE (VD15) bit according to the following table:

200LINE	LCDTYP	LINES	MUX	CLOCKS	REFR	NOTES
0	0	400	1/200	15	60/70	Sharp
0	1	400	1/200	15	60/70	Generic
1	0	200	1/100	25	71.7	Dual
1	1	200	1/200	25	71.7	Single

The CLOCKS and REFR columns in the table describe the timing cycle in terms of the number of VOSC clocks and the frame refresh rate. In general, VOSC is 14.318 MHz, except for certain 400 line displays which require a 16.7 MHz clock to meet their 70 Hz refresh rate spec. The 14.31818 MHz clock duty cycle range is 40% to 60%. Faster clocks MUST have a 50% duty cycle. It is important to note that in 80 column text modes using 200 line displays, only one host access per 25 clocks is allowed.

For 400 line displays such as Sanyo which require a 70 Hz refresh rate, higher clock rate of 16.7 MHz is necessary. This reduces the clock period from 70 ns to 60 ns, and therefore 100 ns DRAM for video RAM is required. At this speed, even with the 50% duty cycle requirement, certain timing margins are narrow. The worst case is tRP. The VG600 can theoretically provide 90 ns assuming perfectly matched internal delays, and the minimum requirement is 80 ns for Fujitsu and 90 ns for NEC parts. tRAS cannot be shaved much to compensate for this, because the VG600 theoretically provides 120 ns and the devices required 100 ns.

VIDEO MEMORY CONFIGURATION

400 Line DRAM Configuration

A 400 line display requires 128 Kbytes of DRAM, configured as 4 64K x 4 DRAMs. The multiplexed row/column address bus is VMA[0..7]. The DRAM data bus is VD[0..15]. The DRAM array is divided into an even addressed bank (VA0 is reset) and an odd addressed bank (VA0 is set). The addresses are multiplexed such that VA1 and VA9 are multiplexed onto VMA0, and so on until VA8 and VA16 are multipexed onto VMA7. *VRAS0 and *VCAS0 are the row and column address strobes signal for the even bank; *VRAS1 and *VCAS1 are the row and column address strobes for the odd bank. *WE is the write enable signal for both banks. The output enable signals for both DRAM banks are always active.

The 128 Kbytes is divided into several sections:

VA Address Range	Contents	Map [1..0]	SA
[00000H..07FFFH]	Display Buffer	00	0-7FFF
[08000H..0BFFFH]	Character Generator Regular	01	0-3FFF
[0C000H..0FFFFH]	Character Generator Enhanced	01	4000-7FFF
[10000H..17FFFH]	Private Memory	10	0-7FFF
[18000H..1FFFFH]	Private Memory	11	0-777F

Private Memory is for the exclusive use of the ROM BIOS. It may be only accessed through the SA memory address range [E8000H..EFFFFH] when MAP[1..0] are set as in the table.

In MDA mode, the lower 4 Kbytes of the Display Buffer, [00000H..00FFFH] is exactly the same as the IBM compatible 4 KByte MDA Display Buffer at the SA address [B0000H..B0FFFH]. The remaining 28 Kbytes [01000H..07FFFH] are unused. In ATT mode, the Display Buffer is exactly the same as the ATT compatible 32 Kbyte Display Buffer at the SA

address [B8000H..BFFFFH]. The display buffer may also be accessed through the SA memory address range [E8000H..EFFFFH] when MAP0 and MAP1 are reset.

The Regular and Enhanced Character Generators may be accessed through the SA address range. [E8000H..EFFFFH] when MAP1 is reset and MAP0 is set. The Regular and Enhanced Character Generators each have four 4 Kbyte character sets:

VA Address Range	SA	Character Set
[08000H..08FFFH]	0000-0FFF	A normal
[09000H..09FFFH]	1000-1FFF	A underline
[0A000H..0AFFFH]	2000-2FFF	B normal
[0B000H..0BFFFH]	3000-3FFF	B underline
[0C000H..0CFFFH]	4000-4FFF	A enhanced
[0D000H..0DFFFH]	5000-5FFF	A enhanced underline
[0E000H..0EFFFH]	6000-6FFF	B enhanced
[0F000H..0FFFFH]	7000-7FFF	B enhanced underline

Each character set has 256 characters. Each character has 16 character scan lines. Each character scan line is one byte. SA[0..3] addresses the scan lines in the usual order, with the first byte corresponding to the top scan line. VA[0..3] addresses the scan lines in a different order. The top eight scan lines are contained in the even addressed banks (VA0 reset), while the bottom eight scan lines are contained in the odd addressed banks (VA0 set). This is accomplished by hardware mapping SA3 to VA0 and SA0 to VA3 for system accesses to the character generator area. Bit 7 corresponds to the leftmost pixel of a scan line. Characters with the intense attribute use the Enhanced Character Generator. Characters without the intense attribute use the Regular Character Generator.

400 Line Static RAM Configuration

Static RAM may also be used with the VG600. If private memory is not needed, only two 32K x 8 RAMs are required, one for the odd and one for the even bank; otherwise four RAMS are required. Where only 2 RAMS are used two octal latches, two inverters, and a NOR gate are required. EA[1..15] are connected to A[0..14] on the even RAM. If the RAMs are battery backed, add one OR gate per RAM for power down disabling. The external logic must be 74AC series. 120 ns RAM will suffice if the clock rate is 14.31818 MHz. A 16.7 MHz clock requires 100 ns RAM.

200 Line DRAM Configuration

A 200 line display requires only the lower 64 Kbytes of DRAM. The VD15 pin must be jumpered to ground to put the VG600 in 200 line mode. The state of this pin is checked only while the RESET pin is high. The multiplexing of the VMA bus is different in 200 line mode, but this has no effect on system operation. Since there is only one 64 Kbyte bank VA0 becomes a memory address bit instead of a bank select, and VA16 is no longer used. VA1 and VA9 are still multiplexed onto VMA0, and so on until VA7 and VA15 are multiplexed onto VMA6. However, VA0 and VA8 are now multiplexed onto VMA7.

The 64 Kbytes is divided into 4 sections:

VA Address Range	Contents	MAP [1..0]	SA
[0000H-3FFFH]	Display buffer	00	0000-3FFF
[4000H-5FFFH]	Character generator MDA	00	4000-5FFF
[6000H-7FFFH]	Character generator ATT	00	6000-7FFF
[8000H-FFFFH]	Private memory	01	0000-7FFF

Private memory is as described in a previous section.

In MDA mode, the lower 4 Kbytes of the Display Buffer, [0000H..0FFFH] is exactly the same as in IBM compatible 4 Kbyte MDA Display Buffer at the SA address [B000H..B0FFFH]. The remaining 12 Kbytes are unusable. In ATT mode, the Display Buffer is exactly the same as the CGA compatible buffer at the SA address [B8000H..BBFFFH]. The display buffer and the character generators may also be accessed through the SA memory address range [E8000H..EFFFFH] when MAP0 is reset.

The 200 line character generators are organized as follows:

SA and VA Address Range	Character Set
[4000H..4FFFH]	A, regular and enhanced
[5000H..5FFFH]	A, underline and enhanced underline
[6000H..6FFFH]	B, regular and enhanced
[7000H..7FFFH]	B, underline and enhanced underline

Each character has 8 character scan lines, each of which is one byte. Ordinarily a 200 line character set would be half the size of a 400 line set, but to

simplify the chip design, the number of bytes per character in the character set was kept the same by interleaving the regular and enhanced character generator sets to combine them into one. The 200 line character sets therefore consist of 256 pairs of characters, where the first character of each pair (SA3 = 0) is the standard font, while the second (SA3 = 1) is the same character but in enhanced font. SA[0..3] addresses the scan lines in the usual order, with the first byte corresponding to the top scan line. VA[0..3] addresses the scan lines in a different order. The normal font scan lines are contained in the even addressed banks (VA0 reset), while the enhanced font lines are contained in the odd addressed banks (VA0 set). This is accomplished by hardware mapping SA3 to VA0 and SA0 to VA3 for system accesses to the character generator area. Bit 7 corresponds to the leftmost pixel of a scan line. As in 400 line mode, characters with the intense attribute use the enhanced font.

200 Line Static RAM Configuration

Static RAM may also be used with the VG600. If private memory is not needed, only one 32K x 8 RAM is required, otherwise two RAMs are required. Where only one RAM is used, no glue logic is required. The RAM address lines are connected to the EA[1..5] Bus. Due to the multiplexing differences described in the previous section, EA[1..7,9..14] correspond to nominal memory addresses [1..7,9..14] but EA8 corresponds to A0 and EA15 corresponds to A8. If the RAMS are battery backed, add one OR gate for power down disabling. 120 ns RAM will suffice if the clock rate is 14.31818 MHz. A 16.7 MHz clock requires 100 ns RAM.

GRAPHICS SOFTWARE CONSIDERATIONS

6845 Compatible IO Registers

Both the MDA mode and the ATT mode use 6845 Compatible IO registers. The 6845 compatible IO registers occupy two byte wide IO locations, mirrored four times over an eight byte range. In MDA mode these are at 3B4H for the Index Register and 3B5H for the Data Register with a range of 3B0H to 3B7H. In ATT alpha modes these are at 3D0H for the Index Register and 3D1H for the Data Register, also mirrored three more times over the range 3D2H to 3D7H. The same physical registers are used for the MDA mode and for the ATT alpha modes. These registers are not used in ATT APA modes, but the VG600 hardware expects the firmware to set the Display and start Address Registers to 0 in APA modes. The 8-bit Index Register (IR) is used to select the internal 6845 register that may be accessed through the Data Register (DR). The VG600 implements the following internal 6845 registers:

Index	Register	Bits
0AH	Cursor start Scan Line	7
0BH	Cursor End Scan Line	5
0CH	Display start Address MSB	6
0DH	Display start Address LSB	8
0EH	Cursor Address MBS	6
0FH	Cursor Address LSB	8
10H	Light pen dummy register	8
11H	Light pen dummy register	8

CSSL[5..6] cursor control functions are implemented as in the IBM spec, not as the 6845 uses them. See the table later in this section. CSSL[0..4] determines the scan line that the cursor starts on. CESL[0..4] determines the scan line that the cursor ends on. For 400 line displays in ATT modes CSSL and CESL are doubled and CESL is then incremented by one. For 200 line displays in MDA mode CSSL and CESL are halved. DSA[0..13] is used in determining the address of the upper left character of the display. CSA[0..13] is used in determining the address of the cursor. Light pen dummy registers 10H and 11H are read-only and return a value of 0. For values of IR[0..4] other than [0AH..11H,0CAH..0CFH]; the DR is undefined when read and ignored when written. Unlike the 6845, IR[5..7] are significant when written to allow access to the special VG600 registers. Assertion of the RESET signal will reset all IR, CSSL, CESL, DSA and CSA bits.

The configuration and palette registers in the chip are accessed the same way as the 6845-compatible registers. LCDCFA and LCDCFB are the configuration registers. The palette registers hold the gray scale shading used in ATT text and 320 x 200 graphics modes.

Index	Register
0CAH	Palette 0 and 1
0CBH	Palette 2 and 3
0CCH	Palette 4 and 5
0CDH	Palette 6 and 7
0CEH	LCDCFA
0CFH	LCDCFB

The bit definitions for LCDCFA and LCDCFB are:

Bit(s)	Signal(s)
LCDCFA0	ATT
LCDCFA1	LCDTYP
LCDCFA2	*LCDREN
LCDCFA3	200 LINE
LCDCFA4	RVVD
LCDCFA5	PVTMEM
LCDCFA[6..7]	MAP[0..1]
LCDCFB[0..2]	RESERVED
LCDDFB3	CHARSETB
LCDCFB[4..5]	CURBLK[0..1]
LCDCFB[6..7]	ATTBLK[0..1]

Assertion of the RESET signal will reset LCDCFA[2, 4..7] and LCDCFB[0..7] and set LCDCFA[0,1].

LCDCFA0 is the ATT bit. When ATT is set, the LCD video subsystem is ATT compatible; when ATT is reset, the LCD video subsystem is MDA compatible.

LCDCFA1 and LCDCFA3 indicate the type of LCD display to be connected. The display type is selected by the LCDTYP[0,1] bits according to the table in section 2.

LCDCFA2 is the *LCDREN bit. The LCD video subsystem always allows writing to both the LCD DRAM and the LCD I/O registers. All writeable registers in the VG600 are capable of being read. The *LCDREN bit determines when the VG600 responds to read accesses. If *LCDREN is set then the VG600 will not respond to read accesses to the I/O ports or to the display memory area in DRAM. If *LCDREN is reset the VG600 will respond to all read accesses.

LCDCFA4 is the RVVD bit. When RVVD is reset, the LCD image is normal — a one produces a one in the LCD data stream. When RVVD is set, the LCD image is reversed — a zero produces a one in the LCD data stream.

LCDCFA5 is the PVTMEM bit. When PVTMEM is set, the 32 Kbyte video DRAM section specified by MAP[0..1] may be accessed in the [E8000H..EFFFFH] memory address range. When PVTMEM is reset, accesses to [E8000..EFFFF] will be ignored.

LCDCFA[6..7] are MAP[0..1]. MAP1 has no effect if a 200 line display is used. MAP[0..1] is used to specify which of the four 32 Kbytes sections of Video DRAM is mapped into the [E8000H..EFFFFH] memory address range. Refer to the tables in the Memory Configuration sections for the usage of these bits.

LCDCFB[4..5] are CURBLK[0..1]. CURBLK[0..1] are used in conjunction with bit 5 of the Curser start Scan Line Register, CSSL5, to control cursor blinking in text modes:

CSSLR6	CSSLR5	CURBLK1	CURBLK0	Cursor Mode
X	1	X	X	Not displayed
X	0	0	0	Steady
X	0	0	1	1/64 frame rate blink
X	0	1	0	1/32 frame rate blink
X	0	1	1	1/16 frame rate blink

LCDCFB[6..7] are ATTBLK[0..1]. ATTBLK[0..1] are used to control the blinking rate of characters displayed with the blinking attribute in text modes:

ATTBLK1	ATTBLK0	Blink Rate
0	0	Steady
0	1	1/64 frame rate blink
1	0	1/32 frame rate blink
1	1	1/16 frame rate blink

The palette registers are organized as four 8 bit registers, each containing two 4 bit grayscale codes. The even palette register occupies the lower nibble of the register, and the odd palette register occupies the upper nibble. The usage of the palette registers is described in the ATT Mode section.

MDA Mode

When MDA mode is selected, the VG600 responds to I/O accesses in the [3B0H..3BBH] range. The I/O port at 3B4H is the 6845 compatible write only 8-bit Index Register (IR). The I/O port at 3B5H is the 6845 compatible Data Register (DR). DSA[0..10] *2 is the word address of the upper left corner character/attribute.

The write only 2-bit MDA CRT Control Port (MDAC) is at I/O address 3B8H. A set MDAC3 enables video, a reset MDAC3 disables video. A set MDAC5 enables the blinking attribute; a reset MDAC5 disables the blinking attribute. MDAC[0..2,4,6..7] are ignored when written. Assertion of the RESET signal will reset MDAC[3,5].

The read only 2-bit MDA CRT status Port (MDAS) is at I/O address 3BAH. MDAS0 is HSYNC. The VG600 generates a synthesized HSYNC pulse approximately 7 or 8 microseconds wide for this purpose. MDAS3 in the IBM MDA board is the video output. In the VG600 it is the logical or of all 8 pixels written to the LCD. MDAS[1..2,4..7] are zero when read. Assertion of the RESET signal will reset MDAS[0,3].

When MDA mode is selected, the VG600 responds to memory accesses in the [B0000H-B7FFFH] range. The VG600 addresses the memory contents in exactly the same fashion as an MDA adaptor. The 4 Kbyte [B0000H..B0FFFH] range is mirrored eight times to fill the 32 Kbyte [B0000H..B7FFFH] range. This mirroring does not occur when the display buffer is accessed through [E8000H..EFFFFH].

The MDA attribute byte, MDAAT[0..7], controls how the character is displayed. If MDAAT7 and MDAC5 are set, then the character blinks at the rate specified by ATTBLK[0..1]. When the character blinks off, the font lookup character will be 20H. If MDAAT3 is set then the Enhanced Character Generator is used; otherwise the Regular Character Generator is used. MDAAT[0..2,4..6] determine the way that the character is displayed. The MDA underline character set is used, if MDAAT0 is set and MDAAT[1..2,4..6] is reset. Otherwise the normal character set is used. The character is hidden if MDAAT[0..2,4..6] are all reset. The Character is displayed in reverse video, if MDAAT[0..2] are reset and MDAAT[4..6] are set.

ATT IO Registers and Memory

When ATT mode is selected, the LCD subsystem responds to IO accesses in the [3D0H..3DFH] range. The IO port at 3D0H is the 6845 compatible write only 8-bit Index Register (IR). The IO port at 3D1H is the 6845 compatible Data Register (DR).

The write only 5-bit ATT Mode Select Register A (ATTMSA) is at IO address 3D8H. The bit definition for this register is:

Bit	Name	Setting	Function
0	CRES	0	40 x 25 Alpha
		1	80 x 25 Alpha
1	GRAPH	0	Character Mode
		1	Graphics Mode
3	VIDE	0	Video disabled
		1	Video enabled
4	GRES0	0	320 x 200 APA
		1	640 x 200 or 640 x 400 APA
5	BLINK	0	MSB of attribute is intensity
		1	MSB of attribute is blink

ATTMSA[2,6..7] are ignored when written. Assertion of the RESET signal will reset ATTMSA[0..1,3..5].

The VG600 does not implement the Color Select Register at 3D9H. This register is used in a CGA adapter or specify the colors used in graphics mode. The VG600 uses black for the foreground color and white for the background color in both 640 x 200 and 640 x 400 graphics modes. However, in 320 x 200 mode and text mode the pixels and characters can be modified by shading, using shade codes stored in the palette registers. Using methods described under those display modes, the VG600 selects a shading method from one of the palette registers and modifies the display accordingly.

Shading is done by logically ANDing the pixels being displayed with shading signals. Shading can be done in three ways: grayscaling, crosshatching, and combinations by the two. In grayscaling a pixel is duty cycle modulated over an integral number of display frames, by ANDing it with a time varying pattern that repeats every 6 frames in X/3 modulation and every 8 frames in X/4 modulation. The X/4

pattern size is 4 x 4 pixels, the X/2 pattern is 2 x 2 pixels, and X/3 pattern size is 4 x 2 pixels. In cross-hatching the pixels in a 4 x 4 area are ANDed with a pattern to turn off those that coincide with 'off' pixels in the pattern. Three patterns are provided. One is a checkerboard with every other pixel off. Another is a slash, where the 4 pixels in a line from the bottom left to top right corner of the 4 x 4 square are "off." The other is a backslash, where the 4 pixels in a line from the top left to bottom right corner are "off." Combinations are provided where the pattern is ORed with a duty cycle signal and the result is ANDed with the raw pixel data. The result turns the pixels that were turned off by the pattern back on for part of the time, so they become gray instead of completely off. The other type of combination ANDs the pattern with the duty cycle signal and the result in ANDed with the raw pixel data. The result is that the pattern turns some of the pixels off, and the ones that remain on become gray. The shade codes are:

Code	Pattern	ON Time	Logic Function
0000		1	Data AND 1
0001		1/4	Data AND Time
0010		1/2	Data AND Time
0011		3/4	Data AND Time
0100		1/3	Data AND Time
0101		2/3	Data AND Time
0110	/	1/2	Data AND (Pattern OR Time)
0111	/		Data AND Pattern
1000	Check	1/4	Data AND (Pattern OR Time)
1001	Check	1/2	Data AND (Pattern AND Time)
1010	Check	1/2	Data AND (Pattern OR Time)
1011	Check		Data AND Pattern
1100	\	1/4	Data AND (Pattern OR Time)
1101	\	1/2	Data AND (Pattern AND Time)
1110	\	1/2	Data AND (Pattern OR Time)
1111	\		Data AND Pattern

The read only 2-bit ATT status Register (ATTS) is at IO address 3DAH. ATTS0 is the logical OR of HSYNC and VSYNC. HSYNC is approximately 7 or 8 microseconds while VSYNC is approximately 170 microseconds, depending on display mode and OSC frequency. ATTS3 is VSYNC. ATTS[4..7] are one and ATTS[1..2] are zero when read.

The VG600 does not support a light pen. The IO ports at [3DBH..3DDH,3DFH] are ignored when read or written.

The write only 3-bit ATT Mode Select Register B (ATTMSB) is at IO address 3DEH. The bit definition for this register is:

Bit	Name	Setting	Function
0	GRES1	0	640 x 200 APA, two 16K alpha pages
		1	640 x 400 APA, one 32K alpha page
3	PAGSEL	0	Select low page for displaying
		1	Select high page for displaying
6	UNDRLN	0	Underline disabled
		1	Underline enabled

If a 200 line display is used, setting GRES1 or PAGSEL will have no effect, and the VG600 will be CGA compatible rather than ATT compatible.

ATTMSB[1..2,4..5,7] are ignored when written. Assertion of the RESET signal will reset ATTMS[0,3,6].

GRAPH, CRES and GRES[0..1] are used to select the ATT mode:

GRAPH	CRES	GRES1	GRES0	ATT Mode
0	0	X	X	40 x 25 Alpha
0	1	X	X	80 x 25 Alpha
1	X	X	0	320 x 200 APA
1	X	0	1	640 x 200 APA
1	X	1	1	640 x 400 APA

In 400 line display mode the entire 32 Kbyte display buffer may be accessed through the SA range [B8000H..BFFFFH]. If a 200 line display is used the 16 Kbyte display buffer may be accessed in the range [B8000H..BBFFFH]. There is no mirroring in true ATT modes, and is mirrored at [BC000..BFFFFH] exactly like a CGA.

ATT Alpha Modes

There are two ATT alpha modes: 40 x 25 and 80 x 25. The method of character/attribute memory mapping is the same as for CGA alpha modes. If GRES1 is set, then all of the 32 Kbyte Display Buffer is available for display. DSA[0..13] * 2 is the

address of the upper left corner character/attribute. If GRES1 is reset, the PAGSEL determines whether the upper or lower half of the Display Buffer is used. If PAGSEL is reset, then DSA[0..12] * 2 is the address of the upper left corner character/attribute and display wraparound occurs from the middle 16 Kbyte boundary of the Display Buffer to the start of the Display Buffer. If PAGSEL is set, then ((DSA[0..12] * 2) + 4000H) is the word address of the upper left corner character/attribute and display wraparound occurs from the end of the Display Buffer to the middle of the Display Buffer. If a 200 line display is used, the VG600 behaves as if GRES1 and PAGSEL are always low.

If underline is enabled, then the ATT attribute byte, ATTAT[0..7], is interpreted in the same way as the MDA attribute byte, MDAAT[0..7]. If underline is disabled, then ATTAT[0..7] may be used to display the character using shading. If ATTAT3 is set, then the Enhanced Character Generator is used; otherwise the Regular Character Generator is used.

If underline is disabled, the attribute bits can be used to display the characters with shading. To do this, the foreground color attribute bits are each logically or'ed with their corresponding background color bits to form a 3 bit code. The palette register indicated by this code is read, and the character is displayed using the shading method whose code is stored in that palette register. The foreground color attribute bits ATTAT[0..2] are also compared to the background color bits ATTAT[4..6] and if they are equal and of equal itensity, the character is not displayed by forcing the font lookup character to be a space. In addition, if the foreground bits ATTAT[0..3] are less than the background bits ATTAT[4..7] the final pixel output is inverted after shading has been applied. For purpose of this comparison, ATTAT7 is considered to be low if ATTMSA5 (blink) is high. The table below shows the palette register selected by the code generated by or'ing the attribute bits.

Attribute Bits			
6+2	5+1	4+0	Palette Register
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

ATT APA Modes

There are three ATT APA modes 320 x 200, 640 x 200 and 640 x 400. 400 line graphics mode requires a 400 line display. If a 200 line display is used, the VG600 behaves as if PAGSEL and GRES1 are low. The pixel to memory mapping for the 320 x 200 and 640 x 200 modes is the same as those modes in a CGA adapter. For the 320 x 200 and 640 x 200 modes, GRES1 is reset. PAGSEL determines whether the upper or the lower half of the Display Buffer is used. If PAGSEL is reset, the lower half of the Display Buffer is used and display wraparound occurs from the middle of the Display Buffer to the start of the Display Buffer. If PAGSEL is set, then the upper half of the Display Buffer is used and display wraparound occurs from the end of the Display Buffer to the middle of the Display Buffer.

The pixel to memory mapping for the 640 x 400 mode is the same as the 640 x 400 mode of the ATT adapter. (0 MOD 4) horizontal lines appear in the [B8000H..B9F3FH] address range. (1 MOD 4) horizontal lines appear in the [BA000H..BBF3FH] address range. (2 MOD 4) horizontal lines appear in the [BC000H..BDF3FH] address range. (3 MOD 4) horizontal lines appear in the [BE000H..BFF3FH] address range. For this mode GRES1 is set and PAGSEL has no effect.

Each pixel in the 320 x 200 graphics mode is represented by a 2 x 2 block of LCD screen pixels on a 400 line display, or by a 2 x 1 block on a 200 line display. In 320 x 200 graphics mode, the VG600 uses the following C[0..1] to read the shade from the indicated palette register, and displays the pixels using that shading:

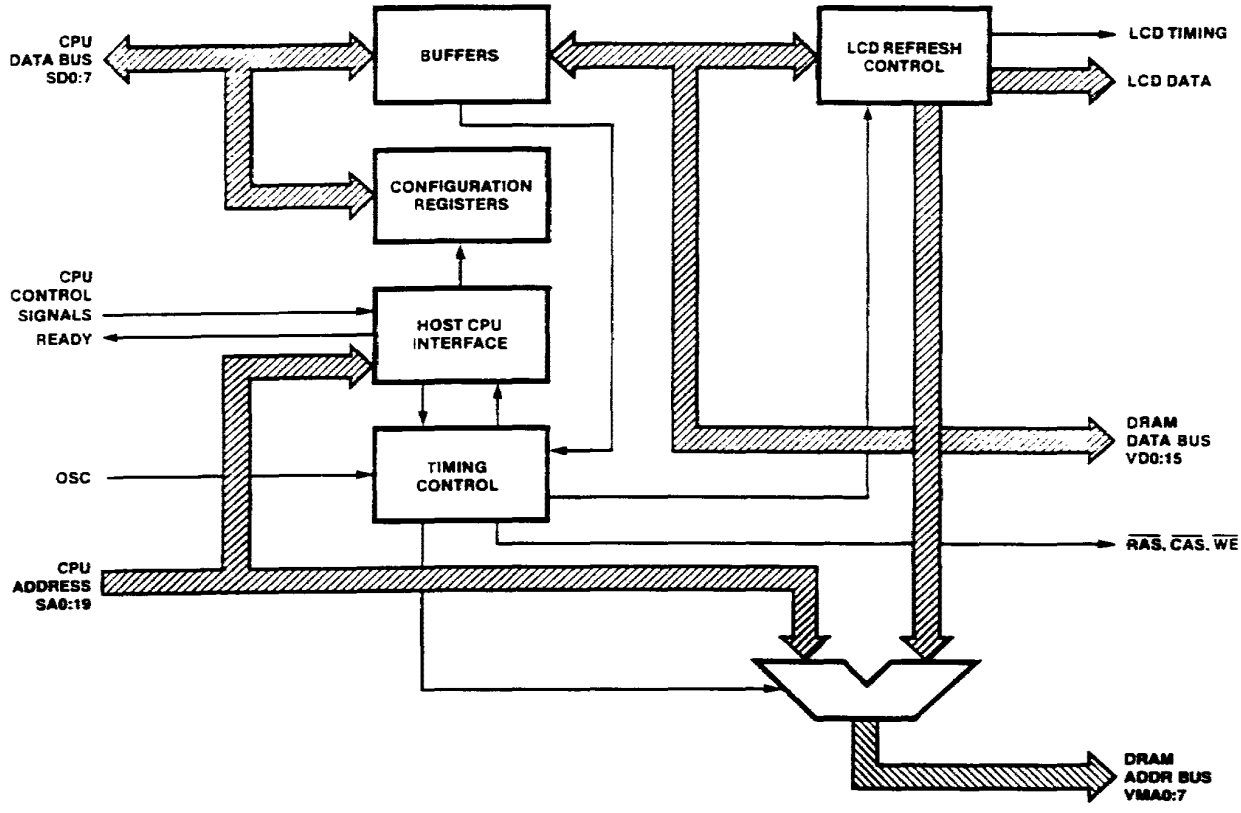
C1	C0	Palette Register
0	0	NA — displays background color
0	1	3
1	0	5
1	1	7

IO Addresses

Address Range	Register
03B0H..03BBH	VIDEO IO, MDA MODE
03BFH VIDEO	IO, MDA MODE
03D0H..3DFH	VIDEO IO, ATT MODE

IO addresses are to be decoded using only SA[0..9], qualified by AEN = 0.

VG-600 BLOCK DIAGRAM



VG-600
LCD CONTROLLER FOR PC ARCHITECTURE SYSTEMS

VG-600 OUTPUT CURRENT DRIVE CAPABILITIES

All VG-600 outputs are designed with IOL/IOH at 6/3 mA except for IOCHRDY at 12/0 mA and SHCLK, LOCLK, E, TLCD [0:3], BLCD [0:3], FRAME, M, SD [0:7] at 12/6 mA.

VG-600 MAXIMUM CAPACITANCE LOADING

Maximum Output Load (pF)	Pin
50	VD[0:15], VMA[0:7], *RAS[0:1] *CAS[0:1], *WE, EA[1:15], *EWE
150	SA[0:19], SD[0:7], *SMRD, *SMWR, *SIORD, *SIOWR, IOCHRDY, SAEN, OSC, RESET
200	TLCD[0:3], BLCD[0:3], SHCLK, LOCLK, FRAME, M, E

ABSOLUTE MAXIMUM RATINGS ($T_A = 25°C$)

Parameter	Symbol	Min	Max	Unit
Power supply voltage	V_{CC}	0	7.0	V
Input voltage	V_{IN}	-0.5	5.5	V
Output current	V_O	-0.5	V_{CC}	V
Operating temperature range	T_{op}	-25	85	°C
Storage temperature range	T_{stg}	-40	125	°C

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Limits		Unit
		Min	Max	
Power Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_a	0	70	°C
Low-level Input Voltage	V_{IL}		0.8	V
High-level Input Voltage	V_{IH}	2.0		V

DC CHARACTERISTICS

Parameter	Symbol	Limits		Unit	Test Conditions
		Min	Max		
Low-level Output Voltage	V_{OL}	—	0.45	V	TTL and CMOS
High-level Output Voltage	V_{OHT}	2.4	—	V	TTL
High-level Output Voltage	V_{OHC}	3.0	—	V	CMOS
Low-level Input Current	I_{IL}	—	-200	μA	
High-level Input Current	I_{IH1}	—	20	μA	V_{IN}=2.4V, V_{CC}=5.5V
High-level Input Current	I_{IH2}	—	200	μA	V_{IN}=5.5V, V_{CC}=5.5V
Output Short Circuit Current	I_{DS}	—	-100	mA	V_O=0V
Input Clamp Voltage	V_{IC}		-1.5	V	I_I=-20mA, V_{CC}=4.5V
Output Leakage Current	I_{OLZ1}	-100	100	μA	Hi-Z
Output Leakage Current	I_{OLZ2}	-200	200	μA	Bidirectional
Clock Input Low Voltage	V_{ILC}	—	0.4	V	
Clock Input High Voltage	V_{IHC}	4.0	—	V	
Electro-Static Voltage	V_{ESD}	—	2000	V	
Operating Current	I_{op}	—		mA	
Operating Frequency	I_{FRO}	—	16.7	MHz	

VG-600 TIMING CHARACTERISTICS

CPU Interface and I/O Access Timing

No.	Parameter	Symbol	Min	Max	Unit	Comment
t_{600}	Command to IOCHRDY low	T_{CRDY}		25	ns	
t_{601}	Address set up time	T_{SAS}	0		ns	
t_{602}	Address hold time	T_{SAH}	0		ns	
t_{603}	Memory read data set up time	T_{RDS}	10		ns	
t_{604}	Memory read data hold time	T_{RDH}		10	ns	
t_{605}	Memory write data delay table	T_{WDD}	200		ns	
t_{606}	Memory write data hold time	T_{WDH}	0		ns	
t_{607}	SD bus to VD bus through delay	T_{SDVD}		25	ns	
t_{608}	I/O cycle address set up time	T_{IOAS}	0		ns	
t_{609}	I/O cycle address hold time	T_{IOAH}	10		ns	
t_{610}	I/O read access time	T_{IOAC}		60	ns	
t_{611}	I/O read data hold time	t_{IODH}		10	ns	
t_{612}	I/O write data set-up time	t_{IOWDS}	50		ns	
t_{613}	I/O write data valid time	t_{IOWDH}	10		ns	

RAM Interface Timing

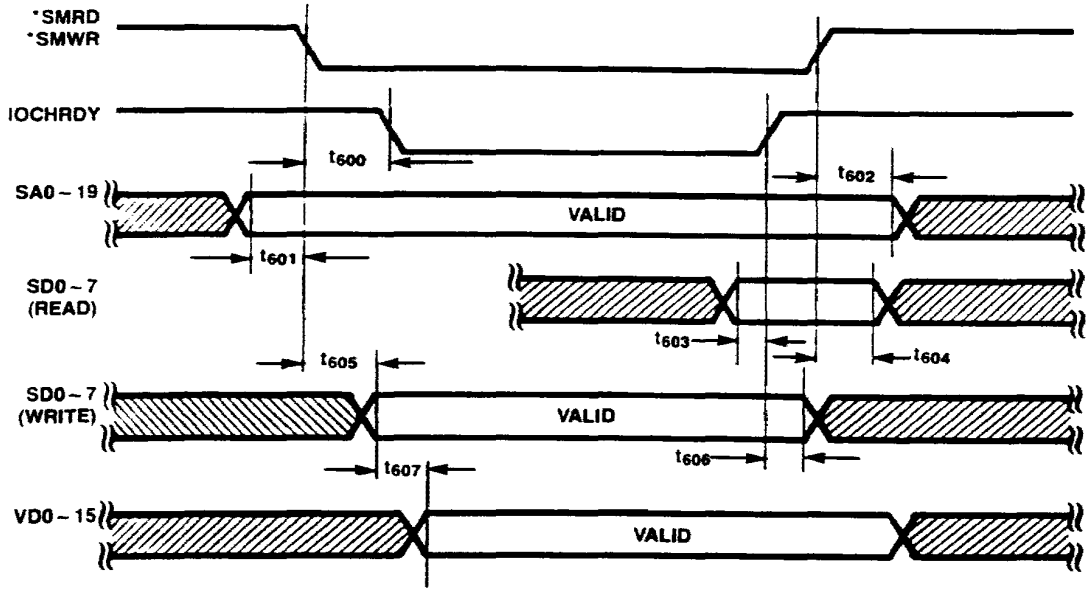
No.	Parameter	Symbol	T_{CY}=60ns		T_{CY}=70ns		Unit
			Min	Max	Min	Max	
t_{614}	Clock low time	T_{CL}	30	30	28	42	ns
t_{615}	RAS precharge time	T_{RP}	90	—	95	—	ns
t_{616}	RAS pulse width	T_{RAS}	105	—	125	—	ns
t_{617}	RAS hold time	T_{RSH}	55	—	65	—	ns
t_{618}	CAS to RAS precharge time	T_{CRP}	15	—	15	—	ns
t_{619}	Row address set up time	T_{ASR}	10	—	10	—	ns
t_{620}	Row address hold time	T_{RAH}	25	—	25	—	ns
t_{621}	Column address set up time	T_{ASC}	15	—	15	—	ns
t_{622}	Column address hold time	T_{CAH}	25	—	25	—	ns
t_{623}	Column address hold time to RAS	T_{AR}	80	—	90	—	ns
t_{624}	Write command set up time	T_{WCS}	10	—	10	—	ns
t_{625}	Read command set up time	T_{RCS}	10	—	10	—	ns
t_{626}	Data hold time	T_{DH}	10	—	10	—	ns
t_{627}	Data set up time	T_{DS}	10	—	10	—	ns
t_{628}	SRAM access time required	T_{ACS}	—	115	—	135	ns
t_{629}	SRAM data hold time	T_{ACH}	0	—	0	—	ns

LCD Interface Timing

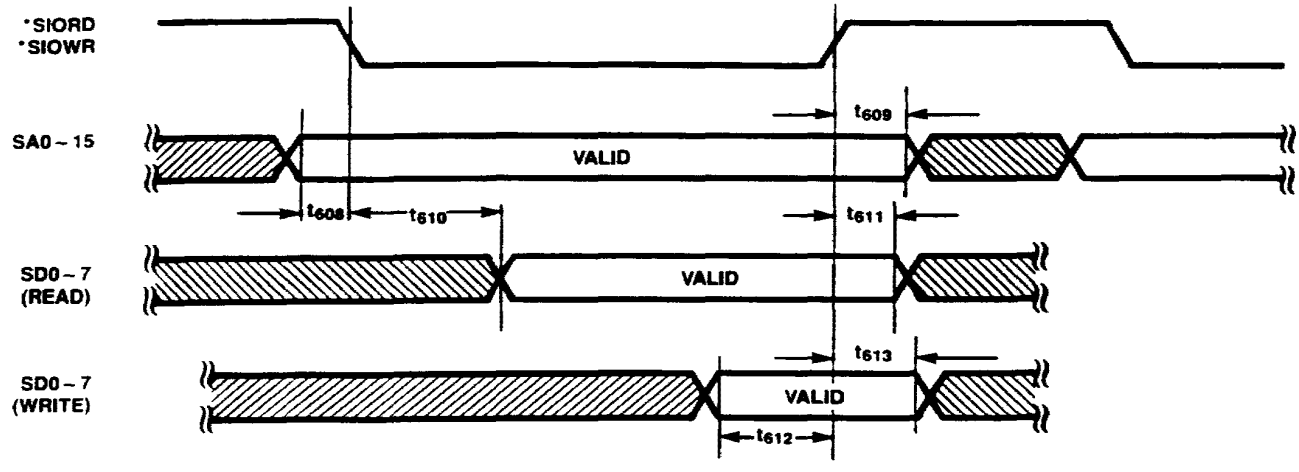
No.	Parameters	Symbol	Min	Max	Unit	Comment
t_{630}	Pixel data to SHCLK set up time	T_{LDS}	150		ns	
t_{631}	Pixel data to SHCLK hold time	T_{LDH}	2 T_{CY}		ns	
t_{632}	SHCLK pulse width	T_{SCY4}	3.5 T_{CY}–8		ns	400 line LCD
t_{633}	SHCLK pulse width	T_{SCY2}	3 T_{CY}–20		ns	200 line LCD
t_{634}	LOCLK to SHCLK delay time	T_{LSD}	2.5 T_{CY}		ns	
t_{635}	SHCLK to LOCLK delay time	T_{SLD}	2 T_{CY}–10		ns	400 line LCD only
t_{636}	SHCLK to E edge time	T_{SCE}	10		ns	
t_{637}	LOCLK high to E low delay time	T_{LCE2}	2 T_{CY}		ns	Generic LCD type LOCLK
t_{638}	E low to LOCLK low delay time	T_{LCE1}	4.5 T_{CY}–10		ns	200 line dual screen only
t_{639}	SHARP LCD type LOCLK pulse width	T_{PLCY}	2.5 T_{CY}–10		ns	
t_{640}	SHARP LCD type LOCLK to SHCLK low	T_{PLCS}	10		ns	
t_{641}	SHARP LCD type LOCLK to SHCLK high	T_{PLCE}	10		ns	
t_{642}	LOCLK low to FRAME low	T_{FRLC}	4 T_{CY}–20		ns	

VG-600 TIMING WAVEFORMS

CPU Interface Timing

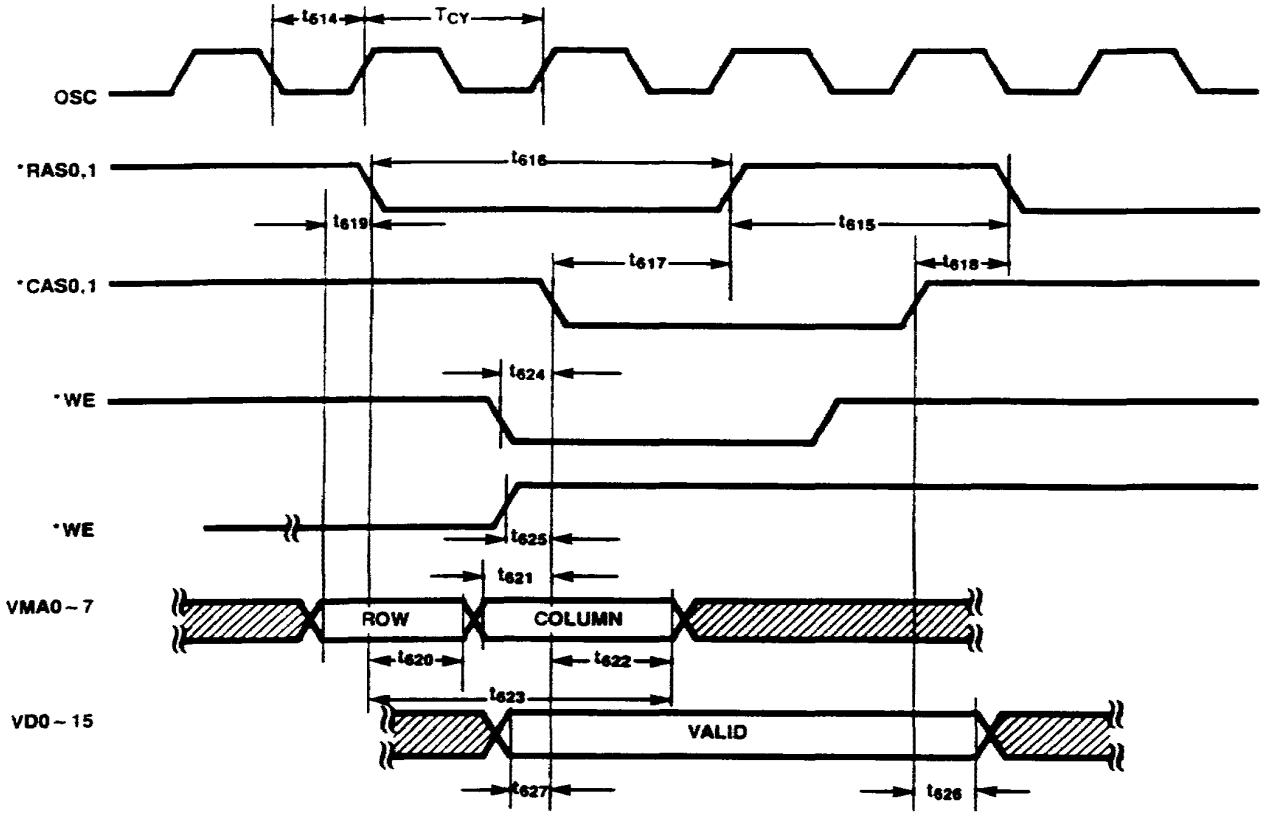


I/O Access Timing

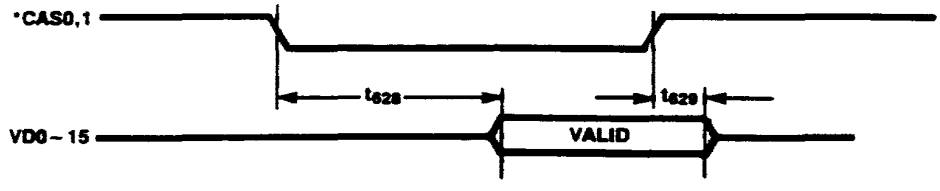


VG-600 TIMING WAVEFORMS (continued)

DRAM Interface Timing

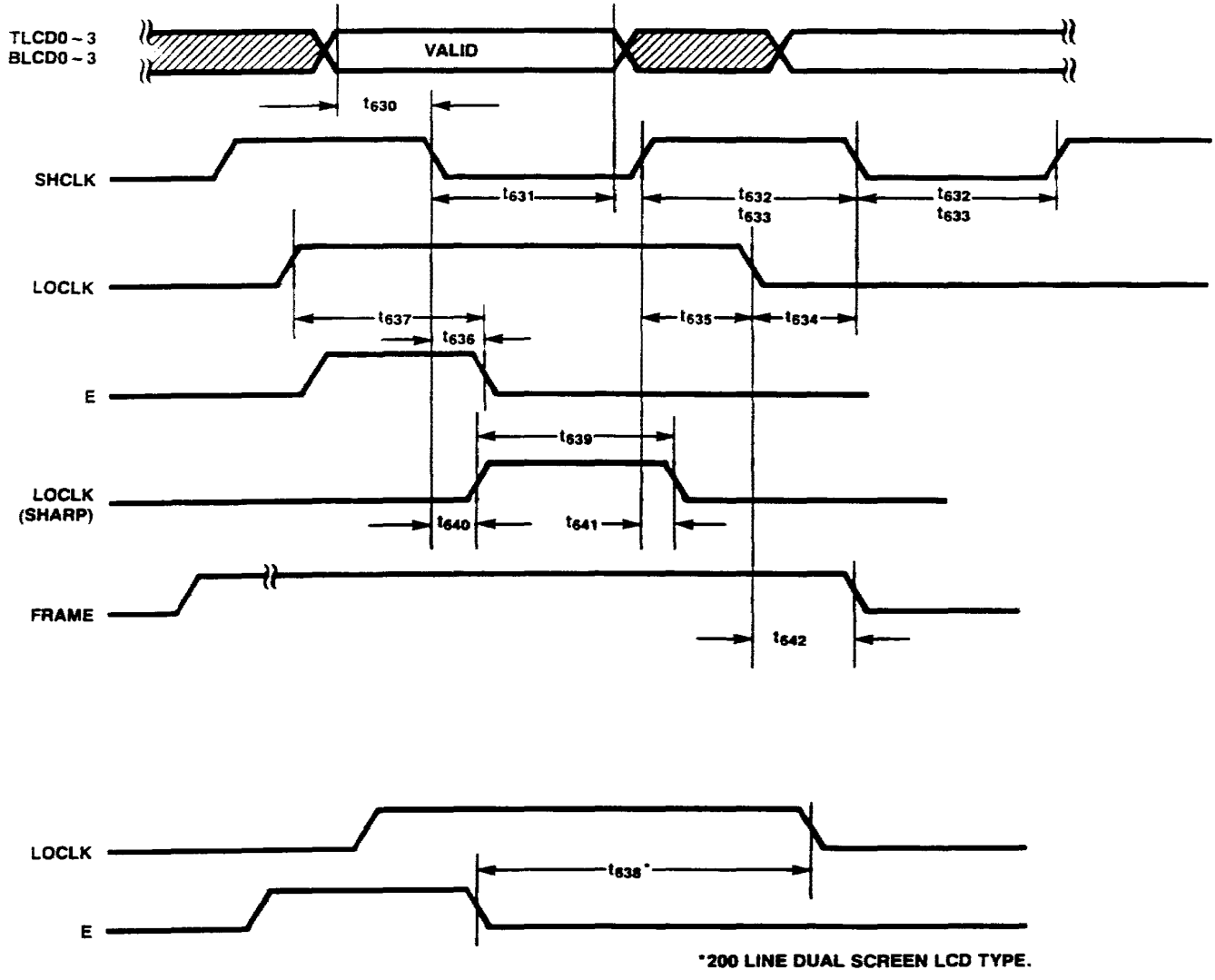


SRAM Timing



VG-600 TIMING WAVEFORMS (continued)

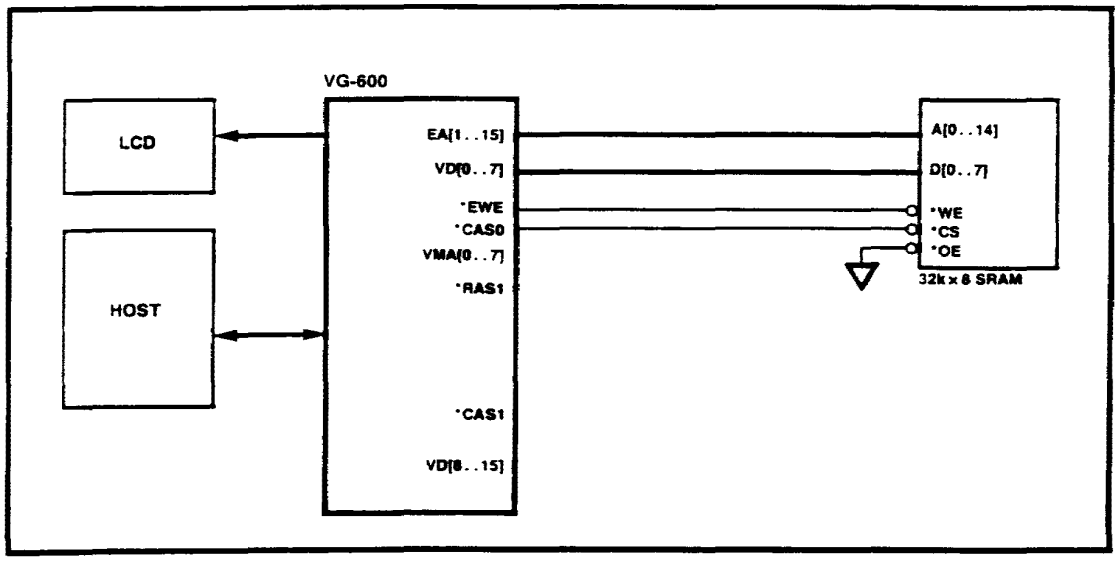
LCD Interface Timing



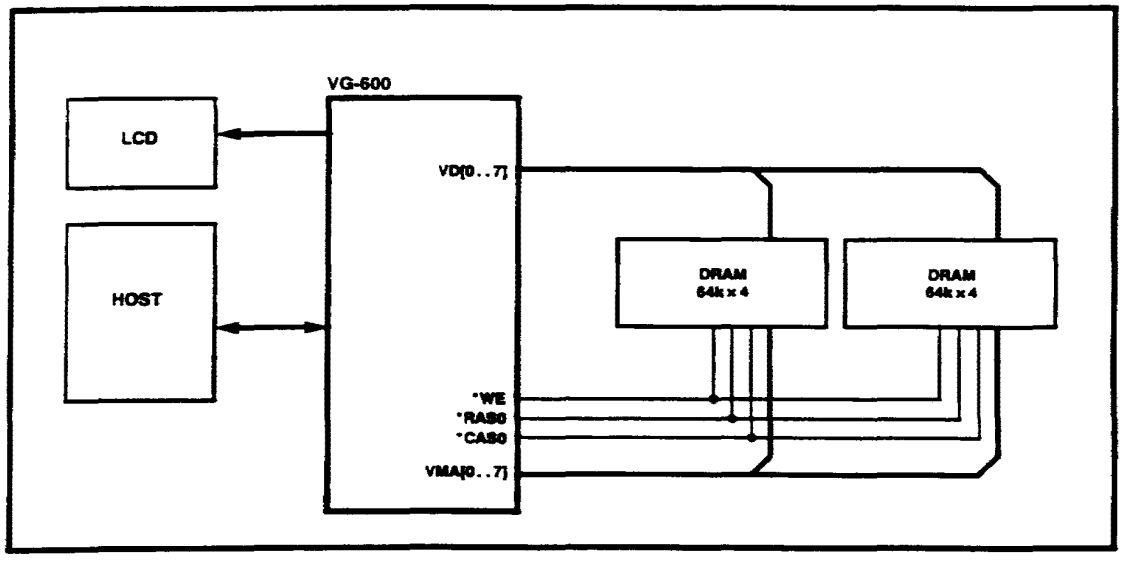
*200 LINE DUAL SCREEN LCD TYPE.

VG-600 CONFIGURATIONS

200 Line with Static RAM

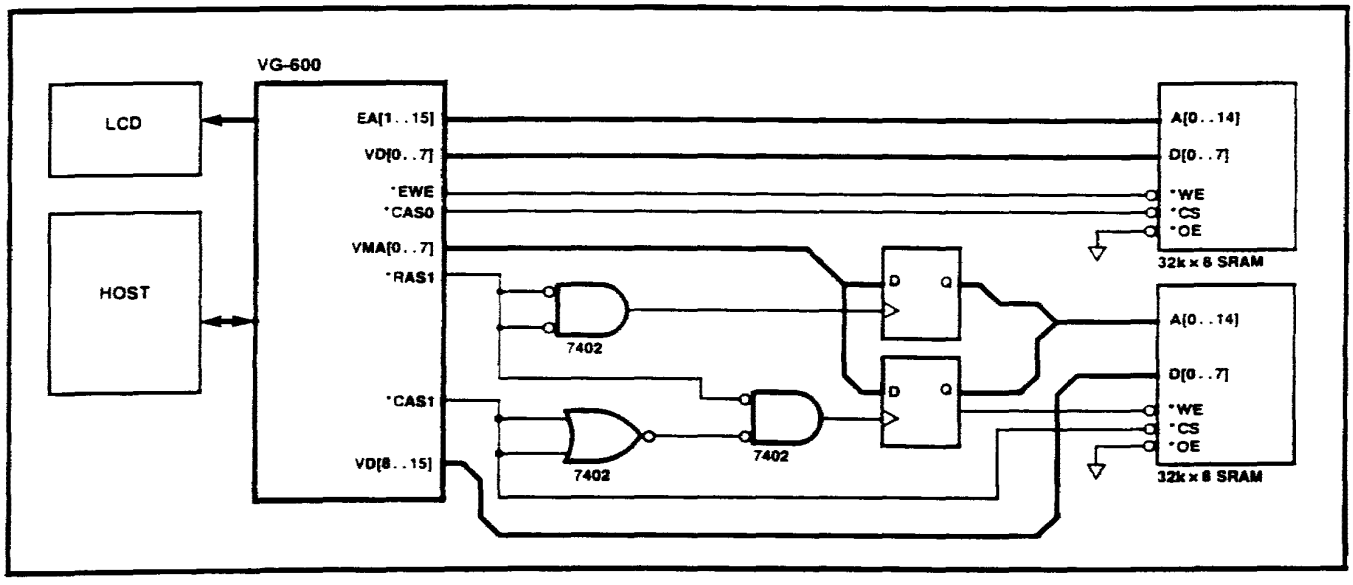


200 Line with Dynamic RAM

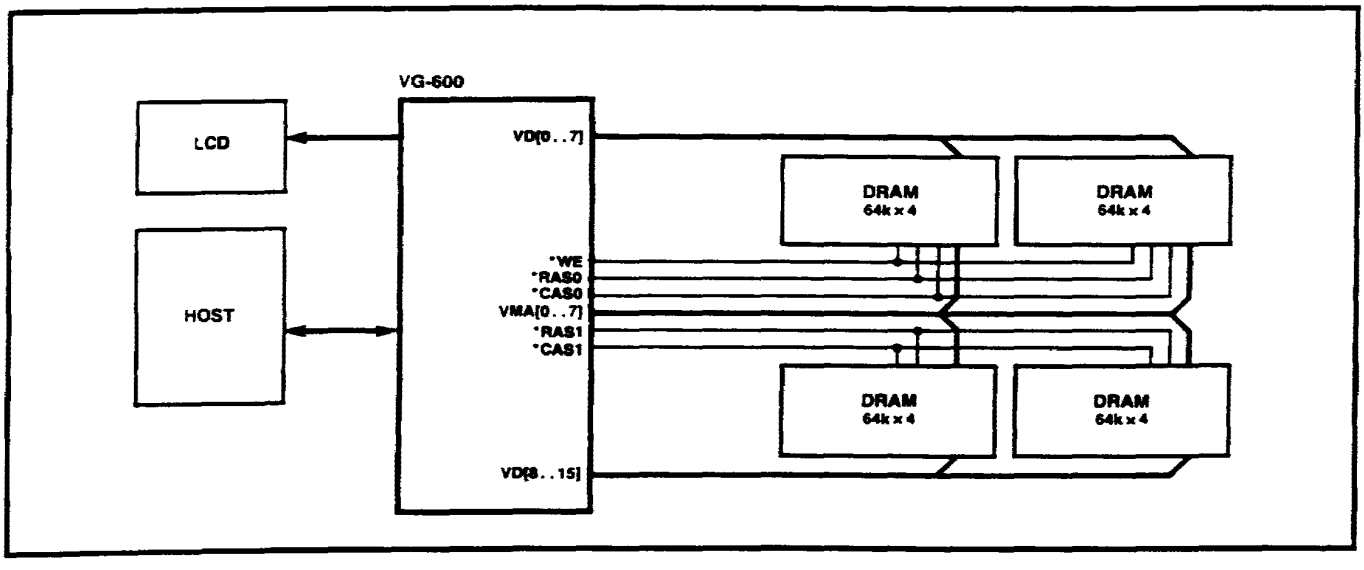


VG-600 CONFIGURATIONS (continued)

400 Line with Static RAM



400 Line with Dynamic RAM



VG-600
LCD CONTROLLER FOR PC ARCHITECTURE SYSTEMS

SUPPORTED LCD DISPLAYS

640 x 200 — Single Screen

Toshiba TLX-561
Hitachi LM250X
Toshiba TLX-932
Seiko F645D
Sanyo LCM-5205-01A

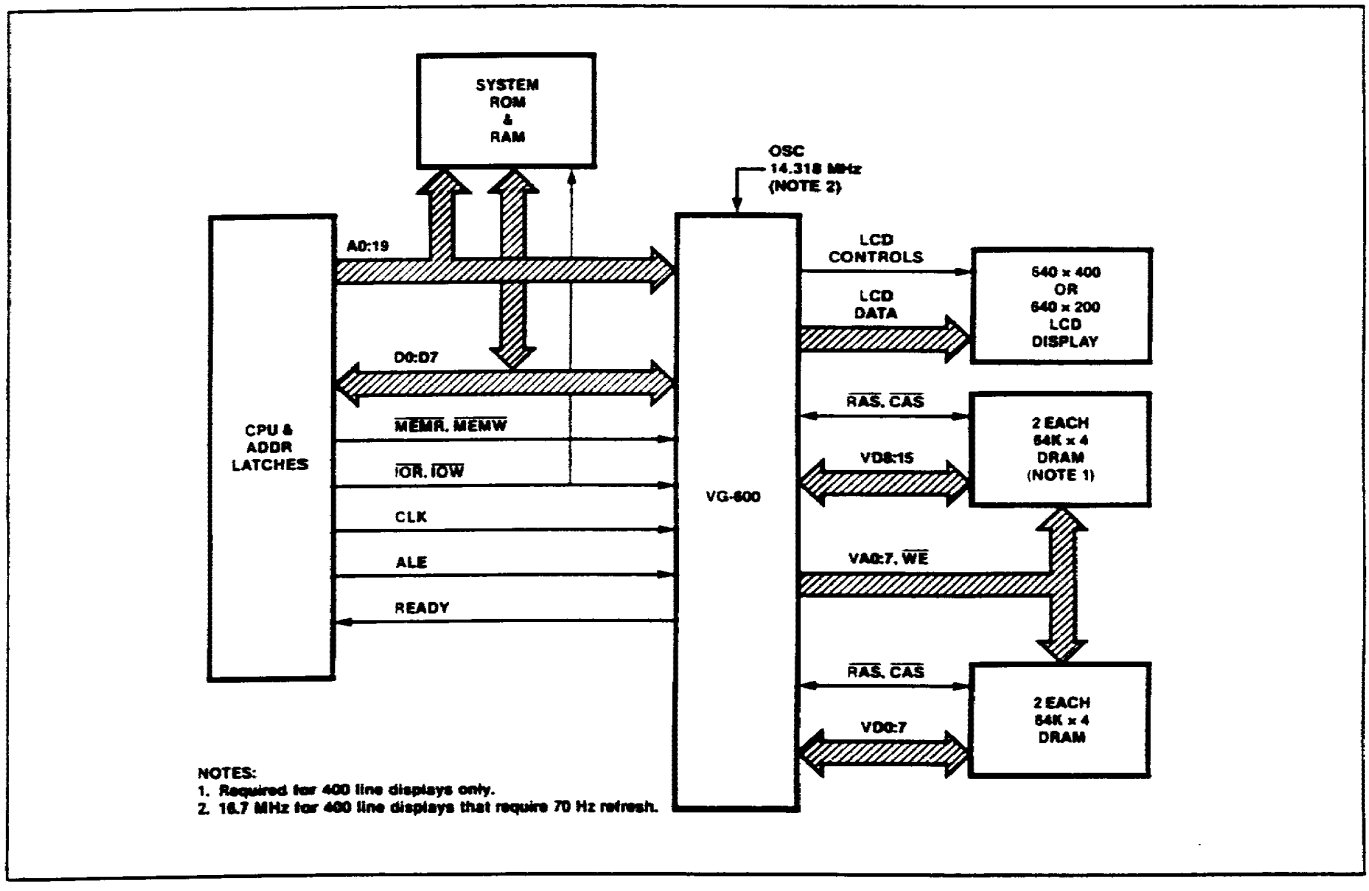
640 x 200 — Split Screen

Sharp LM64004G
Hitachi LM236XB
Hitachi LM585X
Sanyo LCM-591-15A
Sanyo LCM-5203-01A

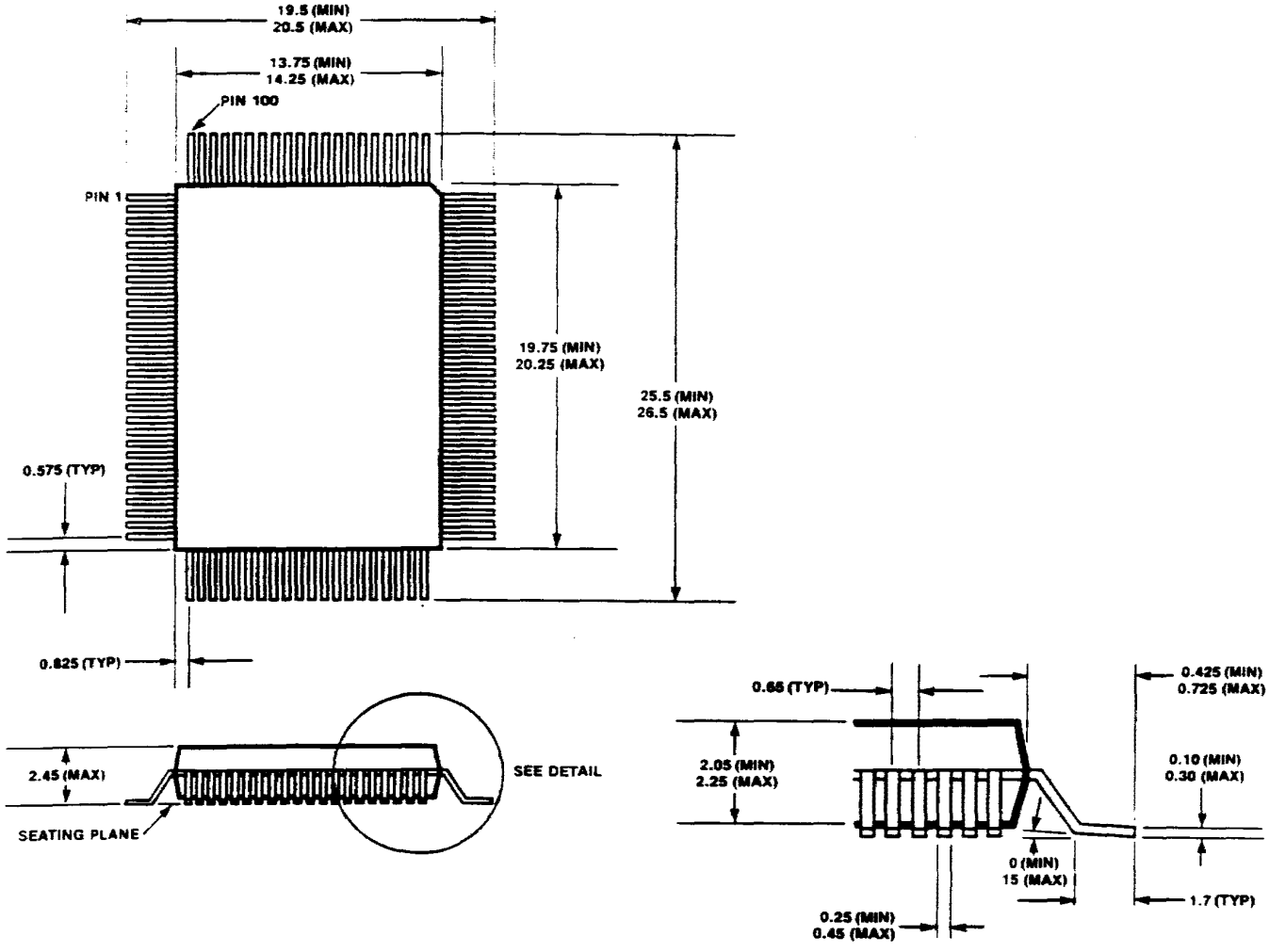
640 x 400 — Split Screen

Sharp LM640351
Sharp LM64015T
Sharp 64035W
Matsushita EDM-LG64AA02D
Toshiba TLX-1181
Hitachi LM-252X
Sanyo LCM-5218-01BA/02BA
Sanyo LCM5201-01A
Matsushita EDM-1G64AA01
Seiko F642F

SAMPLE APPLICATION



PHYSICAL DIMENSIONS (mm)



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