AMCC

PowerPC 405GP/GPr

Embedded Processor

PowerPC™

With speeds of up to 266 MHz (405GP) or 400 MHz (405GPr), the PowerPC 405GP/GPr family of embedded processors provides an optimized balance of performance, low power, and features. These processors are ideally suited for general purpose Internet, communication, data storage, consumer, imaging and pervasive computing applications. They combine a rich feature mix with a variety of small form factors to accommodate a wide range of space-constrained implementations.

Benefits

- Delivers 133 MHz to266 MHz (405GP) or 266 MHz to 400 MHz (405GPr) performance (CPU)
- On-chip SRAM for faster processing in data-intensive applications
- A wide array of small-footprint-package options for high-density applications
- CodePack Decompression stores instructions in memory in compressed format and improves code density by up to 40%
- On-chip SDRAM controller supports up to 1 Gbyte of memory
- On-chip PCI bus interface
- On-chip peripherals including Ethernet MAC and serial ports
- Low power dissipation for high-density and power-conscious applications

The PowerPC 405 Core

The PowerPC 405 core has been optimized for system on a chip designs requiring solid performance, low cost and low power consumption. Performance is enhanced through the use of separate instruction and data cache units. A 5-stage pipeline further boosts performance by offering single cycle execution of most instructions, including loads and stores.

Dual Bus Architecture

The PowerPC 440GP/GPr processors are designed with two on-chip buses: a processor local bus (PLB) and an on-chip peripheral bus (OPB). High-speed peripherals, like the PCI bus or memory controller connect directly to the core through the high-bandwidth, 64-bit PLB. Less demanding devices are served by the 32-bit OPB.

An external bus controller allows external masters to access the on-chip SDRAM and PCI controllers.

Memory Support

A 4-Kbyte on-chip SRAM stores critical code and data, and provides single-cycle access for faster processing in data-intensive router and switch applications as well as other demanding implementations. An on-chip SDRAM controller provides access to up to four banks of external memory for a maximum of 1 Gbyte. Performance is enhanced with separate read and write buffers, while ECC capabilities promote data integrity.

PCI Support

The PowerPC 405GP/GPr processors provide a 32-bit PCI interface that is PCI V2.2 compatible. An internal PCI arbiter on the 405GPr supports six PCI masters.

Ethernet Interface

An on-chip 10/100 Ethernet port provides built-in networking capabilities, making the PowerPC 405GP/GPr processors a low-cost alternative for a variety of communications applications.

Standard Peripherals

The PowerPC 405GP and 405GPr processors offer an array of on-chip standard peripherals. Two serial ports are provided as well as a master and slave IIC controller. Up to 24 general-purpose I/Os further enhance functionality.

PowerPC Partners Ecosystem

AMCC's embedded PowerPC processors are supported by an extensive ecosystem of products and services from a wide range of leading suppliers. AMCC's PowerPC Partners program includes industry-standard providers of:

- Embedded operating systems
- Hardware and software development tools
- Embedded software products and services
- Board-level products
- System design services
- Technical training

For full details of the products and services available through the PowerPC Partners program, or to browse support available for a specific processor, visit:

http://www.amcc.com/Embedded/Partners

AMCC also provides an evaluation kit for this PowerPC processor, including an optimized evaluation board as well as sample applications and other software.

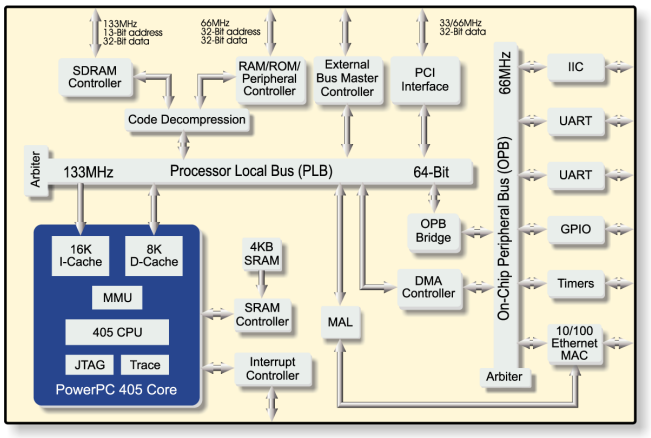
Features

- Speed (frequency):
  133 MHz to 266 MHz (405GP)
  266 MHz to 400 MHz (405GPr)
- Performance: 1.52 DMIPS/MHz
  (404 DMIPS @ 266MHz - 405GP)
  (608 DMIPS @ 400 MHz - 405GPr)
- 16-Kbyte instruction cache/8-Kbyte data cache (405GP) or 16-Kbyte instruction cache/16-Kbyte data cache (405GPr)
- On-chip SDRAM controller with separate 32-byte read and 128-byte write buffers
- Supports up to 1 Gbyte of memory
- External bus master controller allows external masters to access SDRAM and PCI
- DMA controller with four independent channels supports transfers between SDRAM, PCI, internal UARTs and devices on the external peripheral bus
- 32-bit PCI V2.2 compatible PCI interface with synchronous and asynchronous operation
- Internal PCI arbiter supports six PCI masters and external arbitration
- On-chip Ethernet support (10/100 MAC)
- CodePack Decompression stores instructions in memory in compressed format; improves code density by up to 40%

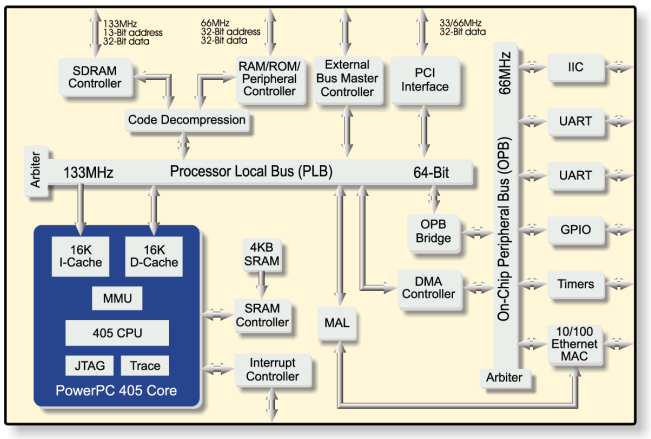
PowerPC 405GP/GPr

- Two serial ports
- Master and slave IIC controller
- Up to 24 general-purpose I/Os
- Interrupt controller including up to 13 external interrupts
- JTAG support in processor core
- RoHS compliant parts available (lead-free) for 27mm and 35mm packages

For more information, please visit ***http://www.amcc.com.***



PPC 405GP



PPC 405GPr

Specifications

Technology	405GP	405GPr
	• 0.25 µm (0.18 µm L_{eff})	• 0.18 µm (0.1 µm L_{eff})
Performance (estimated)	**405GP**	**405GPr**
	• 202 @ 133 MHz	• 404 @ 266 MHz
	• 304 @ 200 MHz	• 506 @ 333 MHz
	• 404 @ 266 MHz	• 607 @ 400 MHz
Frequency	**405GP**	**405GPr**
	• 133/133/66/66 MHz	• 266/133/66/66 MHz
(CPU/SDRAM/PCI/EBC)	• 200/100/66/50 MHz	• 333/133/66/66 MHz
	• 266/133/66/66 MHz	• 400/133/66/66 MHz
Typical Power Dissipation	**405GP**	**405GPr**
	• 1.5 W @ 200 MHz	• 0.72 W @ 266 MHz
		• 0.76 W @ 333 MHz
		• 0.82 W @ 400 MHz
Case Temperature Range	**405GP**	**405GPr**
	• -40° to +85° C	• -40° to +85° C; extended temperature range (-40 to +105° C) at 266 MHz available by derating 333 MHz
Power Supply	**405GP**	**405GPr**
	• 2.5 V (logic), 3.3 V (I/O) Supports 5-V I/Os	• 1.8 V (logic), 3.3 V (I/O) Supports 5-V I/Os
Signal I/Os	**405GP**	**405GPr**
	• 300	• 299
Packaging	**405GP**	**405GPr**
	• 456-ball, (35 mm x 35 mm)	• 456-ball, (35 mm x 35 mm)
	• 456-ball, (27 mm x 27 mm)	• 456-ball, (27 mm x 27 mm)
	• 413-ball, (25 mm x 25 mm)	

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