M1531B : CPU-to-PCI bridge, Memory, Cache and Buffer Controller

1.1 Features

- Supports all Intel/Cyrix/AMD/TI/IBM 586 socket processors. Host bus at 83.3MHz, 75MHz, 66 MHz, 60 MHz and 50MHz at 3.3V/2.5V.
  - Supports linear wrap mode for Cyrix M1 & M2
  - Supports Write Allocation feature for K6
  - Supports Pseudo Synchronous PCI bus access (CPU bus 75MHz - PCI bus 30MHz, CPU bus 83.3MHz - PCI bus 33MHz)

- Supports Pipelined-Burst SRAM
  - Direct mapped, 256KB/512KB/1MB
  - Write-Back/Dynamic-Write-Back cache policy
  - Built-in 8K*2 bit SRAM for MESI protocol to reduce cost and enhance performance
  - Cacheable memory up to 64MB with 8-bit Tag SRAM
  - Cacheable memory up to 512MB with 11-bit Tag SRAM
  - 3-1-1-1-1-1-1-1 for Pipelined Burst SRAM at back-to-back burst read and write cycles.
  - Supports 3.3V/5V SRAMs for Tag Address.
  - Supports CPU Single Read Cycle L2 Allocation.

- Supports FPM/EDO/SDRAM DRAMs
  - 8 RAS Lines up to 1GByte support
  - 64-bit data path to Memory
  - Symmetrical/Asymmetrical DRAMs
  - 3.3V or 5V DRAMs
  - Duplicated MA[1:0] driving pins for burst access
  - No buffer needed for RASJ and CASJ and MA[1:0]
  - CBR and RAS-only refresh for FPM
  - CBR and RAS-only refresh and Extended refresh and self refresh for EDO
  - CBR and Self refresh for SDRAM
  - 16 QWORD deep merging buffer for 3-1-1-1-1-1-1-1 posted write cycle to enhance high speed CPU burst access
  - 6-3-3-3-3-3-3-3 for back-to-back FPM read page hit
    5-2-2-2-2-2-2-2 for back-to-back EDO read page hit
    6-1-1-1-2-1-1-1 for back-to-back SDRAM read page hit
    2-2-2-2 for retired data for posted write on FPM and EDO page-hit
    x-1-1-1 for retired data for posted write SDRAM page-hit
  - Enhanced DRAM page miss performance
  - Supports 64M-bit (16M*4, 8M*8, 4M*16) technology of DRAMs
  - Supports Programmable-strength RAS/CAS/MWEJ/MA buffers.
  - Supports Error Checking & Correction (ECC) and Parity for DRAM
  - Supports the most flexible six 32-bit populated banks of DRAM to support the most friendly DRAM upgrade ability
  - Supports SIMM and DIMM
- Synchronous/Pseudo Synchronous 25/30/33MHz 3.3V/5V tolerance PCI interface
- Concurrent PCI architecture
  - PCI bus arbiter: five PCI masters and M1533/M1543 (ISA Bridge) supported
  - 6 DWORDs for CPU-to-PCI Memory write posted buffers
  - Converts back-to-back CPU to PCI memory write to PCI burst cycle
  - 38/22 DWORDs for PCI-to-DRAM Write-posted/Read-prefetching buffers
  - PCI-to-DRAM up to 133 MB/sec bandwidth (even when L1/L2 writeback)
  - L1/L2 pipelined snoop ahead for PCI-to-DRAM cycle
  - Supports PCI mechanism #1 only
  - PCI spec. 2.1 support. (N(32/16/8)+8 rule, passive release, fair arbitration)
  - Enhanced performance for Memory-Read-Line and Memory-Read-Multiple and Memory-write-Invalidate PCI commands.

- Enhanced Power Management
  - ACPI support
  - Supports PCI bus CLKRUN function
  - Supports Dynamic Clock Stop
  - Supports Power On Suspend
  - Supports Suspend to Disk
  - Supports Suspend to DRAM
  - Self Refresh during Suspend
- 328-pin (27mmx27mm) BGA package

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1.2 Introduction

Aladdin-IV is the succeeding generation chipset of Aladdin-III from Acer Labs. It maintains the best system architecture (2-chip solution) to achieve the best system performance with the lowest system cost (TTL-free). Aladdin-IV consists of two BGA chips to give the 586-class system a complete solution with most up-to-date features and architecture for the most engaging multimedia/ multithreading OS and software applications. It utilizes the modern BGA package to improve the AC characterization, resolves system bottleneck and makes the system manufacturing easier.

M1531B is the successor of M1531. The major differences are the 64-Mbit SDRAM support and more cacheable region support in SDRAM configuration. Please refer to the application note in Appendix A.

M1531B includes the higher CPU bus frequency (up to 83.3MHz) interface for the incoming Cyrix M2 and AMD K6, PBSRAM and L2 controller, internal MESI tag bits (8K*2) to reduce cost and enhance performance, high performance FPM/EDO/SDRAM DRAM controller, PCI 2.1 compliant bus interface, smart deep buffer design for CPU-to-DRAM, CPU-to-PCI, and PCI-to-DRAM to achieve the best system performance, and also the highly efficient PCI fair arbiter. M1531B also provides the most flexible 32/64-bit memory bus interface for the best DRAM upgrade ability and ECC/Parity design to enhance the system reliability. With the concurrent bus design, PCI-to-PCI access can run concurrently with CPU-to-L2 and CPU-to-DRAM access, PCI-to-DRAM access can run concurrently with CPU-to-L2 access. M1531B also supports the snoop ahead feature to achieve the PCI master full bandwidth access (133Mbytes). M1531B also provides the enhanced power management features including ACPI support, suspend DRAM refresh, and internal chip power control to support the Microsoft's On Now technology OS.

M1533 provides the best power management system solution. M1533 integrates ACPI support, deep green function, 2-channel dedicated Ultra-33 IDE master controller, 2-port USB controller, SMBus controller, and PS2 Keyboard/Mouse controller.

M1543 provides the best desktop system solution. M1543 integrates ACPI support, green function, 2-channel dedicated Ultra-33 IDE Master controller, 2-port USB controller, SMBus controller, PS/2 Keyboard/Mouse controller and the Super I/O (Floppy Disk Controller, 2 serial port/1 parallel port) support.

In the following diagram, ALADDIN-IV gives a highly integrated system solution and a most up-to-date architecture, which provides the best cost/performance system solution for Desktop and also for Notebook vendors.

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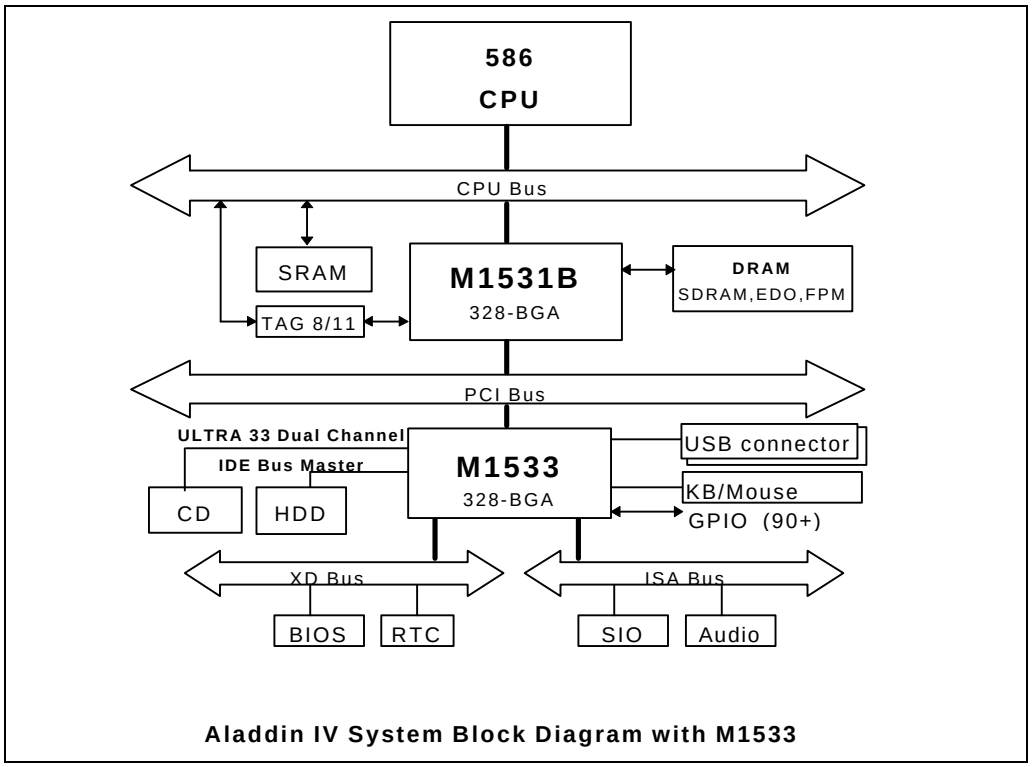
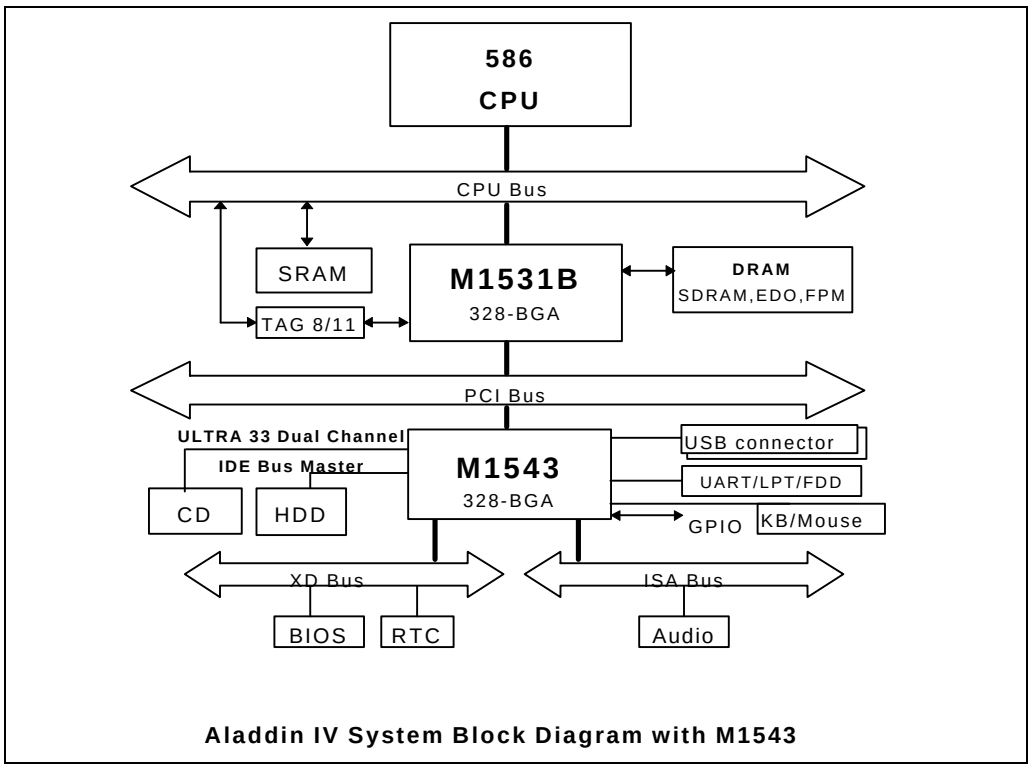


Aladdin IV System Block Diagram with M1533



Aladdin IV System Block Diagram with M1543

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Section 2 : Pin Description

2.1 Pinout Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	NC	PHLDAJ	AD3	AD6	AD8	AD12	PAR	TRDYJ	AD17	AD22	AD25	AD30	REQJ3	GNTJ2	GNTJ3	MPD2	MPD0	MD61	MD29	MD62
B	BEJ0	PHLDJ	AD2	AD5	AD7	AD11	CBEJ1	DEVSELJ	AD16	AD21	AD24	AD29	REQJ2	GNTJ1	MPD5	MPD1	MD63	MD27	MD60	MD28
C	BEJ3	BEJ2	BEJ1	AD4	CBEJ0	AD10	AD15	STOPJ	CBEJ2	AD20	CBEJ3	AD28	REQJ1	GNT0J	MPD4	MD30	MD25	MD58	MD26	MD59
D	BEJ6	BEJ5	BEJ4	AD0	AD1	AD9	AD14	LOCKJ	FRAMEJ	AD19	AD23	AD27	REQJ0	MPD7	MPD3	MD55	MD23	MD56	MD24	MD57
E	DCJ	HITMJ	EADSJ	BEJ7	RSTJ	PCIMRQJ	AD13	SERRJ	IRDYJ	AD18	PCLKIN	AD26	AD31	MPD6	MD31	MD20	MD53	MD21	MD54	MD22
F	BRDYJ	BOFFJ	SMIACTJ	HLOCKJ	ADSJ	VCC_B								VCC_C	VCC_C	MD50	MD18	MD51	MD19	MD52
G	HD63	CACHEJ	AHOLD	KENJ	NAJ	VCC_A			**M1531B**						VCC_C	MD15	MD48	MD16	MD49	MD17
H	HD60	HD61	HD62	WRJ	MIOJ											MD45	MD13	MD46	MD14	MD47
J	HD55	HD56	HD57	HD58	HD59				GND	GND	GND	GND				MD10	MD43	MD11	MD44	MD12
K	HD51	HD52	HD53	HD54	HCLKIN				GND	GND	GND	GND				MD40	MD8	MD41	MD9	MD42
L	HD46	HD47	HD48	HD49	HD50				GND	GND	GND	GND				MD5	MD38	MD6	MD39	MD7
M	HD41	HD42	HD43	HD44	HD45				GND	GND	GND	GND				MD35	MD3	MD36	MD4	MD37
N	HD36	HD37	HD38	HD39	HD40										VDD5S	REQJ4	GNTJ4	MD1	MD34	MD2
P	HD31	HD32	HD33	HD34	HD35	VCC_A									VCC_C	32K	SUSPEND	MD32	MD0	MD33
R	HD26	HD27	HD28	HD29	HD30	VDD5	VCC_A							VCC_B	VCC_C	RASJ6	RASJ7	CASJ2	CASJ7	CASJ3
T	HD21	HD22	HD23	HD24	HD25	HD0	A12	A5	GWEJ	COEJ	CADVJ	TWEJ	MAA0	MAA1	SCASJ1	SRASJ1	MWEJ1	RASJ1	RASJ0	CASJ6
U	HD16	HD17	HD18	HD19	HD20	HD1	A13	A8	CCSJ	BWEJ	CADSJ	TIO0	TIO1	MAB0	MAB1	MA5	MWEJ	RASJ4	RASJ3	RASJ2
V	HD15	HD14	HD13	HD6	HD3	A17	A14	A10	A4	A29	A25	A24	A23	TIO2	MA2	MA4	MA8	CASJ5	CASJ1	RASJ5
W	HD12	HD11	HD10	HD5	HD2	A18	A15	A11	A7	A30	A31	A22	A21	TIO4	TIO6	MA3	MA7	MA10	CASJ0	CASJ4
Y	HD9	HD8	HD7	HD4	A20	A19	A16	A9	A6	A3	A28	A26	A27	TIO3	TIO5	TIO7	MA6	MA9	MA11	TIO8

TOP VIEW

Figure 2-1. M1531B Pin Diagram

	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Y	TIO 8	MA 11	MA9	MA6	TIO 7	TIO 5	TIO 3	A27	A26	A28	A3	A6	A9	A16	A19	A20	HD4	HD7	HD8	HD9
W	CAS J4	CAS J0	MA 10	MA7	MA3	TIO 6	TIO 4	A21	A22	A31	A30	A7	A11	A15	A18	HD2	HD5	HD10	HD 11	HD 12
V	RAS J5	CAS J1	CASJ 5	MA8	MA4	MA2	TIO 2	A23	A24	A25	A29	A4	A10	A14	A17	HD3	HD6	HD 13	HD 14	HD 15
U	RAS J2	RAS J3	RAS J4	MW EJ	MA5	MAB 1	MAB0	TIO 1	TIO0	CADSJ	BWEJ	CCS J	A8	A13	HD1	HD20	HD 19	HD 18	HD 17	HD 16
T	CAS J6	RAS J0	RAS J1	MW EJ1	SRA SJ1	SCA SJ1	MAA 1	MAA 0	TWE J	CADV J	COEJ	GWE J	A5	A12	HD0	HD25	HD 24	HD 23	HD 22	HD 21
R	CAS J3	CAS J7	CAS J2	RAS J7	RASJ 6	VCC _C	VCC_ B							VCC _A	VDD 5	HD 30	HD 29	HD 28	HD 27	HD 26
P	MD3 3	MD0	MD 32	SUSPE ND	32K	VCC _C			**M1531B**						VCC _A	HD 35	HD 34	HD 33	HD 32	HD 31
N	MD2	MD3 4	MD1	GNT J4	REQJ 4	VDD 5S										HD 40	HD 39	HD 38	HD 37	HD 36
M	MD3 7	MD4	MD 36	MD3	MD 35				GND	GND	GND	GND				HD 45	HD 44	HD 43	HD 42	HD 41
L	MD7	MD 39	MD 6	MD 38	MD5				GND	GND	GND	GND				HD 50	HD 49	HD 48	HD 47	HD 46
K	MD 42	MD9	MD 41	MD8	MD 40				GND	GND	GND	GND				HCL KIN	HD 54	HD 53	HD 52	HD 51
J	MD 12	MD 44	MD 11	MD 43	MD 10				GND	GND	GND	GND				HD 59	HD 58	HD 57	HD 56	HD 55
H	MD 47	MD 14	MD 46	MD 13	MD 45											MIO J	WR J	HD6 2	HD6 1	HD 60
G	MD 17	MD 49	MD 16	MD 48	MD 15	VCC _C									VCC _A	NAJ	KE NJ	AHOL D	CACH EJ	HD 63
F	MD 52	MD1 9	MD5 1	MD1 8	MD 50	VCC _C	VCC_ C								VCC _B	ADS J	HLOCK J	SMIA CTJ	BOF FJ	BRD YJ
E	MD 22	MD 54	MD 21	MD 53	MD 20	MD 31	MPD 6	AD 31	AD 26	PCLKI N	AD 18	IRDYJ	SER RJ	AD1 3	PCIM RQJ	RST J	BEJ 7	EAD SJ	HIT MJ	DCJ
D	MD 57	MD 24	MD 56	MD 23	MD 55	MPD 3	MPD 7	REQ J0	AD 27	AD 23	AD 19	FRAM EJ	LOC KJ	AD1 4	AD9	AD1	AD0	BEJ 4	BEJ 5	BEJ 6
C	MD 59	MD 26	MD 58	MD 25	MD 30	MPD 4	GNT 0J	REQ J1	AD 28	CBEJ 3	AD 20	CBEJ 2	STO PJ	AD1 5	AD 10	CBE J0	AD4	BEJ 1	BEJ 2	BEJ 3
B	MD 28	MD 60	MD2 7	MD 63	MPD 1	MPD 5	GNT J1	REQ J2	AD 29	AD 24	AD 21	AD 16	DEV SEL J	CBE J1	AD 11	AD7	AD5	AD2	PHL DJ	BEJ 0
A	MD 62	MD 29	MD6 1	MPD 0	MPD 2	GNT J3	GNT J2	REQ J3	AD 30	AD 25	AD 22	AD 17	TRD YJ	PAR	AD 12	AD8	AD6	AD3	PHL DAJ	NC

Figure 2-2. M1531B Pin Diagram (bottom view)

2.2 Pin Description Table :

Pin Name	Type	Description
Host Interface : 3.3V/2.5V		
A[31:3]	I/O Group A	**Host Address Bus Lines**. A[31:3] have two functions. As inputs, along with the byte enable signals, these pins serve as the address lines of the host address bus which define the physical area of memory or I/O being accessed. As outputs, the M1531B drives them during inquiry cycles on behalf of PCI masters.
BEJ[7:0]	I Group A	**Byte Enables**. These are the byte enable signals for the data bus. BEJ[7] applies to the most significant byte and BEJ[0] applies to the least significant byte. They determine which byte of data must be written to the memory, or are requested by the CPU. In local memory read and line-fill cycles, these inputs are ignored by the M1531B.
ADSJ	I Group A	**Address Strobe**. The CPU will start a new cycle by asserting ADSJ first. The M1531B will not precede to execute a cycle until it detects ADSJ active.
BRDYJ	O Group A	**Burst Ready**. The assertion of BRDYJ means the current transaction is complete. The CPU will terminate the cycle by receiving 1 or 4 active BRDYJs depending on different types of cycles.
NAJ	O Group A	**Next Address**. It is asserted by the M1531B to inform the CPU that pipelined cycles are ready for execution.
AHOLD	O Group A	**CPU AHold Request Output**. It connects to the input of CPU's AHOLD pin and is actively driven for inquiry cycles.
EADSJ	O Group A	**External Address Strobe**. This signal is connected to the CPU EADSJ pin. During PCI cycles, the M1531B will assert this signal to proceed snooping.
BOFFJ	O Group A	**CPU Back-Off**. If BOFFJ is sampled active, CPU will float all its buses in the next clock. M1531B will assert this signal to request CPU floating all its output buses.
HITMJ	I Group A	**Primary Cache Hit and Modified**. When snooped, the CPU asserts HITMJ to indicate that a hit to a modified line in the data cache occurred. It is used to prohibit another bus master from accessing the data of this modified line in the memory until the line is completely written back.
MIOJ	I Group A	**Host Memory or I/O**. This bus definition pin indicates the current bus cycle is either memory or input/ output.
DCJ	I Group A	**Host Data or Code**. This bus definition pin is used to distinguish data access cycles from code access cycles.
WRJ	I Group A	**Host Write or Read**. When WRJ is driven high, it indicates the current cycle is a write. Inversely, if WRJ is driven low, a read cycle is performed.
HLOCKJ	I Group A	**Host Lock**. When HLOCKJ is asserted by the CPU, the M1531B will recognize the CPU is locking the current cycles.
CACHEJ	I Group A	**Host Cacheable**. This pin is used by the CPU to indicate the system that CPU wants to perform a line fill cycle or a burst write back cycle. If it is driven inactive in a read cycle, the CPU will not cache the returned data, regardless of the state of KENJ.
KENJ/INV	O Group A	**Cache Enable Output**. This signal is connected to the CPU's KENJ and INV pins. KENJ is used to notify the CPU whether the address of the current transaction is cacheable. INV is used during L1 snoop cycles. The M1531B drives this signal high (low) during the EADSJ assertion of a PCI master write (read) snoop cycle.
SMIACTJ	I Group A	**SMM Interrupt Active**. This signal is asserted by the CPU to inform the M1531B that SMM mode is being entered.
HD[63:0]	I/O Group A	**Host Data Bus Lines**. These signals are connected to the CPU's data bus. HD[63] applies to the most significant bit and HD[0] applies to the least significant bit.
MPD[7:0]	I/O Group C	**DRAM Parity /ECC check bits**. These are the 8 bits for parities/ECC check bits over DRAM data bus. MPD[7] applies to the most significant bit and MPD[0] applies to the least significant bit.
RASJ[7] / SRASJ[0]	O Group C	**Row Address Strobe 7**, (FPM/EDO) of DRAM row 7. **SDRAM Row Address Strobe (SDRAM) copy 0**. It connects to SDRAM RASJ. This is a multifunction pin and determined by Index-5Ch bit0.

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Pin Description Table (continued)

Pin Name	Type	Description
DRAM Interface 3.3V/5V Tolerance		
RASJ[6]/ SCASJ[0]	O Group C	**Row Address Strobe 6**, (FPM/EDO) of DRAM row 6. **SDRAM Column address strobe (SDRAM) copy 0**. It connects to SDRAM CASJ. This is a multifunction pin and determined by Index-5Ch bit0.
RASJ5/TIO[9]	I/O Group C	**Row Address Strobe 5,** (FPM/EDO) of DRAM row 5. In SDRAM, they are used to drive the corresponding SDRAM CSJs. **SRAM Tag[9].** It connects to SRAM tag address bit 9. This is a multifunction pin and determined by index-4Ch bits [7:6].
RASJ4/TIO[10]	I/O Group C	**Row Address Strobe 4,** (FPM/EDO) of DRAM row 4. In SDRAM, they are used to drive the corresponding SDRAM CSJs. **SRAM Tag[10].** It connects to SRAM tag address bit 10. This is a multifunction pin and determined by index-4Ch bits [7:6].
RASJ[3:0]	O Group C	**Row Address Strobes**. These signals are used to drive the corresponding RASJs of FPM/EDO DRAMs. In SDRAM, they are used to drive the corresponding SDRAM CSJs.
CASJ[7:0] / DQM[7:0]	O Group C	**Column Address Strobes or Synchronous DRAM Input/Output Data Mask**. These CAS signals should be connected to the corresponding CASJs of each bank of DRAM. The value of CASJs equals that of HBEJs for write cycles. During DRAM read cycles, all of CASJs will be active. In SDRAM, these pins act as synchronized output enables during a read cycle and the byte mask during write cycle, these pins are connected to SDRAM DQM[7:0].
MA[11:2]	O Group C	**DRAM Address Lines**. These signals are the address lines[11:2] of all DRAMs. The M1531B supports DRAM types ranging from 256K to 64Mbits.
MAA[1:0]	O Group C	**Memory Address copy A** for [1:0]. These signals are the address lines[1:0] copy 0 of all DRAMs.
MAB[1:0]/ MA[13:12]	O Group C	**Memory Address copy B** for [1:0]/SDRAM Memory Address lines[13:12]. These signals are the address lines[1:0] copy 1 of FPM/EDO DRAMs. In SDRAM, M1531B automatically changes these pins' function as MA[13:12] to support 64Mbits SDRAM. Please refer to application note in Appendix A.
MWEJ[0]	O Group C	**DRAM Write Enable**. This is the DRAM write enable pin and behaves according to the early-write mechanism, i.e. , it activates before the CASJs do. For refresh cycles, it will remain deasserted.
MD[63:0]	I/O Group C	**Memory Data**. These pins are connected to DRAM's data bits. MD[63] applies to the most significant bit and MD[0] applies to the least significant bit.
CLKEN[0]/ REQJ[4]	I/O Group C	**SDRAM Clock Enable Copy 0** or **PCI Master Request**. This signal is used as SDRAM clock enable copy 0 to do self refresh during suspend. This pin can also be used as bus request signal of the fifth PCI master. This function is controlled by Index -5Dh bit 1.
CLKEN[1]/ GNTJ[4]	O Group C	**SDRAM Clock Enable Copy 1** or **PCI Master Grant**. This signal is used as SDRAM clock enable copy 1 to do self refresh during suspend. This pin can also be used as grant signal of the fifth PCI master. This function is controlled by Index -5Dh bit 1.
Secondary Cache Interface 3.3V/2.5V		
CADVJ	O Group A	**Synchronous SRAM Advance**. This signal will make PBSRAM internal burst address counter advance.
CADSJ	O Group A	**Synchronous SRAM Address Strobe**. This signal connects to PBSRAM ADSCJ.
CCSJ	O Group A	**Synchronous SRAM Chip Select**. This signal connects to PBSRAM CE1J to mask ADSPJ and enable ADSCJ sampling.
GWEJ	O Group A	**Synchronous SRAM Global Write Enable**. This signal will write all the byte lanes data into PBSRAM.

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COEJ	O Group A	**Synchronous SRAM Output Enable**. This signal will enable the data output driving of PBSRAM.
BWEJ	O Group A	**Synchronous SRAM Byte-Write Enable**. This signal connects to byte write enable of PBSRAM.

Pin Description Table (continued)

Pin Name	Type	Description
Secondary Cache Interface 3.3V/5V Tolerance		
MWEJ[1]	I/O Group C	**Another copy of MWEJ**. This pin is used for multifunction in M1531. In M1531B, this pin is always as another copy of MWEJ. BIOS should fix the programming index-41h bit 6, bit 3 and bit 0 as '110'.
SRASJ[1]	I/O Group C	**Synchronous DRAM (SDRAM) RAS copy 1**. This pin is used for multifunction in M1531. In M1531B, this pin is always as synchronous DRAM (SDRAM) RAS copy 1. BIOS should fix the programming index-41h bit 3 and bit0 as '10'.
SCASJ[1]	I/O Group C	**Synchronous DRAM (SDRAM) CAS copy 1**. This pin is used for multifunction in M1531. In M1531B, this pin is always as synchronous DRAM CAS copy 1. BIOS should fix the programming index-41h bit 3 and bit 0 as '10'.
TIO[8:0]	I/O Group B	**SRAM Tag[8:0]**. This pin contains the L2 tag address for 256 KB L2 caches. TIO[6:0] contain the L2 tag address and TIO7 contains the L2 cache valid bit for 512 KB caches. TIO[5:0] contain L2 tag address, TIO7 contains L2 cache valid bit and TIO6 contains the L2 cache dirty bit for 1MB cache. TIO[8] is the tag address bit 8 and supports cacheable region up to 128MB.
TAGWEJ	O Group B	**Tag Write Enable**. This signal, when asserted, will write into the external tag new state and tag addresses.
PCI Interface 3.3V/5V Tolerance		
AD[31:0]	I/O Group B	**PCI Address and Data Bus Lines**. These lines are connected to the PCI bus. AD[31:0] contain the information of address or data for PCI transactions.
CBEJ[3:0]	I/O Group B	**PCI Bus Command and Byte Enables**. Bus commands and byte enables are multiplexed in these lines for address and data phases, respectively.
FRAMEJ	I/O Group B	**Cycle Frame of PCI Buses**. This indicates the beginning and duration of a PCI access. It will be as an output driven by M1531B on behalf of CPU, or as an input during PCI master access.
DEVSELJ	I/O Group B	**Device Select**. When the target device has decoded the address as its own cycle, it will assert DEVSELJ.
IRDYJ	I/O Group B	**Initiator Ready**. This signal indicates the initiator is ready to complete the current data phase of transaction.
TRDYJ	I/O Group B	**Target Ready**. This pin indicates the target is ready to complete the current data phase of transaction.
STOPJ	I/O Group B	**Stop**. This signal indicates the target is requesting the master to stop the current transaction.
LOCKJ	I/O Group B	**Lock Resource Signal**. This pin indicates the PCI master or the bridge intends to do exclusive transfers.
REQJ[3:0]	I Group B	**Bus Request signals of PCI Masters**. When asserted, it means the PCI Master is requesting the PCI bus ownership from the arbiter.
GNTJ[3:0]	O Group B	**Grant signals to PCI Masters**. When asserted by the arbiter, it means the PCI master has been legally granted to own the PCI bus.
PHLDJ	I Group B	**PCI bus Hold Request**. This active low signal is a request from M1533/M1543 for the PCI bus.
PHLDAJ	O Group B	**PCI bus Hold Acknowledge**. This active low signal grants PCI bus to M1533/M1543.
PAR	I/O Group B	**Parity bit of PCI bus**. It is the even parity bit across PAD[31:0] and CBEJ[3:0].
SERRJ/ CLKRUNJ	I/O Group B	**System Error or PCI Clock RUN**. If the M1531B detects parity errors in DRAMs, it will assert SERRJ to notify the system. As CLKRUNJ, this signal will connect to M1533 CLKRUNJ to start, or maintain the PCI CLOCK. It is a multifunction pin and determined by Index-77h bit0.

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Pin Description Table (continued)

Pin Name	Type	Description
Clock, Reset, and Suspend		
HCLKIN	I Group A	**CPU bus Clock Input**. This signal is used by all of the M1531B logic that is in the Host clock domain.
RSTJ	I Group B	**System Reset**. This pin, when asserted, resets the M1531B state machine, and sets the register bits to their default values.
PCICLK	I Group B	**PCI bus Clock Input**. This signal is used by all of the M1531B logic that is in the PCI clock domain.
PCIMRQJ	O Group B	**Total PCI Request**. This signal is used to notify M1533/M1543 there is PCI master requesting PCI bus.
SUSPENDJ	I Group C	**Suspend**. When actively sampled, the M1531B will enter the I/O suspend mode. This signal should be pulled high when the suspend feature is disabled.
OSC32KO	I Group C	The refresh reference clock of frequency 32KHz during suspend mode. This signal should be pulled to a fixed value when the suspend feature is disabled.
Power Pins		
VCC_A	P	**Vcc 3.3V or 2.5V Power for Group A.** This power is used for CPU interface and L2 control signals. If this power connects to 3.3V, the relative signals will output 3.3V and accept 3.3V input. If this power connects to 2.5V, the relative signals will output 2.5V and accept 2.5V input.
VCC_B	P	**Vcc 3.3V Power for Group B.** This power is used for PCI interface and Tag signals. It must connect to 3.3V. The relative signals will output 3.3V and 5V input tolerance.
VCC_C	P	**Vcc 3.3V Power for Group C.** This power is used for DRAM interface signals during normal operation and suspend refresh. It must connect to 3.3V. The relative signals will output 3.3V and 5V input tolerance.
VDD_5	P	**Vcc 5.0V Power for Group A and Group B.** This pin supplies the 5V input tolerance circuit and the core power for the internal circuit except the suspend circuit.
VDD_5S	P	**Vcc 5.0V Power for Group C.** This pin supplies the 5V input tolerance circuit and the core power for the internal suspend circuit.
Vss or Gnd	P	**Ground**

2.3 Numerical Pin List

Pin no.	Pin name	Type
A1	--	-
A2	PHLDAJ	O
A3	AD3	I/O
A4	AD6	I/O
A5	AD8	I/O
A6	AD12	I/O
A7	PAR	I/O
A8	TRDYJ	I/O
A9	AD17	I/O
A10	AD22	I/O
A11	AD25	I/O
A12	AD30	I/O
A13	REQJ3	I
A14	GNTJ2	O
A15	GNTJ3	O
A16	MPD2	I/O
A17	MPD0	I/O
A18	MD61	I/O
A19	MD29	I/O
A20	MD62	I/O
B1	BEJ0	I
B2	PHLDJ	I
B3	AD2	I/O
B4	AD5	I/O
B5	AD7	I/O
B6	AD11	I/O
B7	CBEJ1	I/O
B8	DEVSELJ	I/O
B9	AD16	I/O
B10	AD21	I/O
B11	AD24	I/O
B12	AD29	I/O
B13	REQJ2	I
B14	GNTJ1	O
B15	MPD5	I/O
B16	MPD1	I/O
B17	MD63	I/O
B18	MD27	I/O
B19	MD60	I/O
B20	MD28	I/O
C1	BEJ3	I
C2	BEJ2	I
C3	BEJ1	I
C4	AD4	I/O
C5	CBEJ0	I/O

Pin no.	Pin name	Type
C6	AD10	I/O
C7	AD15	I/O
C8	STOPJ	I/O
C9	CBEJ2	I/O
C10	AD20	I/O
C11	CBEJ3	I/O
C12	AD28	I/O
C13	REQJ1	I
C14	GNTJ0	O
C15	MPD4	I/O
C16	MD30	I/O
C17	MD25	I/O
C18	MD58	I/O
C19	MD26	I/O
C20	MD59	I/O
D1	BEJ6	I
D2	BEJ5	I
D3	BEJ4	I
D4	AD0	I/O
D5	AD1	I/O
D6	AD9	I/O
D7	AD14	I/O
D8	LOCKJ	I/O
D9	FRAMEJ	I/O
D10	AD19	I/O
D11	AD23	I/O
D12	AD27	I/O
D13	REQJ0	I
D14	MPD7	I/O
D15	MPD3	I/O
D16	MD55	I/O
D17	MD23	I/O
D18	MD56	I/O
D19	MD24	I/O
D20	MD57	I/O
E1	DCJ	I
E2	HITMJ	I
E3	EADSJ	O
E4	BEJ7	I
E5	RSTJ	I
E6	PCIMRQJ	O
E7	AD13	I/O
E8	SERRJ	I/O
E9	IRDYJ	I/O
E10	AD18	I/O

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Numerical Pin List (continued)

Pin no.	Pin name	Type
E11	PCLKIN	I
E12	AD26	I/O
E13	AD31	I/O
E14	MPD6	I/O
E15	MD31	I/O
E16	MD20	I/O
E17	MD53	I/O
E18	MD21	I/O
E19	MD54	I/O
E20	MD22	I/O
F1	BRDYJ	O
F2	BOFFJ	O
F3	SMIACTJ	I
F4	HLOCKJ	I
F5	ADSJ	I
F6	VCC_B	P
F14	VCC_C	P
F15	VCC_C	P
F16	MD50	I/O
F17	MD18	I/O
F18	MD51	I/O
F19	MD19	I/O
F20	MD52	I/O
G1	HD63	I/O
G2	CACHEJ	I
G3	AHOLD	O
G4	KENJ	O
G5	NAJ	O
G6	VCC_A	P
G15	VCC_C	P
G16	MD15	I/O
G17	MD48	I/O
G18	MD16	I/O
G19	MD49	I/O
G20	MD17	I/O
H1	HD60	I/O
H2	HD61	I/O
H3	HD62	I/O
H4	WRJ	I
H5	MIOJ	I
H8		
H9		
H10		
H11		
H12		
H13		
H16	MD45	I/O
H17	MD13	I/O
H18	MD46	I/O
H19	MD14	I/O

Pin no.	Pin name	Type
H20	MD47	I/O
J1	HD55	I/O
J2	HD56	I/O
J3	HD57	I/O
J4	HD58	I/O
J5	HD59	I/O
J8		
J9	GND	P
J10	GND	P
J11	GND	P
J12	GND	P
J13		
J16	MD10	I/O
J17	MD43	I/O
J18	MD11	I/O
J19	MD44	I/O
J20	MD12	I/O
K1	HD51	I/O
K2	HD52	I/O
K3	HD53	I/O
K4	HD54	I/O
K5	HCLKIN	I
K8		
K9	GND	P
K10	GND	P
K11	GND	P
K12	GND	P
K13		
K16	MD40	I/O
K17	MD8	I/O
K18	MD41	I/O
K19	MD9	I/O
K20	MD42	I/O
L1	HD46	I/O
L2	HD47	I/O
L3	HD48	I/O
L4	HD49	I/O
L5	HD50	I/O
L8		
L9	GND	P
L10	GND	P
L11	GND	P
L12	GND	P
L13		
L16	MD5	I/O
L17	MD38	I/O
L18	MD6	I/O
L19	MD39	I/O
L20	MD7	I/O
M1	HD41	I/O

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Numerical Pin List (continued)

Pin no.	Pin name	Type
M2	HD42	I/O
M3	HD43	I/O
M4	HD44	I/O
M5	HD45	I/O
M8		
M9	GND	P
M10	GND	P
M11	GND	P
M12	GND	P
M13		
M16	MD35	I/O
M17	MD3	I/O
M18	MD36	I/O
M19	MD4	I/O
M20	MD37	I/O
N1	HD36	I/O
N2	HD37	I/O
N3	HD38	I/O
N4	HD39	I/O
N5	HD40	I/O
N8		
N9		
N10		
N11		
N12		
N13		
N15	VDD5S	P
N16	REQJ4	I/O
N17	GNTJ4	O
N18	MD1	I/O
N19	MD34	I/O
N20	MD2	I/O
P1	HD31	I/O
P2	HD32	I/O
P3	HD33	I/O
P4	HD34	I/O
P5	HD35	I/O
P6	VCC_A	P
P15	VCC_C	P
P16	32K	I
P17	SUSPENDJ	I
P18	MD32	I/O
P19	MD0	I/O
P20	MD33	I/O
R1	HD26	I/O
R2	HD27	I/O
R3	HD28	I/O
R4	HD29	I/O
R5	HD30	I/O
R6	VDD5	P

Pin no.	Pin name	Type
R7	VCC_A	P
R14	VCC_B	P
R15	VCC_C	P
R16	RASJ6	O
R17	RASJ7	O
R18	CASJ2	O
R19	CASJ7	O
R20	CASJ3	O
T1	HD21	I/O
T2	HD22	I/O
T3	HD23	I/O
T4	HD24	I/O
T5	HD25	I/O
T6	HD0	I/O
T7	A12	I/O
T8	A5	I/O
T9	GWEJ	O
T10	COEJ	O
T11	CADVJ	O
T12	TWEJ	O
T13	MAA0	O
T14	MAA1	O
T15	SCASJ1	I/O
T16	SRASJ1	I/O
T17	MWEJ1	I/O
T18	RASJ1	O
T19	RASJ0	O
T20	CASJ6	O
U1	HD16	I/O
U2	HD17	I/O
U3	HD18	I/O
U4	HD19	I/O
U5	HD20	I/O
U6	HD1	I/O
U7	A13	I/O
U8	A8	I/O
U9	CCSJ	O
U10	BWEJ	O
U11	CADSJ	O
U12	TIO0	I/O
U13	TIO1	I/O
U14	MAB0	O
U15	MAB1	O
U16	MA5	O
U17	MWEJ	I/O
U18	RASJ4	O
U19	RASJ3	O
U20	RASJ2	O
V1	HD15	I/O
V2	HD14	I/O

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Numerical Pin List (continued)

Pin no.	Pin name	Type
V3	HD13	I/O
V4	HD6	I/O
V5	HD3	I/O
V6	A17	I/O
V7	A14	I/O
V8	A10	I/O
V9	A4	I/O
V10	A29	I/O
V11	A25	I/O
V12	A24	I/O
V137	A23	I/O
V14	TIO2	I/O
V15	MA2	O
V16	MA4	O
V17	MA8	O
V18	CASJ5	O
V19	CASJ1	O
V20	RASJ5	O
W1	HD12	I/O
W2	HD11	I/O
W3	HD10	I/O
W4	HD5	I/O
W5	HD2	I/O
W6	A18	I/O
W7	A15	I/O
W8	A11	I/O
W9	A7	I/O
W10	A30	I/O
W11	A31	I/O
W12	A22	I/O
W13	A21	I/O
W14	TIO4	I/O
W15	TIO6	I/O
W16	MA3	O
W17	MA7	O
W18	MA10	O
W19	CASJ0	O
W20	CASJ4	O
Y1	HD9	I/O
Y2	HD8	I/O
Y3	HD7	I/O
Y4	HD4	I/O
Y5	A20	I/O
Y6	A19	I/O
Y7	A16	I/O
Y8	A9	I/O
Y9	A6	I/O
Y10	A3	I/O
Y11	A28	I/O
Y12	A26	I/O
Y13	A27	I/O
Y14	TIO3	I/O
Y15	TIO5	I/O
Y16	TIO7	I/O
Y17	MA6	O
Y18	MA9	O
Y19	MA11	O
Y20	TIO8	I/O

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2.4 Alphabetical Pin List

Pin no.	Pin name	Type
A1	--	-
P16	32K	I
Y10	A3	I/O
V9	A4	I/O
T8	A5	I/O
Y9	A6	I/O
W9	A7	I/O
U8	A8	I/O
Y8	A9	I/O
V8	A10	I/O
W8	A11	I/O
T7	A12	I/O
U7	A13	I/O
V7	A14	I/O
W7	A15	I/O
Y7	A16	I/O
V6	A17	I/O
W6	A18	I/O
Y6	A19	I/O
Y5	A20	I/O
W13	A21	I/O
W12	A22	I/O
V137	A23	I/O
V12	A24	I/O
V11	A25	I/O
Y12	A26	I/O
Y13	A27	I/O
Y11	A28	I/O
V10	A29	I/O
W10	A30	I/O
W11	A31	I/O
D4	AD0	I/O
D5	AD1	I/O
B3	AD2	I/O
A3	AD3	I/O
C4	AD4	I/O
B4	AD5	I/O
A4	AD6	I/O
B5	AD7	I/O
A5	AD8	I/O
D6	AD9	I/O
C6	AD10	I/O
B6	AD11	I/O
A6	AD12	I/O
E7	AD13	I/O
D7	AD14	I/O
C7	AD15	I/O
B9	AD16	I/O
A9	AD17	I/O
E10	AD18	I/O
D10	AD19	I/O
C10	AD20	I/O
B10	AD21	I/O
A10	AD22	I/O
D11	AD23	I/O
B11	AD24	I/O
A11	AD25	I/O
E12	AD26	I/O
D12	AD27	I/O
C12	AD28	I/O
B12	AD29	I/O
A12	AD30	I/O
E13	AD31	I/O
F5	ADSJ	I
G3	AHOLD	O
B1	BEJ0	I
C3	BEJ1	I
C2	BEJ2	I
C1	BEJ3	I
D3	BEJ4	I
D2	BEJ5	I
D1	BEJ6	I
E4	BEJ7	I
F2	BOFFJ	O
F1	BRDYJ	O
U10	BWEJ	O
G2	CACHEJ	I
U11	CADSJ	O
T11	CADVJ	O
W19	CASJ0	O
V19	CASJ1	O
R18	CASJ2	O
R20	CASJ3	O
W20	CASJ4	O
V18	CASJ5	O
T20	CASJ6	O
R19	CASJ7	O
C5	CBEJ0	I/O
B7	CBEJ1	I/O
C9	CBEJ2	I/O

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Alphabetical Pin List (continued)

Pin no.	Pin name	Type
C11	CBEJ3	I/O
U9	CCSJ	O
T10	COEJ	O
E1	DCJ	I
B8	DEVSELJ	I/O
E3	EADSJ	O
D9	FRAMEJ	I/O
H10		
H11		
H12		
H13		
H8		
H9		
J10	GND	P
J11	GND	P
J12	GND	P
J13		
J8		
J9	GND	P
K10	GND	P
K11	GND	P
K12	GND	P
K13		
K8		
K9	GND	P
L10	GND	P
L11	GND	P
L12	GND	P
L13		
L8		
L9	GND	P
M10	GND	P
M11	GND	P
M12	GND	P
M13		
M8		
M9	GND	P
N10		
N11		
N12		
N13		
N8		
N9		
C14	GNTJ0	O
B14	GNTJ1	O
A14	GNTJ2	O
A15	GNTJ3	O
N17	GNTJ4	O
T9	GWEJ	O
K5	HCLKIN	I

Pin no.	Pin name	Type
T6	HD0	I/O
U6	HD1	I/O
W5	HD2	I/O
V5	HD3	I/O
Y4	HD4	I/O
W4	HD5	I/O
V4	HD6	I/O
Y3	HD7	I/O
Y2	HD8	I/O
Y1	HD9	I/O
W3	HD10	I/O
W2	HD11	I/O
W1	HD12	I/O
V3	HD13	I/O
V2	HD14	I/O
V1	HD15	I/O
U1	HD16	I/O
U2	HD17	I/O
U3	HD18	I/O
U4	HD19	I/O
U5	HD20	I/O
T1	HD21	I/O
T2	HD22	I/O
T3	HD23	I/O
T4	HD24	I/O
T5	HD25	I/O
R1	HD26	I/O
R2	HD27	I/O
R3	HD28	I/O
R4	HD29	I/O
R5	HD30	I/O
P1	HD31	I/O
P2	HD32	I/O
P3	HD33	I/O
P4	HD34	I/O
P5	HD35	I/O
N1	HD36	I/O
N2	HD37	I/O
N3	HD38	I/O
N4	HD39	I/O
N5	HD40	I/O
M1	HD41	I/O
M2	HD42	I/O
M3	HD43	I/O
M4	HD44	I/O
M5	HD45	I/O
L1	HD46	I/O
L2	HD47	I/O
L3	HD48	I/O
L4	HD49	I/O

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Alphabetical Pin List (continued)

Pin no.	Pin name	Type
L5	HD50	I/O
K1	HD51	I/O
K2	HD52	I/O
K3	HD53	I/O
K4	HD54	I/O
J1	HD55	I/O
J2	HD56	I/O
J3	HD57	I/O
J4	HD58	I/O
J5	HD59	I/O
H1	HD60	I/O
H2	HD61	I/O
H3	HD62	I/O
G1	HD63	I/O
E2	HITMJ	I
F4	HLOCKJ	I
E9	IRDYJ	I/O
G4	KENJ	O
D8	LOCKJ	I/O
V15	MA2	O
W16	MA3	O
V16	MA4	O
U16	MA5	O
Y17	MA6	O
W17	MA7	O
V17	MA8	O
Y18	MA9	O
W18	MA10	O
Y19	MA11	O
T13	MAA0	O
T14	MAA1	O
U14	MAB0	O
U15	MAB1	O
P19	MD0	I/O
N18	MD1	I/O
N20	MD2	I/O
M17	MD3	I/O
M19	MD4	I/O
L16	MD5	I/O
L18	MD6	I/O
L20	MD7	I/O
K17	MD8	I/O
K19	MD9	I/O
J16	MD10	I/O
J18	MD11	I/O
J20	MD12	I/O
H17	MD13	I/O
H19	MD14	I/O
G16	MD15	I/O
G18	MD16	I/O
G20	MD17	I/O
F17	MD18	I/O
F19	MD19	I/O
E16	MD20	I/O
E18	MD21	I/O
E20	MD22	I/O
D17	MD23	I/O
D19	MD24	I/O
C17	MD25	I/O
C19	MD26	I/O
B18	MD27	I/O
B20	MD28	I/O
A19	MD29	I/O
C16	MD30	I/O
E15	MD31	I/O
P18	MD32	I/O
P20	MD33	I/O
N19	MD34	I/O
M16	MD35	I/O
M18	MD36	I/O
M20	MD37	I/O
L17	MD38	I/O
L19	MD39	I/O
K16	MD40	I/O
K18	MD41	I/O
K20	MD42	I/O
J17	MD43	I/O
J19	MD44	I/O
H16	MD45	I/O
H18	MD46	I/O
H20	MD47	I/O
G17	MD48	I/O
G19	MD49	I/O
F16	MD50	I/O
F18	MD51	I/O
F20	MD52	I/O
E17	MD53	I/O
E19	MD54	I/O
D16	MD55	I/O
D18	MD56	I/O
D20	MD57	I/O
C18	MD58	I/O
C20	MD59	I/O
B19	MD60	I/O
A18	MD61	I/O
A20	MD62	I/O
B17	MD63	I/O
H5	MIOJ	I
A17	MPD0	I/O
B16	MPD1	I/O

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Alphabetical Pin List (continued)

Pin no.	Pin name	Type
A16	MPD2	I/O
D15	MPD3	I/O
C15	MPD4	I/O
B15	MPD5	I/O
E14	MPD6	I/O
D14	MPD7	I/O
U17	MWEJ	I/O
T17	MWEJ1	I/O
G5	NAJ	O
A7	PAR	I/O
E6	PCIMRQJ	O
E11	PCLKIN	I
A2	PHLDAJ	O
B2	PHLDJ	I
T19	RASJ0	O
T18	RASJ1	O
U20	RASJ2	O
U19	RASJ3	O
U18	RASJ4	O
V20	RASJ5	O
R16	RASJ6	O
R17	RASJ7	O
D13	REQJ0	I
C13	REQJ1	I
B13	REQJ2	I
A13	REQJ3	I
N16	REQJ4	I/O
E5	RSTJ	I
T15	SCASJ1	I/O
E8	SERRJ	I/O
F3	SMIACTJ	I
T16	SRASJ1	I/O
C8	STOPJ	I/O
P17	SUSPENDJ	I
U12	TIO0	I/O
U13	TIO1	I/O
V14	TIO2	I/O
Y14	TIO3	I/O
W14	TIO4	I/O
Y15	TIO5	I/O
W15	TIO6	I/O
Y16	TIO7	I/O
Y20	TIO8	I/O
A8	TRDYJ	I/O
T12	TWEJ	O
F14	VCC_C	P
F15	VCC_C	P
F6	VCC_B	P
G15	VCC_C	P
G6	VCC_A	P
P6	VCC_A	P
P15	VCC_C	P
R14	VCC_B	P
R15	VCC_C	P
R7	VCC_A	P
R6	VDD5	P
N15	VDD5S	P
H4	WRJ	I

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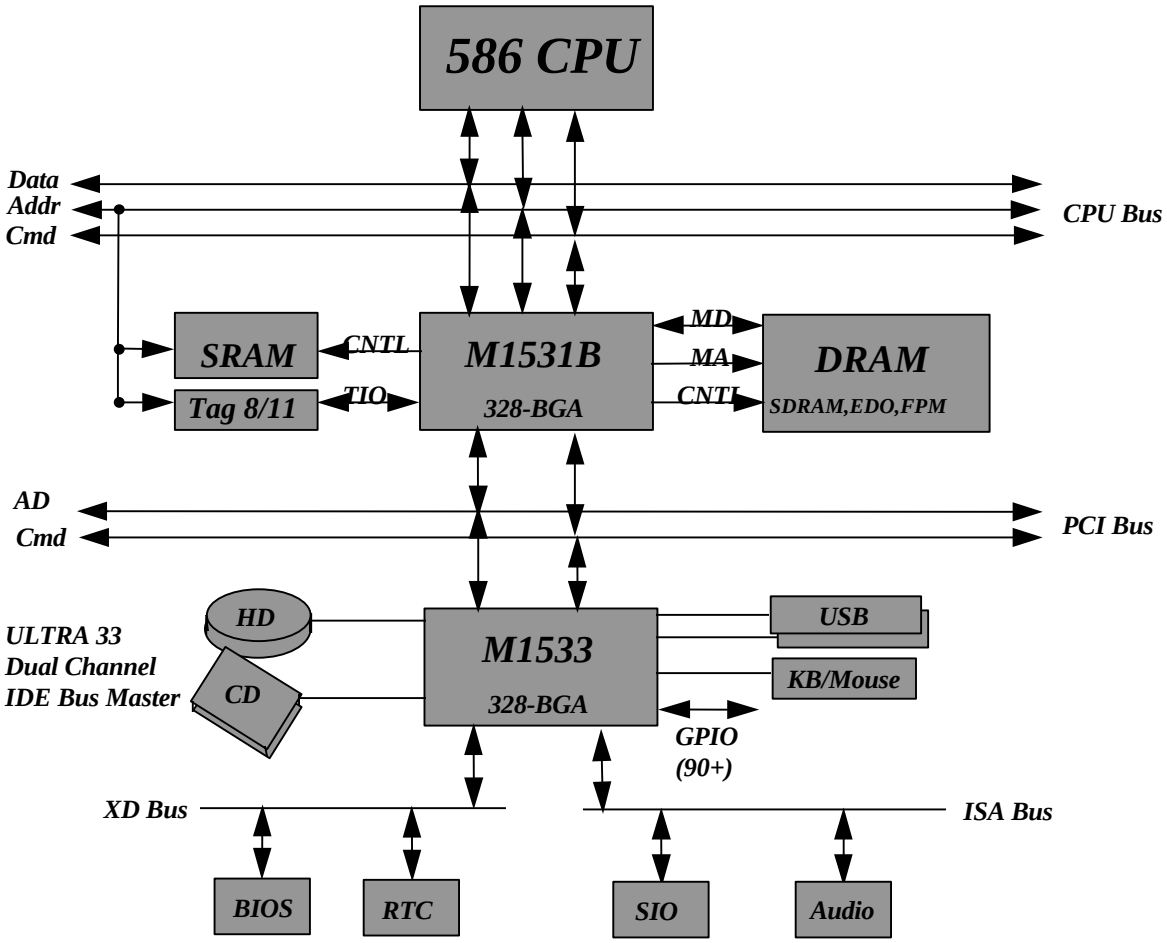
Section 3 : Function Description

3.1 System Architecture

In the following illustration, ALADDIN-IV gives a highly integrated system solution and a most up-to-date system architecture, which includes the Parity/ECC, PBSRAM, SDRAM, ACPI, Ultra-33 IDE Master, USB, PS2 Keyboard/Mouse, and highly concurrent multibus with smart deep FIFO between the buses, such as the HOST/ DRAM/PCI/ ISA/ DEDICATED IDE/USB buses. Using Aladdin-IV, you can achieve a TTL free solution and provide the best system performance.



Aladdin IV System Block Diagram with M1533

The M1531B provides a complete integrated solution for the system controller and data path components in a Pentium processor system. It provides a 64-bit CPU bus interface, 32-bit PCI bus interface, 64/72 DRAM data bus with ECC or parity, secondary cache interface including Pipelined Burst SRAM or Memory Cache, PCI master to DRAM interface, and 5 PCI masters, CPU, and M1533/M1543 arbiter. The following figure shows the highly efficient data path in the M1531B. The M1531B bus interfaces are designed to interface with 2.5V, 3.3V and 5V buses. It directly connects to 3.3V or 2.5V CPU bus, 3.3V or 5V Tag, 3.3V or 5V DRAM bus, and 3.3V or 5V PCI bus.

The M1533 provides a highly integrated PCI-to-ISA bridge solution for the best Notebook system. It comprises a 2-channel dedicated Ultra-33 IDE master interface, Plug-and-Play port, APIC interface, PS/2 keyboard and mouse controller, 2-port Universal Serial Bus feature, PCI 2.1 Compliance operation, ACPI, and Enhanced Green function.

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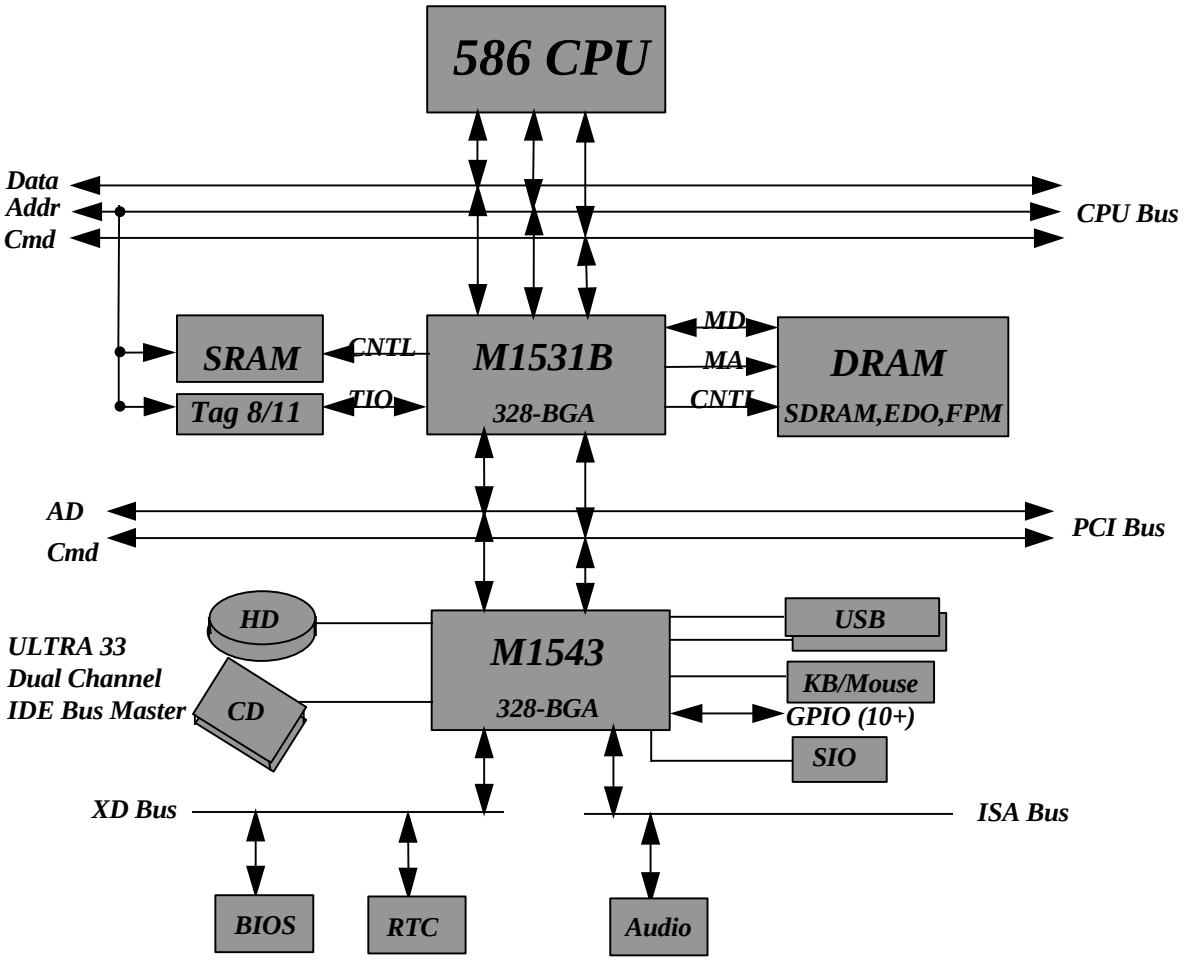
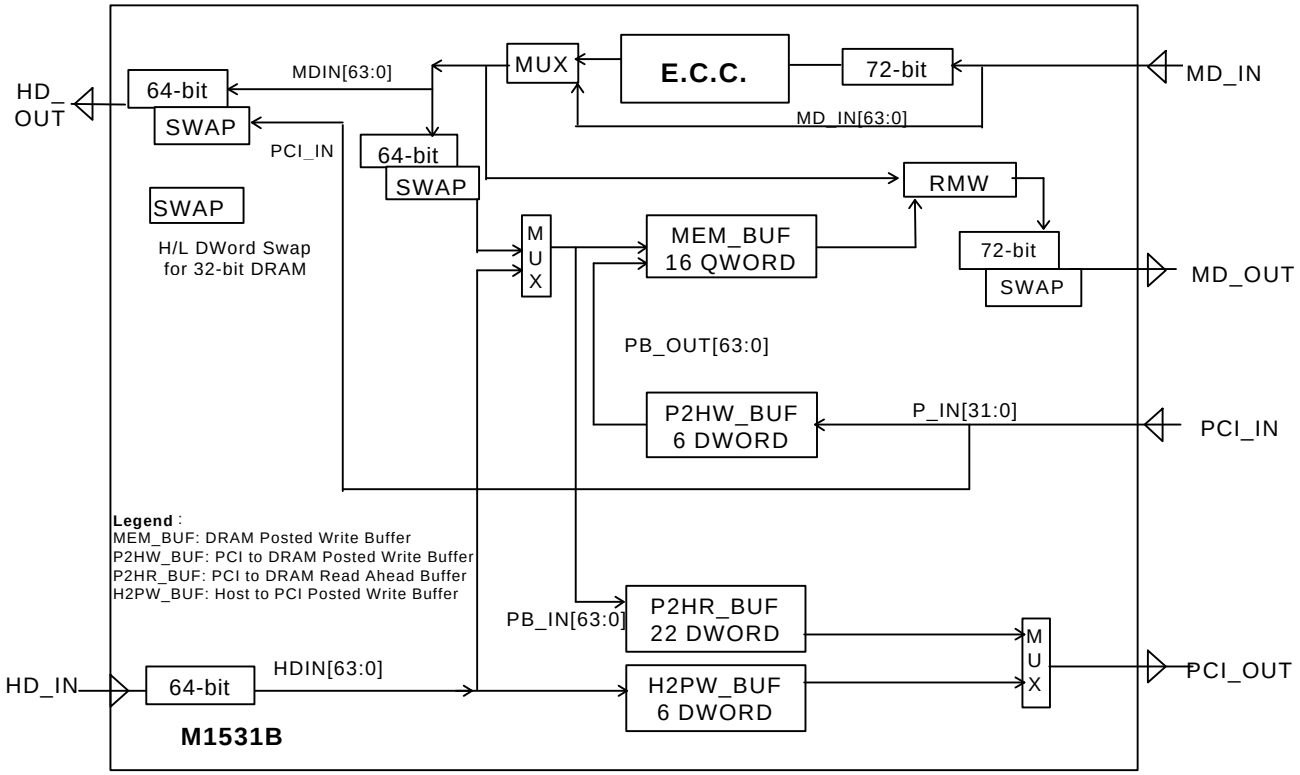
The M1543 provides a highly integrated PCI-to-ISA bridge solution for the best Desktop system. It comprises a 2-channel dedicated Ultra-33 IDE master interface, Plug-and-Play port, APIC interface, PS/2 keyboard and mouse controller, 2-port Universal Serial Bus feature, PCI 2.1 Compliance operation, ACPI, Green function, and the Super I/O function.



Aladdin IV System Block Diagram with M1543

Data Path and Buffer Architecture of M1531B



3.2 CPU Interface

The M1531B supports all Pentium-class CPUs including Intel P54C/P55C, Cyrix M1, AMD K5, and Ti Dakota. Furthermore, M1531B supports a high performance CPU interface to Cyrix M2, and AMD K6 with higher CPU bus frequency (up to 83.3 MHz) to achieve the Pentium Pro-class system performance. M1531B also supports Cyrix Linear Wrap mode for M1 and M2 to gain the best system performance. M1531B can also interface to 2.5V CPU I/O interface for Notebook use. In the higher CPU bus frequency interface, M1531B will do the so-called pseudo-synchronous design instead of the asynchronous design. When 75/83.3 MHz CPU bus is used, the PCI bus will be running at 30/33 MHz (divide CPU bus by 2.5). The pseudo-synchronous clock design is a better solution than the pure asynchronous clock design, it eliminates the performance degradation to synchronize two asynchronous buses and helps the chip reliability to resolve the chip testing issue.

3.3 Clock Design Philosophy

The system provides 3 clocks for M1531B, HCLKIN has the same frequency with the CPUCLK, Cache clock, and SDRAM clock. PCLKIN has the same frequency with the PCI bus clock, and 32K is a 32K frequency clock from M1533/M1543 CLK32KO or from the system board clock source. System designer should minimize the clock skew between CPUCLK, Cache clock, SDRAM clock, and HCLKIN, and also the skew between PCLKIN and PCI bus clock. Regarding the skew between M1531B's HCLKIN and PCLKIN, PCLKIN should lag HCLKIN for 1 ~ 4 ns. The internal clock design philosophy uses the HCLKIN running the state machine of CPU interface, L2 controller, and DRAM controller, and uses the PCLKIN running the PCI state machine, and automatically takes good care of the internal signal interface between different clock frequency state machines. Also M1531B will support the internal smart clock control, it will shut off the internal clock when the CPU or PCI bus is idle to save the power consumption. 32K clock is used for the DRAM Suspend refresh clock. It is a clock input and not necessarily relative to HCLKIN or PCLKIN.

3.4 Cache Memory Timing/Configuration

The M1531B integrates a high performance L2 write back/dynamic-writeback direct mapping cache controller using MESI protocol of L1 and L2, and has an L2 MESI tag 8Kx2 bits built-in to maintain the data coherence for optimizing CPU bus utilization. The L2 cache can be configured for Memory Cache or Pipelined Burst SRAM with cache size ranging from 256KB, 512KB to 1MB. The cacheable region can be up to 512MB under 256KB cache memory configuration, by using 11-bit tag option. Or, by using an 8Kx8 tag RAM, the cacheable region of the system is 64MB. The controller can perform a dynamic-writeback cycle to DRAM, which the L1 write cycle will be directed to DRAM intelligently with 3-1-1-1 timing without stalling the CPU execution. Also M1531B can support the CPU single read cycle L2 allocation feature, M1531B will do the L2 line fill even when the CPU issues only a single read cycle to improve the L2 hit rate for some special application. The following table shows the best performance for the L2 Read/Write access.

The timing of cache memory system is shown in following table :

	READ	WRITE	B2B READ	B2B WRITE
PBSRAM and Memory cache	3-1-1-1	3-1-1-1	3-1-1-1-1-1-1-1	3-1-1-1-1-1-1-1

The following L2 Cache Table shows the different configurations supported by M1531B.

Configuration	**DATA SRAM**			**TAG SRAM**				**Internal**	**Note**
Cache Size	Size	Bank	Address lines	Address lines	Data Lines	Tag Size	Cacheable DRAM Size	**MESI**	
256K	(32K32)*2	1	A3-A17	A5-A17	A18-A25	8K8	64M	8K2	
512K	(64K16)*4	1	A3-A18	A5-A18	A19-A25	16K8	64M	16K1 dirty bit	TAG[6] as valid bit
512K	(32K32)*4	2	A3-A18	A5-A18	A19-A25	16K8	64M	16K1 dirty bit	TAG[6] as valid bit
1M	(64K32)*4	2	A3-A19	A5-A19	A20-A25	32K8	64M	disable	TAG[6] as valid bit, TAG[7] as dirty bit
256K	(32K32)*2	1	A3-A17	A5-A17	A18-A26	8K9	128M	8K2	
512K	(64K16)*4	1	A3-A18	A5-A18	A19-A26	16K9	128M	16K1 dirty bit	TAG[6] as valid bit
512K	(32K32)*4	2	A3-A18	A5-A18	A19-A26	16K9	128M	16K1 dirty bit	TAG[6] as valid bit
1M	(64K32)*4	2	A3-A19	A5-A19	A20-A26	32K9	128M	disable	TAG[6] as valid bit, TAG[7] as dirty bit
256K	(32K32)*2	1	A3-A17	A5-A17	A18-A27	8K10	256M	8K2	
512K	(64K16)*4	1	A3-A18	A5-A18	A19-A27	16K10	256M	16K1 dirty bit	TAG[6] as valid bit
512K	(32K32)*4	2	A3-A18	A5-A18	A19-A27	16K10	256M	16K1 dirty bit	TAG[6] as valid bit
1M	(64K32)*4	2	A3-A19	A5-A19	A20-A27	32K10	256M	disable	TAG[6] as valid bit, TAG[7] as dirty bit
256K	(32K32)*2	1	A3-A17	A5-A17	A18-A28	8K11	512M	8K2	
512K	(64K16)*4	1	A3-A18	A5-A18	A19-A28	16K11	512M	16K1 dirty bit	TAG[6] as valid bit
512K	(32K32)*4	2	A3-A18	A5-A18	A19-A28	16K11	512M	16K1 dirty bit	TAG[6] as valid bit
1M	(64K32)*4	2	A3-A19	A5-A19	A20-A28	32K11	512M	disable	TAG[6] as valid bit, TAG[7] as dirty bit

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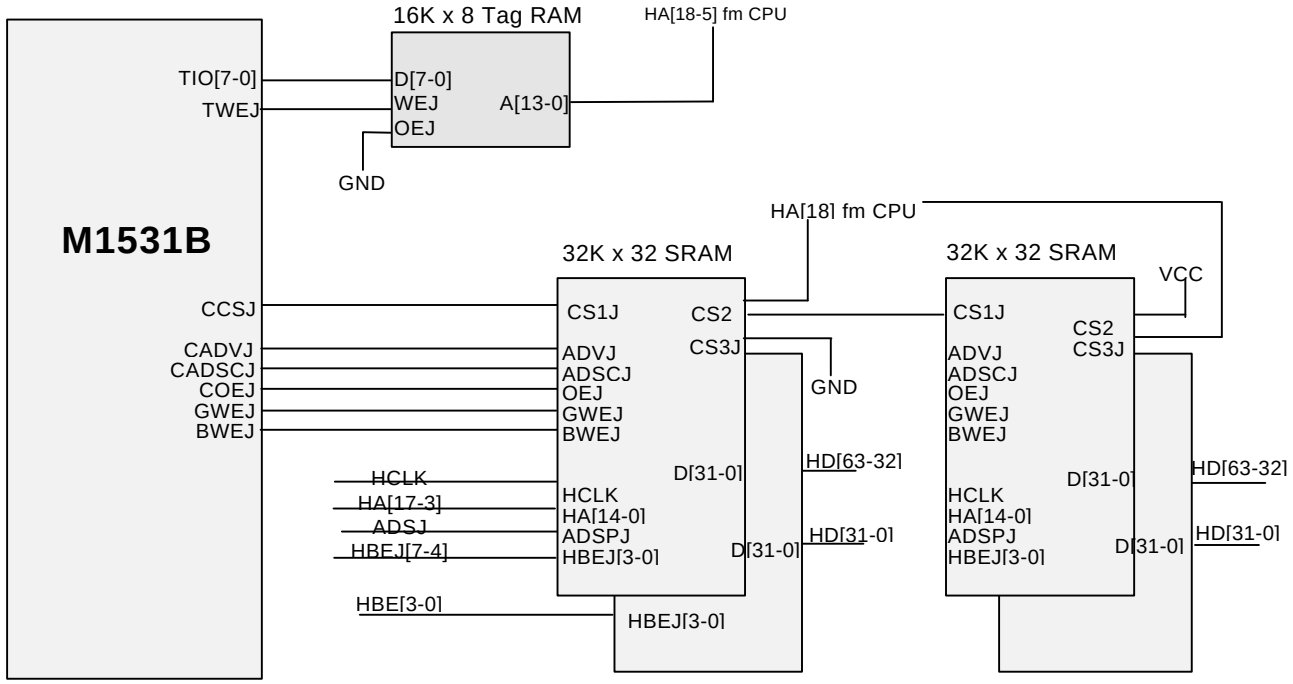
The following table shows the different standard SRAM access time requirements for different CPU clock frequencies.

CPU Bus Frequency (MHz)	PBSRAM Clock-to-Output Access Time (ns)	Tag RAM Access Time (ns)
50	13.5	20
60	10	15
66	8.5	15
75	7	12
83.3	6	10

In the following figures, two recommended cache subsystems are shown as follows :

Pipelined Burst SRAM L2 with 512K & 8-bit Tag RAM (64M cacheable region)



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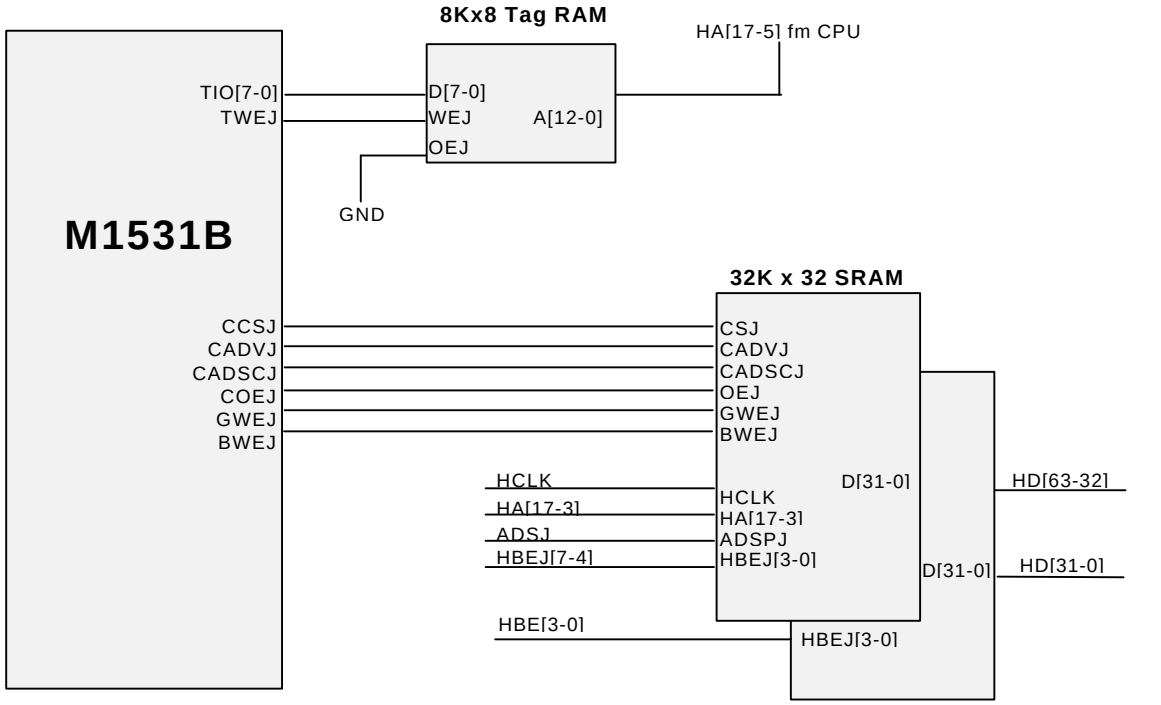
Pipelined Burst SRAM L2 with 256K & 8-bit Tag RAM (64M cacheable region)



3.5 SYSTEM MEMORY TIMING/CONFIGURATION

The DRAM controller of the M1531B supports a variety of DRAM types and improves the first data transaction performance by using a speculative cycle to shorten the latency. Basically, it supports a 32/64-bit memory bus for 8 banks of single-sided SIMMs or 4 banks of double sided SIMMs, and also supports the 64-bit memory bus for 6 banks of single-sided DIMMs or 3 banks of double sided DIMMs. For the best system upgrade ability, ALADDIN IV supports six single-sided 32-bit populated DRAM banks or three double-sided 32-bit populated DRAM banks. The system memory can be easily configured to 12MB by using the most popular 16-Mbit memory types. In this configuration, one bank is 64-bit 8MB, and the other bank is 32-bit 4MB. In the upgrade path, all banks can be extended to 64-bit memory. M1531B also supports the most flexible 32-bit memory population, it supports low DWORD and high DWORD population.

The controller can handle 8 banks of single-sided or 4 banks of double-sided 64-bit memory, with the memory size ranging from 2MB to 1GB. It also supports a programmable driving capability of MA/RAS/CAS/WE to optimize the access timing and the system cost in certain system memory configurations. MA[0-1] are duplicated to gain the burst timing design of the system. Both the EDO and FPM are supported with an optimized timing to support the possible cacheless systems in low end market segments. The SDRAM features are also configured in this chip. M1531B supports a high performance SDRAM controller to push the new DRAM performance to the high edge. M1531B also enhances the DRAM page miss access timing for multithreading and multitasking application. For the best DRAM performance, M1531B has integrated a 16-QWORD deep merging DRAM write buffer. The deep buffer can post the CPU write data and also the PCI master write data and do byte merge to relief the DRAM bus access.

As to the System Management RAM (SMRAM), the M1531B allows several optional noncacheable spaces to map the SMRAM which includes regions such as 38000h-3FFFFh to B page, A/B region to A/B page and D page to B region.

3.5.1 Memory Type supported

Table 3-1. Memory Structure Supported for FPM/EDO

Memory Structure	Address mode	Address size	Memory Structure	Address mode	Address size
4Mbits			2Mx8	Asymmetric	11x10
512Kx8	Asymmetric	10x9	4Mx4	Symmetric	11x11
1Mx4	Symmetric	10x10	4Mx4	Asymmetric	12x10
16Mbits			64Mbits		
1Mx16	Asymmetric	12x8	4Mx16	Symmetric	11x11
1Mx16	Symmetric	10x10	8Mx8	Asymmetric	12x11
2Mx8	Asymmetric	12x9	16Mx4	Symmetric	12x12

Memory Structure	Address size	Bank size
16Mbits SDRAM		
2x2Mx4	11x10	32MB
2x1Mx8	11x9	16MB
2x512Kx16	11x8	8MB
64Mbits SDRAM		
2x8Mx4	13x10	128MB
2x4Mx8	13x9	64MB
2x2Mx16	13x8	32MB
2x2Mx16	11x10	32MB
2x1Mx32	11x9	16MB
2x512Kx64	11x8	8MB
2x1Mx32	12x8	16MB
4x4Mx4	12x10	128MB
4x2Mx8	12x9	64MB
4x1Mx16	12x8	32MB
4x2Mx8	11x10	64MB
4x1Mx16	11x9	32MB
4x512Kx32	11x8	16MB

3.5.2 MA Mapping Table Supported

In the following table, ALADDIN-IV supports a versatile memory MA mapping table to accommodate many different approaches of DRAM populated banks. Furthermore, it supports the 32-bit memory bus on each possible available bank.

Table 3-2. Several DRAM Address translation supported for some specific purpose
Normal FPM/EDO DRAM Address Translation Table

MA[11:0]	11	10	9	8	7	6	5	4	3	2	1	0
Row	A24/25	A23	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12
Column	A26	A24	A22	A11	A10	A9	A8	A7	A6	A5	A4	A3

Row MA[11] : If 64Mbits DRAM is not populated, then A24 is driven; if 64Mbits DRAM is populated, then A25 is driven

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1M x 16, 2M x 8 FPM/EDO DRAM Address Translation Table

Specific DRAM Address Translation Table for Asymmetric 1M x 16

MA[11:0]	11	10	9	8	7	6	5	4	3	2	1	0
Row	A22	A21	A11	A20	A19	A18	A17	A16	A15	A14	A13	A12
Column				A23	A10	A9	A8	A7	A6	A5	A4	A3

Address Size = 12 x 8, 12 x 9

32-bit bank FPM/EDO DRAM Address Translation Table

MA[11:0]	11	10	9	8	7	6	5	4	3	2	1	0
Row	A23/A24	A22	A11	A20	A19	A18	A17	A16	A15	A14	A13	A12
Column	A25	A23	A21	A4	A10	A9	A8	A7	A6	A5	(A2)	A3

Row MA[11] : if 64Mbits DRAM is not populated, then A23 is driven; if 64Mbits DRAM is populated, then A24 is driven

32-bit Bank 1M x 16, 2M x 8 FPM/EDO DRAM Address Translation Table

MA[11:0]	11	10	9	8	7	6	5	4	3	2	1	0
Row	A10	A21	A11	A20	A19	A18	A17	A16	A15	A14	A13	A12
Column				A22	A4	A9	A8	A7	A6	A5	(A2)	A3

Address Size = 12 x 8, 12 x 9

64MB SDRAM MA mapping table (2-bank: 13*10,13*9, 13*8, 12*8) (4-bank: 12*10,12*9,12*8)

MA[11:0]	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Row	A23	A24	A11	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12
Column	A23	A24	A11	L	A26	A25	A10	A9	A8	A7	A6	A5	A4	A3

64MB SDRAM MA mapping table (4-bank: 11*10,11*9,11*8)

MA[11:0]	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Row	X	A23	A11	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12
Column	X	A23	A11	L	A25	A24	A10	A9	A8	A7	A6	A5	A4	A3

16MB SDRAM MA mapping table (2-bank: 11*10,11*9, 11*8) 64MB MA mapping table (2-bank: 12*10,12*9,12*8)

MA[11:0]	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Row	x	x	A11	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12
Column	x	x	A11	L	A24	A23	A10	A9	A8	A7	A6	A5	A4	A3

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3.5.3 Outstanding DRAM timing

The following table shows the timing of EDO/FPM DRAMs :

Table 3-3. Lead time of first data transaction, check time at T2

r.lead	w.lead	ras.prch	t.lead(t2)	sle. lead	ras-cas	read.. hit	wr..hit	r.row . mis	r.pg. mis	w.rtr. row.m	w.rtr.pg. ms
6	5	3	-1	-1	3	4	5	7	10	8	11
6	5	3	-1	-1	2	4	5	6	9	7	10
6	5	4	-1	-1	3	4	5	7	11	8	12
6	5	4	-1	-1	2	4	5	6	10	7	11
6	5	3	-1	0	3	5	5	8	11	8	11
6	5	3	-1	0	2	5	5	7	10	7	10
6	5	4	-1	0	3	5	5	8	12	8	12
6	5	4	-1	0	2	5	5	7	11	7	11

Note : r.lead means "read lead off cycle" w.lead means "write lead off cycle"
ras.prch means "RAS precharge time", and is controlled by Index -44h bit2.
t.lead (t2) means "Hit/Miss check point", and is controlled by Index-40h bit0.
sle.lead means "Read Speculative Leadoff", and is controlled by Index-45h bit5.
ras-cas means "RAS to CAS delay", and is controlled by Index-44h bit3.
read hit means "read hit lead off cycle"
write hit means "write hit lead off cycle"
r.row.mis means "read row miss lead off cycle"
r.pg.mis means "read page miss lead off cycle"
w.rtr.rw.m means "write buffer retired write row miss cycle"
w.rtr.pg.ms means "write buffer retired write page miss cycle"

Table 3-4. CPU to DRAM read performance Summary for BEDO/EDO/FPM DRAMs

DRAM speed	DRAM type	Performance (in Host CLK)				
Read (Burst rate)		50 MHz	60 MHz	66 MHz	75 MHz	83 MHz
50 ns	EDO	x-222	x-222	x-222	x-222	x-333
	FPM	x-333	x-333	x-333	x-333	x-333
60 ns	EDO	x-222	x-222	x-222	x-222	x-333
	FPM	x-333	x-333	x-333	x-333	x-444
70 ns	EDO	x-333	x-333	x-333	x-333	x-333
	FPM	x-333	x-444	x-444	x-444	x-444

Page hit		50/60 MHz	66 MHz	75/83 MHz
60 ns	EDO/FPM	4	5	6
Row Miss				
60 ns	EDO/FPM	6	7	8
Page Miss				
60 ns	EDO/FPM	9	10	11

Back-to-back Burst Reads with Page hit		50/60 MHz	66 MHz	75 MHz	83 MHz
60 ns	EDO	4-222-2222	5-222-2222	5-222-2222	6-333-3333
60 ns	FPM	4-333-3333	5-333-3333	6-333-4333	6-444-4444

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Table 3-5. CPU to DRAM Write Performance Summary

DRAM speed	DRAM type	Performance (in Host CLK)		
Posted Single Write with Write Buffer Empty		50 MHz	60/66 MHz	75/83 MHz
60 ns	EDO/FPM	3.3.3	3.3.3	3.3.3

Posted Burst Write with Write Buffer Empty		50 MHz	60/66 MHz	75/83 MHz
60 ns	EDO/FPM	3-111	3-111	3-111

Single Retire Hit		50/60 MHz	66 MHz	75/83 MHz
60 ns	EDO	2	2	2
60 ns	FPM	2	3	3

Single Retire Row Miss with RAS-CAS = 2T		50/60 MHz	66 MHz	75/83 MHz
60 ns	EDO	4	4	4
60 ns	FPM	4	5	5

Single Retire Page Miss with RAS-CAS = 2T		50/60 MHz	60/66 MHz	75/83 MHz
60 ns	EDO	7	7	7
60 ns	FPM	7	8	8

Retire Burst		50/60 MHz	66 MHz	75/83 MHz
60 ns	EDO	x-222	x-222	x-222
60 ns	FPM	x-222	x-333	x-333

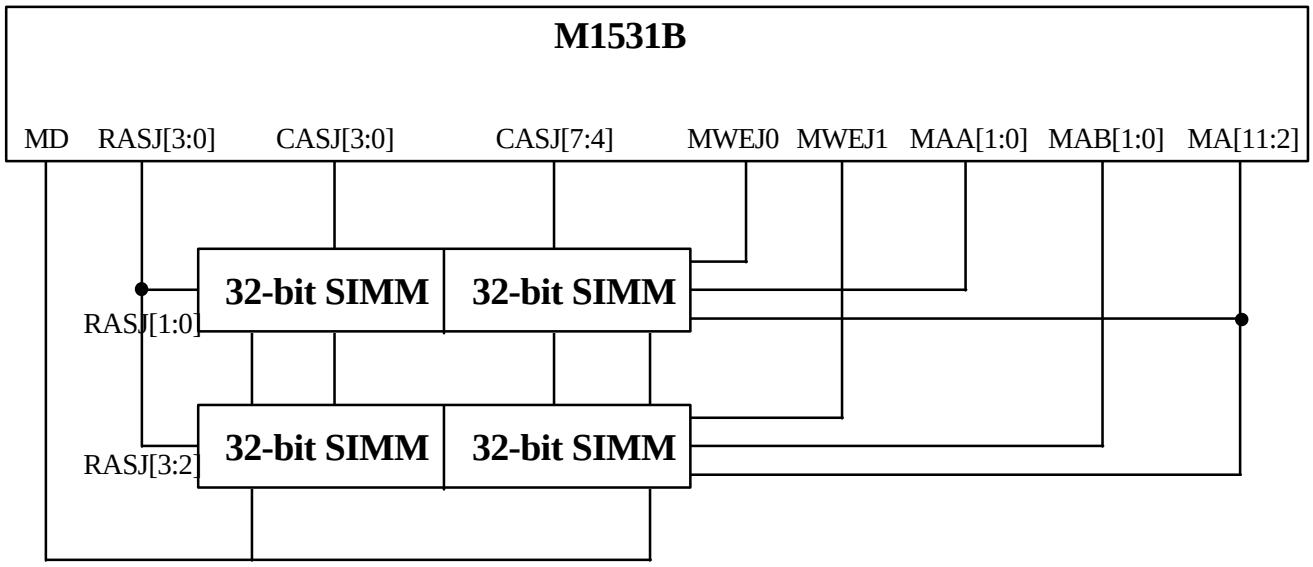
Table 3-6. SDRAM Performance Summary

Cycle Type	83/75/66 MHz		60 MHz		50 MHz	
CAS Latency	CL=3	CL=2	CL=3	CL=2	CL=3	CL=2
Burst Read Page Hit	7-1-1-1	6-1-1-1	6-1-1-1	5-1-1-1	6-1-1-1	5-1-1-1
Read Bank Miss	10-1-1-1	8-1-1-1	10-1-1-1	8-1-1-1	10-1-1-1	8-1-1-1
Read Page Miss	13-1-1-1	10-1-1-1	13-1-1-1	10-1-1-1	13-1-1-1	10-1-1-1
Back-to-back Burst Read Page Hit	7-1-1-1-2-1-1-1	6-1-1-1-2-1-1-1	6-1-1-1-2-1-1-1	5-1-1-1-2-1-1-1	6-1-1-1-2-1-1-1	5-1-1-1-2-1-1-1
Write Page Hit	3	3	3	3	3	3
Write Row Miss	6	5	6	5	6	5
Write Page Miss	9	7	9	7	9	7
Posted Write	3-1-1-1	3-1-1-1	3-1-1-1	3-1-1-1	3-1-1-1	3-1-1-1
Write Retire rate from Posted Write Buffer	-1-1-1	-1-1-1	-1-1-1	-1-1-1	-1-1-1	-1-1-1

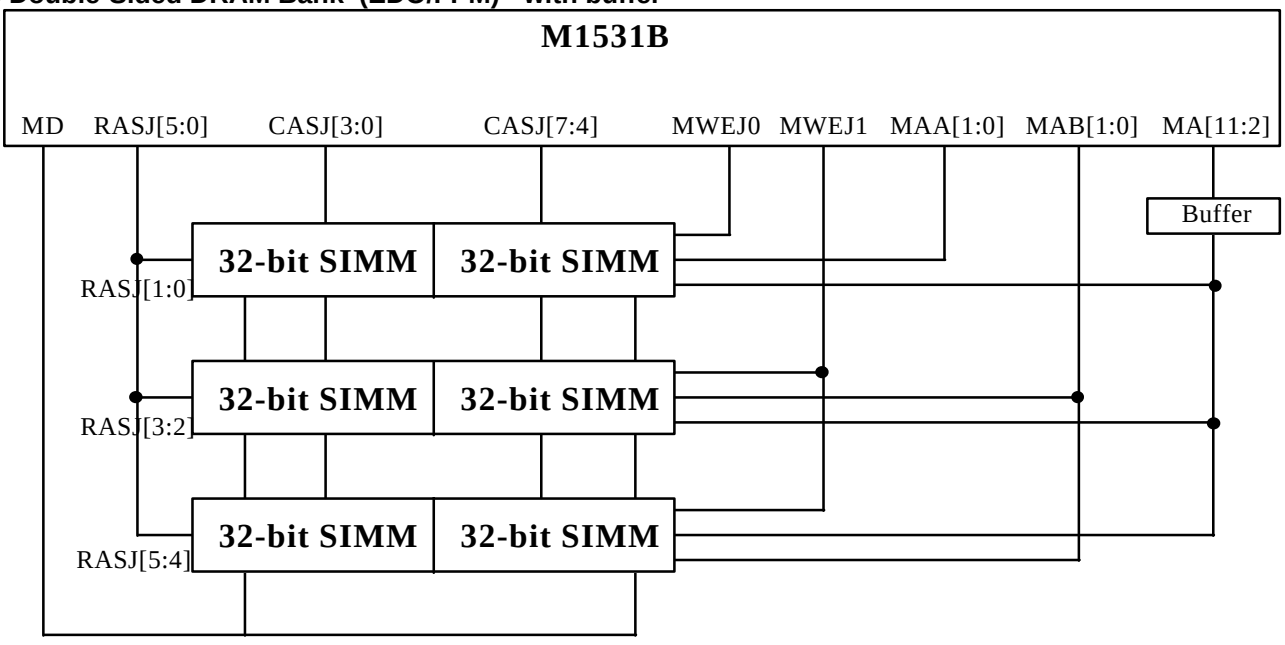
3.5.4 EDO/FPM/(BEDO) DRAM Configuration

ALADDIN-IV supports 8 banks of single sided SIMMs or 4 banks of double sided SIMMs maximum so that any mentioned combination can be fully supported. The following diagram shows some possible applications.

2 Double-Sided DRAM Bank (EDO/FPM)



3 Double-Sided DRAM Bank (EDO/FPM) - with buffer



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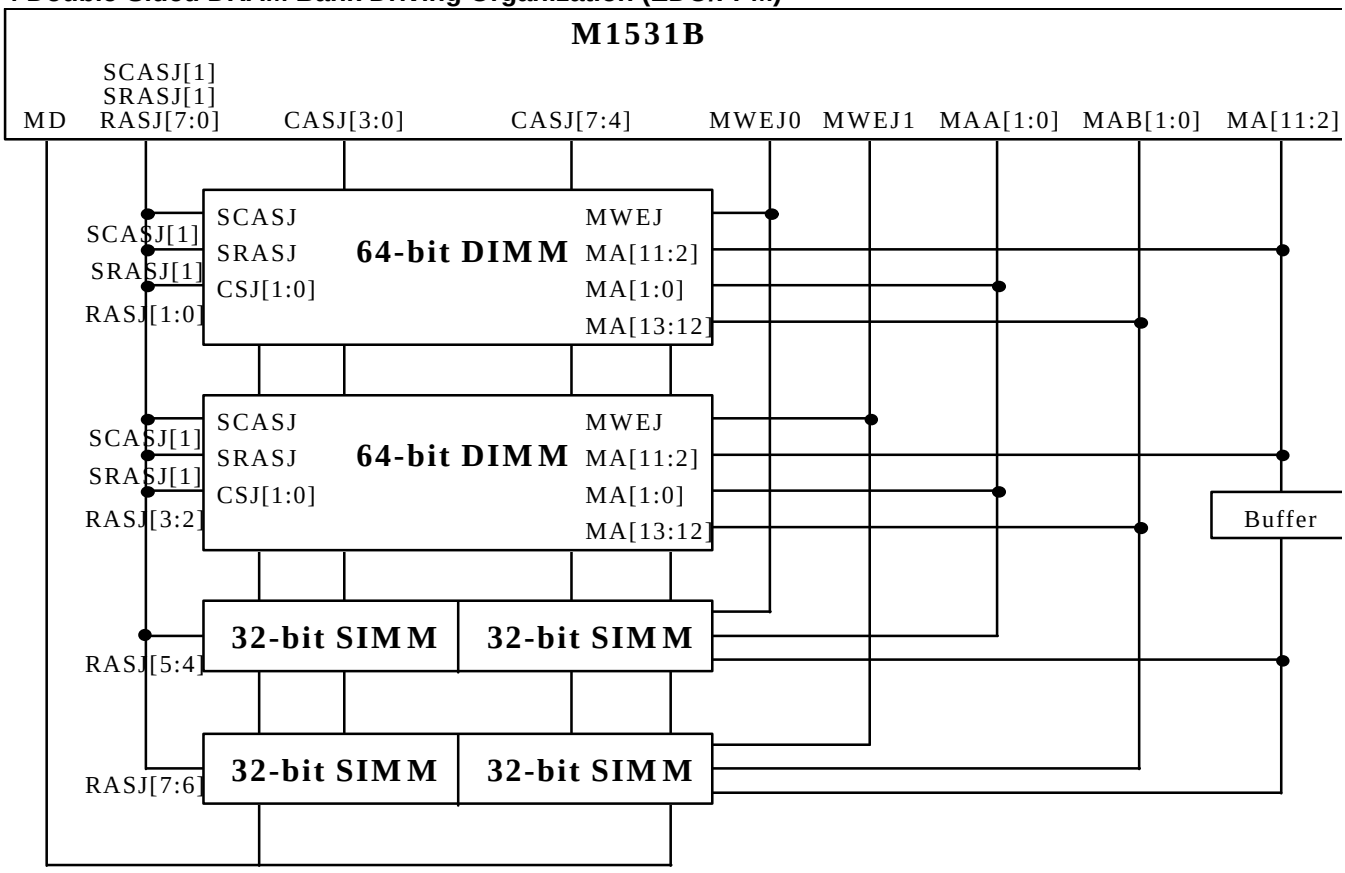
4 Double-Sided DRAM Bank Driving Organization (EDO/FPM)



2 Double-Sided DRAM Bank (EDO/FPM) +
2 Double-Sided SDRAM Bank

3.5.5 SDRAM Support

Aladdin IV supports the most popular synchronous DRAM (SDRAM) at sizes of 1M*16, 2M*8, and 4M*4 with extra performance and flexibility. Interleaved and linear wrap type for both CAS latency 2 and 3 with burst length 4 are supported. Users are permitted to use pure SDRAM up to 6 banks single sided or 3 banks of double sided, or mix with FPM/EDO DRAM on a row-by-row basis without any constraint. Furthermore, M1531B supports SDRAM Speculative Read and Enhanced Page mode which not only minimizes the effect of CAS latency (CL) and RAS Precharge time (Trp) but also largely enhances the overall performance of the system. JEDEC standard for SDRAM including 2n rule are supported too. Note that M1531B does not support the 32-bit SDRAM population.

ALADDIN-IV utilizes SDRAM commands that support both SDRAM and PC SDRAM. The commands are :

- Mode Register Set (MRS)
- CAS-Before-RAS Refresh (CBR)
- Self-Refresh (SEFR)
- Precharge All Banks (PALL)
- Precharge Selected Bank (PRCH)
- Row Active (RACT)
- Write (WRITE)
- Read (READ)
- No Operation (NOP)
- Device Deselect (DESL)

The following Table shows the command truth table M1531B supports.

Table 3-7. Command Truth Table

Function	Symbol	CKE	CSJ	SRASJ	SCASJ	WEJ	A11-(BA)	A10-(AP)	A[9:8]	A[7:0]
Mode Register Set	MRS	H *1	L	L	L	L	L	L	L	V *2
Self-Refresh	SEFR	L	L	L	L	H	L	L	L	L
Precharge All Banks	PALL	H	L	L	H	L	K	H	K	K
Precharge Selected Bank	PRCH	H	L	L	H	L	V *3	L	K	K
Row Active	RACT	H	L	L	H	H	V *4	V *4	V *4	V *4
Write	WRITE	H	L	H	L	L	V *3	L	V *5	V *5
Read	READ	H	L	H	L	H	V *3	L	V *5	V *5
No Operation	NOP	H	L	H	H	H	K	K	K	K
Device Deselect	DESL	H	H	H	H	H	K	K	K	K
CAS-before-RAS	CBR	H	L	L	L	H	K	K	K	K

Notes :

1. V = Valid, L = Logic Low, H = Logic High. K = Keep the value in previous cycle.
2. Please refer to Table 3-8.
3. A11 = 0 to select bank 0. A11 = 1 to select bank 1.
4. A[11:0] shows the Row Address.
5. A[9:0] is used as the column address for 4M*4 SDRAM, A[8:0] is used as the column address for 2M*8 SDRAM, A[7:0] is used as the column address for 1M*16 SDRAM.

In terms of Wrap Type of SDRAM, ALADDIN-IV supports both Interleave mode and Linear (Sequential) mode. The following table shows the Mode Register Set Table supported by M1531B.

Table 3-8. Mode Register Set

A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	ADDRESS
0	0	0	0	0	CAS Latency			Burst Type	Burst Length			Mode Register

A6	A5	A4	CAS Latency	Index-5Ch bit4
0	1	0	2	1
0	1	1	3	0

A3	Burst Type	Description
0	Sequential	for M1/M2 Linear Wrap Mode
1	Interleave	for P54C/P55C/K5/K6 Interleave mode

A2	A1	A0	Burst Length
0	1	0	4
Others			Not Support

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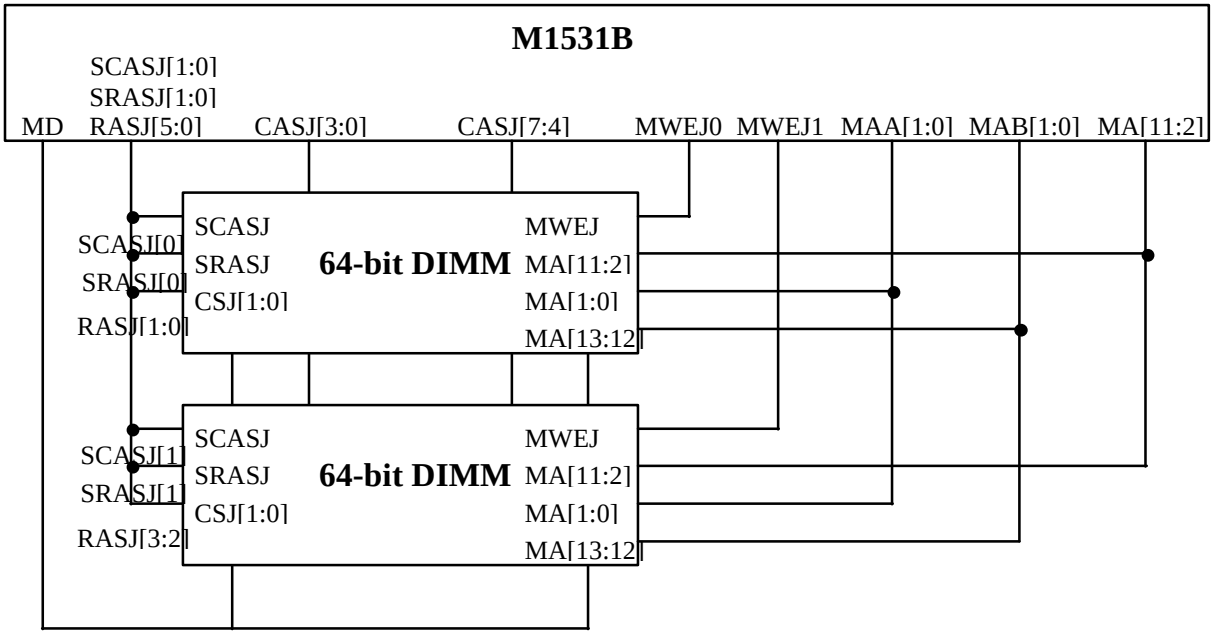
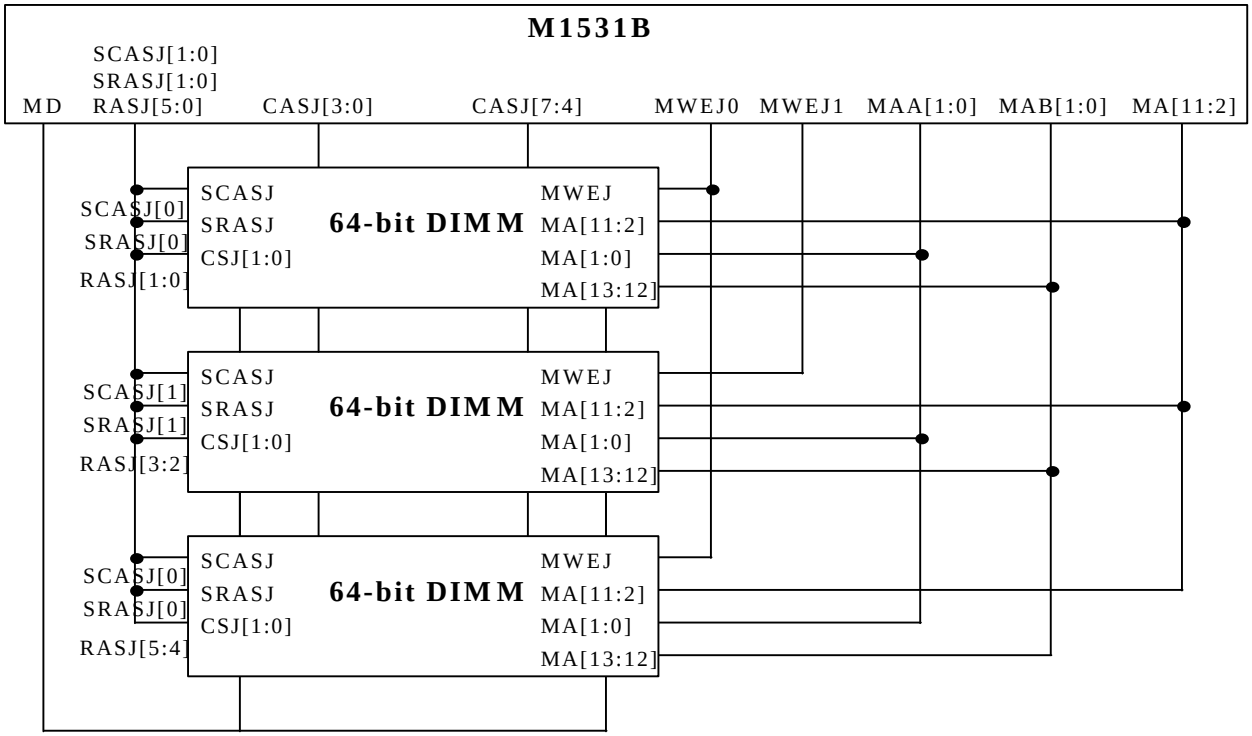
ALADDIN-IV supports two sets of SDRAM control signals. Following figures show the topological configuration when supporting SDRAM. The first figure below illustrates 4-bank single-sided or 2-bank double sided support of SDRAM. The following figure shows 6-bank support of SDRAM. Please refer to Table 3-5 for the source of SRASJ[1:0], SCASJ[1:0] and MWEJ[1:0].





3.5.6 Signal Assignment of DRAM interface

As several DRAM architectures are supported, the signal of each configuration have to be multiplexed to optimize the pinout. Shown here is the signal assignment for each configuration and is controlled by Index-41h bit6, bit3, and bit0. In the following table, MWEJ[1] will become MKREFRQJ when Memory Cache has been used (Index-41h bit6 = 0).

Table 3-9. Signal Assignment of Versatile DRAM Architecture

		without buffer	with buffer		w/o buffer
EDO/Cache/8BK	**4-bank**	**6-bank**	**6-bank**	**4 SDRAM bank**	**6 SDRAM bank**
TAG[7:0]	TAG[7:0]	TAG[7:0]	TAG[7:0]	TAG[7:0]	TAG[7:0]
TAG[8]	TAG[8]	TAG[8]	TAG[8]	TAG[8]	TAG[8]
SCASJ[1],SRASJ[1]	SCASJ[1],SRASJ[1]	SCASJ[1],SRASJ[1]	SCASJ[1],SRASJ[1]	SCASJ[1],SRASJ[1]	SCASJ[1],SRASJ[1]
MWEJ[1]	MWEJ[1]	MWEJ[1]	MWEJ[1]	MWEJ[1]	MWEJ[1]
RAS0	RAS0	RAS0	RAS0	SCS0	SCS0
RAS1	RAS1	RAS1	RAS1	SCS1	SCS1
RAS2	RAS2	RAS2	RAS2	SCS2	SCS2
RAS3	RAS3	RAS3	RAS3	SCS3	SCS3
RAS4	TAG[10]	TAG[10]	TAG[10]	TAG[10]	SCS4
RAS5	TAG[9]	TAG[9]	TAG[9]	TAG[9]	SCS5
RAS6	RAS6	RAS6	RAS6	SCAS0	SCAS0
RAS7	RAS7	RAS7	RAS7	SRAS0	SRAS0
CAS[7:0]	CAS[7:0]	CAS[7:0]	CAS[7:0]	DQM[7:0]	DQM[7:0]
MAA[1:0]	MAA[1:0]	MAA[1:0]	MAA[1:0]	MAA[1:0]	MAA[1:0]
MAB[1:0]	MAB[1:0]	MAB[1:0]	MAB[1:0]	MA[13:12]	MA[13:12]
MWEJ[0]	MWEJ[0]	MWEJ[0]	MWEJ[0]	MWEJ[0]	MWEJ[0]

3.5.7 DRAM Load Analysis for each memory configuration and memory type.

The existing versatile/complicated memory configuration, which might result in a big variation of DRAM loading and the control signal timing. ALADDIN-IV is designed to target some large reasonable memory types and number of banks to optimize COST and TIMING. If only 4 banks of single sided DRAM SIMMs or 2 banks of double sided DRAM SIMMs or 6 banks of single sided DRAM DIMMs or 3 banks of double sided DRAM DIMMs are designed in motherboard, M1531B is designed to be TTL free for the DRAM control signals buffer.

3.6 CPU-to-PCI Posted Write Buffer

The M1531B integrates a 6-DWORD CPU-to-PCI posted write buffer to enhance the CPU-to-PCI performance. With this buffer, the M1531B can minimize the latency of CPU-to-PCI write cycles and maximize the concurrency of CPU bus and PCI bus when CPU writes data to PCI bus. The PCI burst write cycles and fast back-to-back cycles for CPU-to-PCI access are also supported by this buffer.

In addition, the M1531B CPU-to-PCI posted write buffer supports data merge, it can improve the CPU-to-PCI non-32 bits access performance.

3.7 PCI MASTER Latency and Throughput Analysis

The M1531B includes a smart PCI-to-DRAM interface, including a smart deep PCI-to-DRAM buffer and the enhanced PCI arbiter. All these components are designed to optimize the system performance and maximize the PCI bus bandwidth.

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3.7.1 Smart Deep Post Write & Prefetch Buffer

The smart deep PCI-to-DRAM buffer of M1531B plays the key role to boost PCI master read/write performance. It consists of 38 DWORDs posted write buffer and 22 DWORDs prefetch buffer.

The 38 DWORDs PCI-to-DRAM posted write buffers enhance the PCI master bandwidth of accessing DRAM. With the implementation of L1/L2 writeback merge and smart buffer management, the M1531B can sustain the ultimate 133-Mbytes/sec bandwidth for PCI master writing to local memory. More significantly, the maximum bandwidth is independent of results from the L1/L2 snooping and writeback cycle, the DRAM types and L2 types.

On the other hand, to optimize the PCI master read performance when accessing DRAM, the M1531B includes 22 DWORDs PCI-to-DRAM read prefetch buffers. With the implementation of L1/L2 writeback and smart buffer management, the M1531B can sustain the ultimate 133 Mbytes/sec bandwidth for PCI Master reading from Local memory. And the maximum bandwidth is independent of results of the L1/L2 snooping, writeback cycle and L2 types.

Considering the performance and concurrency of multi-master systems, for example the MPEG/Multimedia applications, the PCI-to-DRAM read prefetch buffer of M1531B is configured as two independent units. Each unit prefetches and keeps data independently with the other one. With this configuration, the M1531B minimizes the PCI master read latency and reduces the overhead of snooping and prefetching.

3.7.2 PCI 2.1 Compliant

The M1531B is fully compliant to the PCI 2.1 Specification. The M1531B supports Passive Release and programmable latency control timers for the first and subsequent data transaction. With the flexible PCI latency control, it can achieve the best system performance.

3.7.3 Pipelined Snoop Ahead

The M1531B utilizes an enhanced pipelined snoop protocol to minimize the L1 & L2 snoop overhead. While snooping L1 & L2, the M1531B also performs speculative read to DRAM such that the latency of master read cycle can be minimized. It combines with the deep smart read/write buffer to optimize PCI master performance.

3.7.4 PCI Arbiter

The M1531B integrates an enhanced PCI arbiter. It provides a fair arbitration by using a PCI and CPU Time Slice mechanism. The arbitration algorithm is also designed to minimize the snoop overhead. Besides the M1533/M1543 ISA bridge, the M1531B supports up to 5 PCI masters to make the system motherboard design more flexible and engaging.

To balance the bandwidth of ISA masters and PCI masters and utilize the most bandwidth of PCI bus, the M1531B also supports passive release of PCI 2.1 latency requirements, which makes PCI master access possible when ISA master is active. By this way, the Aladdin-IV can target the best system performance and the most concurrency between PCI bus and ISA bus.

3.7.5 ACPI Support

The M1531B provides the scheme to support ACPI relative functions. By means of PM2_BASE_ADDRESS register (Index-70h - Index-71h) and PM2_CONTROL register (Index-72h Bits[1:0]), software can easily enable/disable PCI arbiter as ACPI requirement. In addition, PCIMRQJ signal makes ISA Bridge aware of PCI master bus request to generate SMI/SCI.

3.8 Low Power Features

The ALADDIN-IV supports sophisticated power saving features, called Power On Suspend (Sleeping), Suspend to DRAM (Suspend), and Suspend to Disk. Under Power On Suspend state, the system will turn off the signal event of host and keep the DRAM refresh active through the M1531B's DRAM interface that is triggered by a 32K clock source. After the Power On suspend event is triggered, by programming a bit of M1533/M1543's internal register, the M1533/M1543 will initiate a handshake with the M1531B. During the handshake, the M1533/M1543 will issue STPCLK to the host, stop the system clock generator, pull the I/O output level to leakageless polarity and turn on the SUSPEND REFRESH circuit to sustain the DRAM data. Theoretically, the only power request under the Power On suspend is the circuit of DRAM suspend refresh. M1531B core has two different power planes, one for the Suspend Refresh circuit, the other is for the other circuit except Suspend Refresh circuit. During Suspend to DRAM state, the system designer can shut off the power except the DRAM suspend refresh circuit to save more system power. Under the Suspend to Disk, only the M1533/M1543 resume circuit is powered and get the minimized system power consumption.

The M1531B and the M1533/M1543 are designed with a very sophisticated I/O circuit and to perform the leakage control under the power saving mode, which is very popular in notebook designs.

For desktop designs, the Power On suspend can provide the system a very efficient **STAND-ON** feature that is more demanding in future home PC systems for Microsoft On Now technology OS.

In the M1533/M1543 of ALADDIN-IV, the solution gives a deep green function. Regarding deep PMU for Peripheral device, one might design a dedicated PMU device to accompany the Power On suspend feature to form a very deep power saving system, such as a notebook system.

To leave the power saving mode, ALADDIN-IV provides several internal event detectors or external event detectors. The system will resume in a very careful/dedicated process and protocol to recover the system to original status, same as the status before entering.

3.9 DRAM Refresh

The M1531B provides CAS-before-RAS (CBR) refresh and RAS-only refresh for FPM DRAM, CAS-before-RAS (CBR) refresh and RAS-only refresh and Extended refresh and self refresh for EDO DRAM, and CAS-before-RAS (CBR) refresh and Self refresh for SDRAMs. FPM/EDO refresh methods use "staggered" and "smart refresh" (i.e. refresh is only performed on banks that are populated) algorithm. The DRAM refresh rate can be controlled via the Index 45h Bits[2:0].

3.10 ECC/Parity Algorithm

The M1531B provides an ECC DRAM data integrity feature when Index 49h bit0 is set to '1'. The ECC feature provides single-error correction, double-error detection, and detection of all errors confined to a single nibble (SEC-DEC-S4ED) for DRAM data integrity. But, the ECC algorithm will not be implemented for the 32-bit only DRAM populated banks. The M1531B will generate 8-bit ECC check bits for 64-bit data to DRAM when the ECC feature is enabled and the current DRAM cycle is a write access operation.

If a partial write (less than 64-bit write) event occurs, a read-modified-write operation will be performed by the M1531B. The M1531B will detect all single bit, double-bit errors, and all errors confined to a single nibble when ECC is enabled and a DRAM read cycle is performed. The M1531B also corrects all single-bit errors and the corrected data is then transferred to the requester (CPU or PCI). This corrected data will not be written back to DRAM in the current M1531B version. The ECC error reporting condition and status are defined in Index 49h-4Ah. The ECC errors are latched until cleared by software. The software programmer also can detect 64 from 72-bit wide SIMMs or check ECC circuit operations via the ECC (parity) test mode (Index 49h bit1 set to '1'). The ECC check bits (or parities) can be forced to any value (defined in Index 4Bh) during all DRAM write access cycles in the ECC/Parity test mode. All the DRAM read leadoff latency timings should add 1 HCLKIN when the ECC feature is enabled.

The M1531B also provides another DRAM data integrity feature -- conventional DRAM even parity generation and checking when Index 49h bit0 is set to '0'. The DRAM parity checking error reporting condition and status also are defined in Index 49h-4Ah. The DRAM parity generation and checking feature will also be supported to the 32-bit only DRAM populated banks. The software can differentiate the 64 from 72-bit wide SIMMs or check parity circuit operation via the ECC/Parity test mode. The conventional Parity check will not degrade the system performance.

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Section 4 : Configuration Registers

I. M1531B PCI Mechanism #1 Configuration Cycle Ports

I/O Address **0CF8h**
Register Name : **CFGADR - Configuration Address Register**
Default Value 00000000h
Attribute Read/Write
Size This register must be 32-bit I/O access in PCI configuration access mechanism #1. An 8-bit or 16-bit access will pass through the Configuration Address Register onto the PCI bus.

Bit Number	Bit Function
31 (0)	PCI Configuration Space Access. 0 : Configuration Disable. 1 : Configuration Enable. When this bit is set to 1, accesses to PCI configuration space are enabled, otherwise, accesses to PCI configuration space are disabled.
30-24 (00h)	Reserved.
23-16 (00h)	Bus Number. When the bus number is programmed to 00H, the target of the configuration is directly connected to the M1531B and a type 0 configuration cycle is generated. If the bus number is non-zero, a type 1 configuration cycle is generated on the PCI bus.
15-11 (00h)	Device Number. It is used by M1531B to drive the IDSEL lines that select a specific PCI device during initialization. The IDSEL lines are only driven when Bus Number is 0h. As for the others, the M1531B will send the configuration to a PCI or PCI bridge device.
10-8 (0h)	Function Number. It is used to select a specific device function during initialization.
7-2 (00h)	Register Number. It is used to select a specific register during initialization.
1-0 (0h)	Reserved. Fixed at '00'.

I/O Address **0CFCh**
Register Name : **CFGDAT - Configuration Data Register**
Default Value 00000000h
Attribute Read/Write
Size This register may be 8-bit or 16-bit or 32-bit I/O access in configuration access mechanism #1.
Description This register contains the information which is sent or received during the PCI bus data phase of configuration write or read cycles. CPU access of 8, 16 or 32-bit wide to this register are supported.

Note : M1531B only supports PCI mechanism #1 access.

II. M1531B PCI Configuration Space Mapped Registers

The M1531B will respond to CPU/PCI configuration access for which AD16 is high during the address phase.

Register Index	**01h-00h**
Register Name	**VID - Vendor Identification Register**
Default Value	10B9h
Attribute	Read Only
Size	16 bits
Description	This is a 16-bit value assigned to Acer Labs Inc. This register is combined with index 03h-02h uniquely to identify any PCI device. Write to this register has no effect.

Register Index	**03h-02h**
Register Name	**DID - Device Identification Register**
Default Value	1531h
Attribute	Read Only
Size	16 bits
Description	This is a 16-bit value assigned to the M1531B.

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Register Index **05h-04h**
Register Name : **COM - Command Register**
Default Value 0006h
Attribute Read/Write
Size 16 bits

Bit Number	Bit Function
15-9 (000h)	Reserved.
8 (0)	Enable the SERRJ Output Driver. 0 : Disable. 1 : Enable. SERRJ uses an o/d (Open Drain) pad in M1531B. The motherboard design should use a pull-up resistor (2.2KΩ) to keep this pin logic high. When the DRAM ECC/Parity check or the PCI Parity check is enabled and an error is found, the M1531B will drive SERRJ low to M1533/M1543 to generate NMI when this bit is enabled. Disabling the SERRJ output driver will always keep this output logic high. This bit is reset to 0 and should be set to 1 once memory has been scrubbed by BIOS in systems that wish to report DRAM ECC/Parity error.
7 (0)	Enable Address/Data Stepping. M1531B does not support this feature. Write to this bit has no effect.
6 (0)	Respond to Parity Errors. 0 : Disable. 1 : Enable. The M1531B will do a PCI parity check in CPU to PCI read and PCI to local memory write. This bit is used to enable the parity check. When a parity error is detected, the M1531B will assert SERRJ and set the Parity Error Bit in the DS register.
5 (0)	Enable VGA Palette Snooping. M1531B does not support this feature. Write to this bit has no effect.
4 (0)	Enable Postable Memory Write Command. M1531B does not support this feature. Write to this bit has no effect.
3 (0)	Enable Special Cycle. M1531B does not support this feature. Write to this bit has no effect.
2 (1)	Control to Act As a PCI Bus Master. M1531B does not support to disable bus master operations. This bit is set to 1 during Power-On to enable PCI master operations. Write to this bit has no effect.
1 (1)	Enable Response to Memory Access. M1531B always accepts PCI master accesses to local memory. Write to this bit has no effect.
0 (0)	Enable Response to I/O Access. M1531B does not respond to any PCI master I/O accesses. Write to this bit has no effect.

Register Index : **07h-06h**
Register Name : **DS - Device Status Register**
Default Value : 0400h
Attribute : Read Only, Read/Write Clear
Size : 16 bits

Bit Number	Bit Function
15 (0)	Detected Parity Error. This bit is set by the M1531B whenever it detects a parity error in a PCI transaction even if parity error handling is disabled (as controlled by bit6 in the command register). Software can reset this bit to 0 by writing a 1 to it.
14 (0)	Signalled System Error. The M1531B will set this bit whenever it asserts SERRJ. Software can reset this bit to 0 by writing a 1 to it.
13 (0)	Received Master Abort. This bit is set by M1531B whenever it terminates a transaction with master abort. This bit is cleared by writing a 1 to it.
12 (0)	Received Target Abort. This bit is set by the M1531B whenever its initiated transaction is terminated with a target abort. This bit is cleared by writing a 1 to it.
11 (0)	Send Target Abort. This bit is set by devices that act as a target to terminate a transaction by target abort. The M1531B never terminates a transaction with target abort therefore this bit is never set. A write to this bit has no effect.
10-9 (10)	DEVSELJ Timing. 00 : Fast. 01 : Medium. 10 : Slow. The M1531B timing for DEVSELJ assertion. Slow timing is selected.
8-0 (000h)	Reserved.

Register Index **08h**
Register Name : **RI - Revision ID Register**
Default Value B0h (B0 Stepping)
Attribute Read Only
Size 8 bits
Description This register contains the version number of M1531B. The value 01 means A0 stepping.

Register Index **0Bh-09h**
Register Name : **CC - Class Code Register**
Default Value 060000h
Attribute : Read Only
Size : 24 bits
Description : These registers contain the Class Codes of the M1531B.

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Register Index : **0Dh**
Register Name : **LT - PCI Latency Timer value**
Default Value : 20h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-3 (04h)	Master Latency Timer Count Value. LT is used to control the amount of time the M1531B, as a bus master, can burst data to the PCI Bus. It can be used to guarantee a minimum amount of the system resources.
2-0 (0h)	Reserved. They are assumed to be 0 when determining the Count Value.

Register Index : **2Bh-0Eh**
Register Name : **Reserved Registers**
Default Value : 00h
Attribute : Read Only

Register Index : **2Dh-2Ch**
Register Name : **SVID - Sub-Vendor Identification**
Default Value : 10B9h
Attribute : Lock Read Only
Size : 16 bits
Description : If Index-70h bit3 = 1, then this port can be Read or Write.

Register Index : **2Fh-2Eh**
Register Name : **SDID - Sub-Device Identification**
Default Value : 1531h
Attribute : Lock Read Only
Size : 16 bits
Description : If Index-70h bit3 = 1, then this port can be Read or Write.

Register Index : **3Fh-30h**
Register Name : **Reserved Registers**
Default Value : 00h
Attribute : Read Only

Register Index: **40h**
Register Name : **L2CP - L2 Cache Performance**
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-6 (0h)	TAG8O, RASJ[5:4] as TAG[9:10] feature option 00 : Tag8O are disabled RASJ[5] -> RASJ[5] RASJ[4] -> RASJ[4] 01 : Tag8O are enabled RASJ[5] -> RASJ[5] RASJ[4] -> RASJ[4] 10 : Tag8O are enabled RASJ[5] -> TAG[9] RASJ[4] -> RASJ[4] (Index 41h bit3,bit0 must be '10') 11 : Tag8O are enabled RASJ[5] -> TAG[9] RASJ[4] -> TAG[10] (Index 41h bit3,bit0 must be '10')
5 (0)	Fast NAJ asserted in CPU single write cycle. 0 : Disable. 1 : Enable. This bit controls the NAJ assertion point during CPU single write cycle. When enabled, NAJ will assert at T2 instead of T3 to achieve the best CPU single write performance. Value 1 is recommended during normal operation.
4 (0)	L1 Snoop HITMJ Check Point. 0 : 3rd CPU Clock after asserting EADSJ. 1 : 2nd CPU Clock after asserting EADSJ. This bit controls the HITMJ strobe point during L1 snoop cycle. Value 1 is recommended during normal operation.
3-1 (0h)	Reserved.
0 (0)	Hit/Miss Check Point (L2 Hit/Miss & DRAM Page Hit/Miss). 0 : T3end (3rd CPU Clock after Sampling ADSJ). 1 : T2end (2nd CPU Clock after Sampling ADSJ). This bit controls the cycle checkpoint of L2 & DRAM access. Value 1 is recommended for the CPU bus frequency equal or less than 75 Mhz. In 83.3 Mhz CPU bus frequency configuration, value 0 is recommended for the best system reliability.

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Register Index: **41h**
Register Name : **L2CCI - L2 Cache Configuration-1**
Default Value: Hardware Strobe Value
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7 (0/1)	L2 Cache Bank Select. 0 : 2-bank Pipelined Burst SRAM / Memory Cache. 1 : 1-bank Pipelined Burst SRAM / Memory Cache. The default value is determined by hardware strobe from HA[24]. If the system does not implement the correct hardware strobe, BIOS should program the correct L2 configuration for normal operation after sorting L2 cache.
6 (0/1)	L2 Cache Type Select. 0 : Memory Cache. 1 : Pipelined Burst SRAM. The default value is determined by hardware strobe from HA[23]. The system must implement the correct hardware strobe for Memory Cache use.
5 (0)	Reserved.
4 (0)	Internal MESI Software Test Mode. 0 : Disable. 1 : Enable. This bit can be used to test internal MESI tag bits by software. It must be kept to '0' in normal operation. Please refer to the MESI Software Test Mode Section 5.5.
2-1 (0/1,0/1)	L2 Cache Size. 00 : None. 01 : 256K. 10 : 512K. 11 : 1M. The default value is determined by hardware strobe from HA[22:21]. If the system does not implement the correct hardware strobe, BIOS should program the correct L2 configuration for normal operation after sorting L2 cache.
3,0 (00)	Must be set as ‘10’

The following L2 Cache Table shows the different configurations supported by M1531B.

Configuration		DATA SRAM			TAG SRAM				Note
Index-41h bits[2:1]	Cache size	SIZE	Bank	Addr Lines	Addr Lines	Data Lines	Tag Size	Cacheable DRAM Size	Index-40h bits 7,6
01	256K	(32K32)*2	1	A3-A17	A5-A17	A18-A25	8K8	64M	00
10	512K	(64K16)*4	1	A3-A18	A5-A18	A19-A25	16K8	64M	00
10	512K	(32K32)*4	2	A3-A18	A5-A18	A19-A25	16K8	64M	00
11	1M	(64K32)*4	2	A3-A19	A5-A19	A20-A25	32K8	64M	00
01	256K	(32K32)*2	1	A3-A17	A5-A17	A18-A26	8K9	128M	01
10	512K	(64K16)*4	1	A3-A18	A5-A18	A19-A26	16K9	128M	01
10	512K	(32K32)*4	2	A3-A18	A5-A18	A19-A26	16K9	128M	01
11	1M	(64K32)*4	2	A3-A19	A5-A19	A20-A26	32K9	128M	01
01	256K	(32K32)*2	1	A3-A17	A5-A17	A18-A27	8K10	256M	10
10	512K	(64K16)*4	1	A3-A18	A5-A18	A19-A27	16K10	256M	10
10	512K	(32K32)*4	2	A3-A18	A5-A18	A19-A27	16K10	256M	10
11	1M	(64K32)*4	2	A3-A19	A5-A19	A20-A27	32K10	256M	10
01	256K	(32K32)*2	1	A3-A17	A5-A17	A18-A28	8K11	512M	11
10	512K	(64K16)*4	1	A3-A18	A5-A18	A19-A28	16K11	512M	11
10	512K	(32K32)*4	2	A3-A18	A5-A18	A19-A28	16K11	512M	11
11	1M	(64K32)*4	2	A3-A19	A5-A19	A20-A28	32K11	512M	11

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Register Index: **42h**
Register Name : **L2CCII - L2 Cache Configuration-2**
Default Value: 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7 (0)	L2 TAG Output Delay. 0 : Disable. 1 : Enable. This bit is used to increase L2 Tag data hold time when M1531B wants to update the L2 Tag content. The M1531B will delay the Tag data output floating timing by one half CPU clock when this bit is enabled. A '1' is recommended in normal operation.
6 (0)	CPU Single Read Cycle L2 Cache Allocation. 0 : Disable. 1 : Enable. When this bit is disabled, the M1531B will only do the L2 Cache allocation after it decodes the CPU burst line-fill cycle. The CPU single read cycle will start a DRAM single read cycle if this cycle is a DRAM cycle and not hit the L2 Cache. When this bit is enabled, the M1531B will also do the L2 Cache allocation after it decodes the CPU single read cycle. The M1531B will issue the AHOLD to hold CPU cycle, start a burst DRAM read cycle to get the whole line data, write the date to the L2 Cache, and then de-assert AHOLD and return the BRDYJ to CPU. This feature is used to increase the L2 hit rate when CPU issues the single cycle instead of the line-fill cycle in some special application. A '1' is recommended in normal operation.
5 (0)	Cacheability of Address Region from A0000h to BFFFFh. 0 : Disable. 1 : Enable. This bit is used to enable the cacheability of address region from A0000h to BFFFFh if this region is programmed as local memory (Index-47h bit3 = 1). If Index-47h bit3 = 0, this bit must be 0.
4 (0)	L2 Dirty Bit Setting. 0 : Normal. 1 : Force Non-dirty (Dirty Bit =0). When this bit is set to 1, all tag lookups will ignore the tag dirty bit and force non-dirty. This bit is used to initialize L2 cache. Please refer to the hardware and software setup section.
3 (0)	Reserved.
2 (0)	L2 Cache Miss or Invalidate. 0 : Normal. 1 : Force L2 Cache Miss or Invalidate. When this bit is set to 1, all tag lookups result in a miss. This bit is used to initialize L2 cache. Please refer to the hardware and software setup section.
1 (0)	L2 Dirty Bit Setting. 0 : Normal. 1 : Force Dirty (Dirty Bit =1). When this bit is set to 1, all tag lookups will ignore the tag dirty bit and force dirty. This bit can be used to flush L2 cache in green application. Software can set this bit and then read all L2 cache tag address to flush the cache.
0 (0)	L2 Cache ON/OFF. 0 : Disable External Cache. 1 : Enable External Cache. This bit is used to disable or enable L2 cache.

Register Index : **43h**
Register Name : **L1CDBC - L1 Cache/DRAM Buffer Control**
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7 (0)	Row 5 (RAS5J) Populated with 32-bit DRAM. 0 : Disable. 1 : Enable. The M1531B supports 32-bit DRAM access. BIOS should program this bit to the correct configuration after DRAM sizing for normal operation.
6 (0)	Row 4 (RAS4J) Populated with 32-bit DRAM. 0 : Disable. 1 : Enable. The M1531B supports 32-bit DRAM access. BIOS should program this bit to the correct configuration after DRAM sizing for normal operation.
5 (0)	Row 3 (RAS3J) Populated with 32-bit DRAM. 0 : Disable. 1 : Enable. The M1531B supports 32-bit DRAM access. BIOS should program this bit to the correct configuration after DRAM sizing for normal operation.
4 (0)	Row 2 (RAS2J) Populated with 32-bit DRAM. 0 : Disable. 1 : Enable. The M1531B supports 32-bit DRAM access. BIOS should program this bit to the correct configuration after DRAM sizing for normal operation.
3 (0)	Row 1 (RAS1J) Populated with 32-bit DRAM. 0 : Disable. 1 : Enable. The M1531B supports 32-bit DRAM access. BIOS should program this bit to the correct configuration after DRAM sizing for normal operation.
2 (0)	Row 0 (RAS0J) Populated with 32-bit DRAM. 0 : Disable. 1 : Enable. The M1531B supports 32-bit DRAM access. BIOS should program this bit to the correct configuration after DRAM sizing for normal operation.
1 (0)	Supports DRAM Posted Write Buffer Read-Around-Write Cycle. 0 : Disable. 1 : Enable. This bit is used to control buffer for back-to-back CPU write and read cycles. Since the M1531B implements the DRAM write buffer to post CPU write cycles, the M1531B will do the read first and then flush the DRAM write buffer if this feature is enabled and the required data of the read cycle do not reside in the buffer. When this bit is disabled, the M1531B will flush the DRAM write buffer data first, and then do the CPU read cycle. A '1' is recommended for normal operation.
0 (0)	L1 Cache ON/OFF. 0 : Disable Internal Cache. 1 : Enable Internal Cache This bit is used to disable or enable L1 cache. When this bit is reset to 0, the M1531B will negate KENJ to prevent either L1 or L2 line fill. When this bit is set to '1', the M1531B will assert KENJ for cacheable memory cycles.

Register Index : **44h**
Register Name : **DTCI - DRAM Timing Configuration - 1**
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-6 (00)	EDO Detection Timer. 00 : 128 CPU Clocks. 01 : 256 CPU Clocks. 10 : 512 CPU Clocks. 11 : 1024 CPU Clocks. These two bits combined with bit 5 are used to do the EDO detection.
5 (0)	EDO Detection Mode. 0 : Disable. 1 : Enable. For the EDO detection procedure, please refer to the DRAM type detection figure in the Hardware and Software programming section.
4 (0)	EDO Page mode DRAM Read Timing. 0 : X-3-3-3. 1 : X-2-2-2. This bit is used to control EDO DRAM read timing. Please refer to lead off table in Section 3.5.3 to check the X value.
3 (0)	RAS-to-CAS Delay Time. 0 : 3T. 1 : 2T. This bit controls the RASJ to CASJ delay. T is the CPU clock cycle.
2 (0)	RAS Pre-charge Period. 0 : 4T, and Refresh RAS Assertion 5T. 1 : 3T, and Refresh RAS Assertion 4T. This bit controls the RASJ pre-charge high time in row miss and refresh cycle. T is the CPU clock cycle.
1 (0)	Page Mode DRAM Read Timing. 0 : X-4-4-4 (CASJ : 1H+3L). 1 : X-3-3-3 (CASJ : 1H+2L). This bit is used to control the Page Mode DRAM read timing. Please refer to lead off table in Section 3.5.3 to check the X value.
0 (0)	EDO or Page Mode DRAM Write Timing. 0 : X-3-3-3. 1 : X-2-2-2. This bit is used to control the EDO or Page Mode DRAM write timing. Please refer to lead off table in Section 3.5.3 to check the X value.

Register Index : **45h**
Register Name : **DTCII - DRAM Timing Configuration -2**
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7 (0)	Enhanced DRAM Paging Feature. 0 : Disable. 1 : Enable. When this bit is enabled, the M1531B will use additional information to close the DRAM page in advance. That is, during DRAM irrelevant cycles, an intelligent guess is done to de-assert the RASJ lines and pre-charge them for later use. This bit is recommended to be set '1' in normal operation to enhance DRAM performance.
6 (0)	DRAM Bank Miss Detection. 0 : Disable 1 : Enable When this bit is enabled, the M1531B enhances the DRAM bank-miss performance. This bit is recommended to be set '1' during normal operation to enhance DRAM performance.
5 (0)	Read Speculative Leadoff Enable. 0 : Disable. 1 : Enable (CASJ Pre-asserted in T2 when Memory Read). This bit is valid only if index-40h bit 0 ='1'. When set to '1', the DRAM controller read request is presented 1 CPU clock earlier than it normally is, before the final memory target has been decoded. If the memory cycle does not actually target DRAM, the DRAM state machine will terminate and return back its previous state.
4 (0)	Refresh Mode. 0 : CAS-before-RAS Mode. 1 : RAS-only Mode. This bit is used to control DRAM refresh mode. In suspend mode, only the CAS-before-RAS mode is supported to save power consumption.
3 (0)	CPU/PCI Master to DRAM Page Mode. 0 : DRAM use Page Mode. 1 : DRAM use Non-page Mode. When this bit is set to '1', the M1531B will close the DRAM page after DRAM access. Otherwise, it will keep DRAM page open until next access.
2-0 (0h)	Refresh period. 000 : 1024 CPU Clocks (15 us in 66Mhz). 001 : 2048 CPU Clocks (30 us in 66Mhz). 010 : 4096 CPU Clocks (60 us in 66Mhz). 011 : 8192 CPU Clocks (120 us in 66Mhz). 100 : 16384 CPU Clocks (256 us in 66Mhz). These three bits are used to control the period to refresh DRAMs.

Register Index : **46h**
Register Name : **PIPEF - Pipe Function**
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-6 (00)	RASJ de-asserted in CPU Bus Idle. 00 : after 2 CPU Clocks. 01 : after 4 CPU Clocks. 10 : after 6 CPU Clocks. 11 : after 8 CPU Clocks. These two bits are used to enhance the DRAM Page Miss performance. M1531B will de-assert the RASJ after programmed number of CPU Clocks. This function is enabled when Index-45h bit7 = 1.
5 (0)	Supports Dynamic Write-Back for Burst Writes. 0 : Disable. 1 : Enable. This feature is used to optimize DRAM buffer usage. When CPU issues a burst write cycle and hits to the L2 Cache, the burst data will write to L2 cache and also the DRAM Posted Write Buffer if the feature is enabled and the buffer is not full. It can keep L2 cache clean to speed up later L2 cache accesses. If this feature is disabled, the CPU hit L2 Cache burst write cycle will directly write to L2 Cache and make the hit line as dirty in L2 Tag.
4 (0)	Supports Dynamic Write-Back for Single Write. 0 : Disable. 1 : Enable. This feature is used to optimize DRAM buffer usage. When CPU issues a single write cycle and hits to the L2 Cache, the single data will write to L2 cache and also the DRAM Posted Write Buffer if the feature is enabled and the buffer is not full. It can keep L2 cache clean to speed up later L2 cache accesses. If this feature is disabled, the CPU hit L2 Cache single write cycle will directly write to L2 Cache and make the hit line as dirty in L2 Tag.
3 (0)	Fast DRAM Line Fill in L2 Write Back. 0 : Disable. 1 : Enable. When CPU issues a line fill cycle, the M1531B will decode this cycle at the cycle check point (defined by Index-40h bit 0). If the cycle address is L2 Cache miss, the M1531B will issue a DRAM burst read cycle and write the data to L2 Cache and return the data to CPU at the same time. If the replaced line is dirty, the M1531B also needs to write back the L2 data to DRAM buffer. This bit is used to control the sequence when this condition happens. When this bit is disabled, the M1531B will first write back the dirty L2 data to DRAM buffer, and then start the DRAM state machine to read the burst data to CPU and also write the L2 Cache. If this bit is enabled, the M1531B will write back the dirty data and start the state machine concurrently. The M1531B will intelligently control the state machine to reduce the wait state when this kind of system behavior happens.
2 (0)	DRAM Pipelined Function Option. 0 : Disable. 1 : Enable. This bit is used to enable the assertion of NAJ when the cycle is a DRAM access cycle. When this bit is disabled, the M1531B will not assert NAJ during DRAM access.
1 (0)	L2 Pipelined Function Option. 0 : Disable. 1 : Enable. This bit is used to enable the assertion of NAJ when the cycle is an L2 access cycle. When this bit is disabled, the M1531B will not assert NAJ during L2 access.
0 (0)	Flush DRAM Buffer in CPU Bus Idle. 0 : Disable. 1 : Enable. This bit is used to enable the DRAM buffer flush when CPU bus is idle. M1531B will flush the DRAM buffer when the CPU bus is idle.

Register Index : **47h**
Register Name : **MISI - Miscellaneous-1**
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7 (0)	Supports Cyrix M1/M2 "1+4" Burst Mode & K6 Write Allocation Feature. 0 : Disable. 1 : Enable. This bit is used to support the Cyrix M1/M2 "1+4" mode to toggle cache address, DRAM Memory address, and issues the correct KENJ disregarding CPU CACHEJ if it is a local memory cycle. This bit is also used to support K6 Write Allocation Feature. If this bit is enabled, M1531B will assert KENJ during CPU single local memory write cycle.
6 (0)	Supports M1/M2 Linear Burst Order. 0 : Disable. 1 : Enable. This bit is used to support the Cyrix M1/M2 linear burst mode to toggle cache address and DRAM Memory address. When it is disabled, Intel toggle mode (interleaved burst) is selected.
5 (0)	14-15M Memory Location. 0 : Local Memory Area. 1 : Non-Local Memory Area. When this bit is set to '0', all memory access address from 14M to 15M will be decoded as local memory cycle and access local DRAM if total memory size is beyond 15M. Otherwise, it will be decoded as non-local memory and pass through PCI bus.
4 (0)	15-16M Memory's Location. 0 : Local Memory Area. 1 : Non-Local Memory Area. When this bit is set to '0', all memory access address from 15M to 16M will be decoded as local memory cycle and access local DRAM if total memory size is beyond 16M. Otherwise, it will be decoded as non-local memory and pass through PCI bus.
3 (0)	Page A-B as Local Memory Area. 0 : Non-local Memory Area. 1 : Local Memory Area. When this bit is set to '1', all memory access address from A0000h to BFFFFh will be decoded as local memory cycle and access local DRAM. Otherwise, it will be decoded as non-local memory and pass through PCI bus.
2 (0)	Force Address Region 80000h-9FFFFh as Non-local Memory Area. 0 : Local Memory Area. 1 : Non-local Memory Area. When this bit is set to '1', all memory access address from 80000h to 9FFFFh will be decoded as non-local cycle and pass through PCI bus. Otherwise, it will be decoded as local memory and access to DRAM.
1-0 (00)	Reserved.

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Register Index : **48h**
Register Name : **SMRM - SMRAM Mapping**
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-6 (0h)	Refresh period adjustment when CPU clock changes. 00 : Refresh period/1 when CPU clock/1. 01 : Refresh period/2 when CPU clock/2. 10 : Refresh period/4 when CPU clock/4. 11 : Refresh period/8 when CPU clock/8. These bits are used to change the refresh period when CPU clock frequency has been changed in some green applications. When CPU clock has slowed down, BIOS should change these bits setting to recompensate the refresh period.
5 (0h)	NAJ assert delay 1T in SDRAM cycle. 0 : disable 1 : enable
4 (0)	SMM Page -A or -B Region Code/Data Split. 0 : Disable. 1 : Enable. **Note**: This bit is valid only if this register bit [3:2]="01". When this bit is enabled, only the cycle command with DCJ='0' can access SMRAM. The CPU data access will pass through PCI bus
3-2 (00)	SMRAM Region. 00: SMM Region at D000 Segment will be re-mapped to B000 Segment. 01: SMM Region at A000 or B000 Segment. 10: SMM Region at 3000 Segment will be re-mapped to B000 Segment. 11 : Reserved. Please refer to the following table.
1 (0)	SMRAM Access Control. 0 : Disable. 1 : Enable. When this bit is disabled, SMRAM can only be accessed during SMI handler. Otherwise, SMRAM area can be accessed any time. This bit is used in SMRAM initialization and must be set to '0' when the initialization process is finished
0 (0)	Supports SMRAM Mapping. 0 : Disable. 1 : Enable. This bit is used to disable or enable SMRAM Mapping.

The following is M1531B address re-mapping table for SMRAM mapping enable.

Bit 3-2-1	SMIACTJ	CPU Logical Address	Re-mapped Physical Address	Access DRAM Y/N
000	0	D0000	B0000	Y
000	1	D0000	non-local	N
001	X	D0000	B0000	Y
010	0	A0000/ B0000	A0000/ B0000	Y
010	1	A0000/ B0000	non-local	N
011	X	A0000/ B0000	A0000/ B0000	Y
100	0	30000	B0000	Y
100	1	30000	30000	Y
101	X	30000	B0000	Y

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Register Index : **49h**
Register Name : **ECCP - ECC/Parity Feature**
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7 (0)	Reserved.
6 (0)	SERRJ Duration. 0 : SERRJ will be asserted for 1 PCI Clock. 1 : SERRJ will be asserted until all the ECC(parity) Error Flags are cleared. When the M1531B detects an ECC or parity error, the M1531B will assert SERRJ for 1 PCI Clock (pulse mode) if this bit is set to '0'. Otherwise, the M1531B will assert the SERRJ to report the memory error until all the ECC/parity error flags are cleared (level mode). This bit is used to control the assertion time of SERRJ.
5 (0)	SERRJ on Parity or Multiple-bit ECC Error. 0 : Disable 1 : Enable. When this bit is set to '0', the M1531B will not assert the SERRJ signal when the memory parity or multiple-bit error occurs. Disabling this bit will disable the DRAM parity error check or DRAM ECC multiple-bit error check. Otherwise, the memory data error will be reported to the system via SERRJ assertion to generate NMI (Non-Maskable Interrupt).
4 (0)	SERRJ on Single-bit ECC Error. 0 : Disable. 1 : Enable. When this bit is set to '0', the M1531B will not assert SERRJ on single-bit DRAM ECC errors. Disabling this bit will disable the DRAM ECC single-bit error check. Otherwise, the M1531B will assert SERRJ to generate NMI (Non-Maskable Interrupt) when it detects a single-bit DRAM ECC error.
3-2 (0h)	Reserved.
1 (0)	ECC/Parity Test Mode Enable. 0 : Disable. 1 : Enable. When this bit is set to '1', the ECC check bits or parity bits will be forced to the value defined in register index 4Bh during all the DRAM write cycles. Otherwise, the ECC check bits or parity bits normal function will be performed. This bit must be set to '0' for normal operation.
0 (0)	DRAM Data Integrity Mode. 0 : Parity. 1 : ECC. When this bit is set to '0', the DRAM data integrity will be implemented by the parity algorithm. Otherwise, the ECC data integrity will be implemented.

Register Index : **4Ah**
Register Name : **ECCE - ECC or Parity Error Status**
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-5 (0h)	ECC Multiple-bit or Parity First Row error. These 3 bits record the first row associated with the ECC multiple-bit or parity error. When an error is detected, these bits are updated and ECCE[4] is set.
4 (0)	ECC Multiple-bit Error or Parity Error Flag. The M1531B sets this bit to '1' when either an ECC multiple-bit error or parity error has been detected, depending on whether ECC or parity feature is enabled, respectively. A write of '1' by software to ECCE[4] will clear this bit and write of '0' has no effect on it.
3-1 (0h)	ECC Single-bit First Row Error. These 3 bits record the first row associated with the ECC single-bit error. When an error is detected, these bits are updated and ECCE[0] is set.
0 (0)	ECC Single-bit Error Flag. The M1531B sets this bit to '1' when an ECC single-bit error has been detected and the ECC function is enabled. A write of '1' by software to ECCE[0] will clear this bit and write of '0' has no effect on it.

Register Index : **4Bh**
Register Name **Reserved**
Default Value : 00h
Attribute : Read Only
Size : 8 bits

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Register Index : **4Ch**
Register Name : **SHADRI - SHADOW Regions Read Enable - 1**
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7 (0)	DC000h-DFFFFh Shadow Region Read Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region DC000h-DFFFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.
6 (0)	D8000h-DBFFFh Shadow Region Read Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region D8000h-DBFFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.
5 (0)	D4000h-D7FFFh Shadow Region Read Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region D4000h-D7FFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.
4 (0)	D0000h-D3FFFh Shadow Region Read Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region D0000h-D3FFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.
3 (0)	CC000h-CFFFFh Shadow Region Read Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region CC000h-CFFFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.
2 (0)	C8000h-CBFFFh Shadow Region Read Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region C8000h-CBFFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.
1 (0)	C4000h-C7FFFh Shadow Region Read Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region C4000h-C7FFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.
0 (0)	C0000h-C3FFFh Shadow Region Read Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region C0000h-C3FFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.

Register Index : **4Dh**
Register Name: **SHADRII - SHADOW Regions Read Enable - 2**
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7 (0)	FC000h-FFFFFh Shadow Region Read Enable. 0 : Disable. 1 : Enable When this bit is enabled, address region FC000h-FFFFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.
6 (0)	F8000h-FBFFFh Shadow Region Read Enable. 0 : Disable 1 : Enable. When this bit is enabled, address region F8000h-FBFFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.
5 (0)	F4000h-F7FFFh Shadow Region Read Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region F4000h-F7FFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.
4 (0)	F0000h-F3FFFh Shadow Region Read Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region F0000h-F3FFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.
3 (0)	EC000h-EFFFFh Shadow Region Read Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region EC000h-EFFFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.
2 (0)	E8000h-EBFFFh Shadow Region Read Enable 0 : Disable. 1 : Enable. When this bit is enabled, address region E8000h-EBFFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.
1 (0)	E4000h-E7FFFh Shadow Region Read Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region E4000h-E7FFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.
0 (0)	E0000h-E3FFFh Shadow Region Read Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region E0000h-E3FFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.

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Register Index : **4Eh**
Register Name : **SHADWI - SHADOW Regions Write Enable - 1**
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7(0)	DC000h-DFFFFh Shadow Region Write Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region DC000h-DFFFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.
6 (0)	D8000h-DBFFFh Shadow Region Write Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region D8000h-DBFFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.
5 (0)	D4000h-D7FFFh Shadow Region Write Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region D4000h-D7FFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.
4 (0)	D0000h-D3FFFh Shadow Region Write Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region D0000h-D3FFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.
3 (0)	CC000h-CFFFFh Shadow Region Write Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region CC000h-CFFFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.
2 (0)	C8000h-CBFFFh Shadow Region Write Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region C8000h-CBFFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.
1 (0)	C4000h-C7FFFh Shadow Region Write Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region C4000h-C7FFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.
0 (0)	C0000h-C3FFFh Shadow Region Write Enable. 0 : Disable. 1 : Enable. When the above bits are enabled, the corresponding memory address region write cycle will access local DRAM. Otherwise, it will pass through PCI bus.

Register Index : **4Fh**
Register Name : **SHADWII - SHADOW Regions Write Enable - 2**
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7 (0)	FC000h-FFFFFh Shadow Region Write Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region FC000h-FFFFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.
6 (0)	F8000h-FBFFFh Shadow Region Write Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region F8000h-FBFFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.
5 (0)	F4000h-F7FFFh Shadow Region Write Enable 0 : Disable. 1 : Enable. When this bit is enabled, address region F4000h-F7FFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.
4 (0)	F0000h-F3FFFh Shadow Region Write Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region F0000h-F3FFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.
3 (0)	EC000h-EFFFFh Shadow Region Write Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region EC000h-EFFFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.
2 (0)	E8000h-EBFFFh Shadow Region Write Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region E8000h-EBFFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.
1 (0)	E4000h-E7FFFh Shadow Region Write Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region E4000h-E7FFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.
0 (0)	E0000h-E3FFFh Shadow Region Write Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region E0000h-E3FFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.

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Register Index : **50h**
Register Name : **SHADCI - SHADOW Regions Cacheable Enable - 1**
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7 (0)	DC000h-DFFFFh Shadow Region Cacheable Enable. 0 : Disable. 1 : Enable. When this bit is enabled and SHADRI[7] = '1', address region DC000h-DFFFFh memory access will become cacheable. Otherwise, it will be non cacheable.
6 (0)	D8000h-DBFFFh Shadow Region Cacheable Enable. 0 : Disable. 1 : Enable. When this bit is enabled and SHADRI[6] = '1', address region D8000h-DBFFFh memory access will become cacheable. Otherwise, it will be non cacheable.
5 (0)	D4000h-D7FFFh Shadow Region Cacheable Enable. 0 : Disable. 1 : Enable. When this bit is enabled and SHADRI[5] = '1', address region D4000h-D7FFFh memory access will become cacheable. Otherwise, it will be non cacheable.
4 (0)	D0000h-D3FFFh Shadow Region Cacheable Enable. 0 : Disable. 1 : Enable. When this bit is enabled and SHADRI[4] = '1', address region D0000h-D3FFFh memory access will become cacheable. Otherwise, it will be non cacheable.
3 (0)	CC000h-CFFFFh Shadow Region Cacheable Enable. 0 : Disable. 1 : Enable. When this bit is enabled and SHADRI[3] = '1', address region CC000h-CFFFFh memory access will become cacheable. Otherwise, it will be non cacheable.
2 (0)	C8000h-CBFFFh Shadow Region Cacheable Enable. 0 : Disable. 1 : Enable. When this bit is enabled and SHADRI[2] = '1', address region C8000h-CBFFFh memory access will become cacheable. Otherwise, it will be non cacheable.
1 (0)	C4000h-C7FFFh Shadow Region Cacheable Enable. 0 : Disable. 1 : Enable When this bit is enabled and SHADRI[1] = '1', address region C4000h-C7FFFh memory access will become cacheable. Otherwise, it will be non cacheable.
0 (0)	C0000h-C3FFFh Shadow Region Cacheable Enable. 0 : Disable. 1 : Enable. When this bit is enabled and SHADRI[0] = '1', address region C0000h-C3FFFh memory access will become cacheable. Otherwise, it will be non cacheable.

Register Index : **51h**
Register Name : **SHADCII - SHADOW Regions Cacheable Enable - 2**
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7 (0)	FC000h-FFFFFh Shadow Region Cacheable Enable. 0 : Disable. 1 : Enable. When this bit is enabled and SHADRII[7] = '1', address region FC000h-FFFFFh memory access will become cacheable. Otherwise, it will be non cacheable.
6 (0)	F8000h-FBFFFh Shadow Region Cacheable Enable. 0 : Disable. 1 : Enable. When this bit is enabled and SHADRII[6] = '1', address region F8000h-FBFFFh memory access will become cacheable. Otherwise, it will be non cacheable
5 (0)	F4000h-F7FFFh Shadow Region Cacheable Enable. 0 : Disable. 1 : Enable. When this bit is enabled and SHADRII[5] = '1', address region F4000h-F7FFFh memory access will become cacheable. Otherwise, it will be non cacheable.
4 (0)	F0000h-F3FFFh Shadow Region Cacheable Enable. 0 : Disable. 1 : Enable. When this bit is enabled and SHADRII[4] = '1', address region F0000h-F3FFFh memory access will become cacheable. Otherwise, it will be non cacheable.
3 (0)	EC000h-EFFFFh Shadow Region Cacheable Enable. 0 : Disable. 1 : Enable. When this bit is enabled and SHADRII[3] = '1', address region EC000h-EFFFFh memory access will become cacheable. Otherwise, it will be non cacheable.
2 (0)	E8000h-EBFFFh Shadow Region Cacheable Enable. 0 : Disable. 1 : Enable. When this bit is enabled and SHADRII[2] = '1', address region E8000h-EBFFFh memory access will become cacheable. Otherwise, it will be non cacheable.
1 (0)	E4000h-E7FFFh Shadow Region Cacheable Enable. 0 : Disable. 1 : Enable. When this bit is enabled and SHADRII[1] = '1', address region E4000h-E7FFFh memory access will become cacheable. Otherwise, it will be non cacheable.
0 (0)	E0000h-E3FFFh Shadow Region Cacheable Enable. 0 : Disable. 1 : Enable. When this bit is enabled and SHADRII[0] = '1', address region E0000h-E3FFFh memory access will become cacheable. Otherwise, it will be non cacheable.

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Register Index : **52h**
Register Name : **MISII - Miscellaneous - 2**
Default Value : F0h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-3 (00h)	SRAM Module Presence Detect Bits HA[31:27] (Read Only). The M1531B will strobe HA[31:27] values and write them into the five-bit register during reset. BIOS can use these five bits to determine the SRAM module configuration and program the L2 size and type.
2-1 (00)	CPU Bus Frequency. (Read Only) 00 : 60 MHz. 01 : 66 MHz. 10 : 75 MHz. 11 : 83.3 MHz. These two bits are hardware strobe from HA[26:25] to indicate the CPU bus frequency.
0 (0)	PCI/CPU Concurrency Enable. 0 : Disable. 1 : Enable. When this bit is enabled, CPU to L2 access will be concurrent with PCI-to-DRAM access. Otherwise, PCI to DRAM access will always prevent the CPU from issuing cycles by asserting AHOLD.

Register Index : **53h**
Register Name : **Reserved**
Default Value : 00h
Attribute : Read Only
Size : 8 bits

Register Index : **55h-54h**
Register Name : **FBMR - PCI Programmable Frame Buffer Memory Region**
Default Value : FFFFh
Attribute : Read/Write
Size : 16 bits

Bit Number	Bit Function
15-4(000)	Base address of Programmable Frame Buffer. The 12-bits correspond to A[31:20] of the starting address. The remaining bits A[19:0] are assumed to be zero. These bits combined with bits 3-0 can determine the Frame Buffer starting address and stopping address. When Index-56h bit 0 is set to '1', the M1531B will decode the boundary and enable CPU to PCI write buffer.
3-0(0)	Size of Programmable Frame Buffer. X000 : 1 Mbytes. X001 : 2 Mbytes X010 : 4 Mbytes. X011 : 8 Mbytes. X100 : 16 Mbytes. Others : Reserved. These bits are used to program the Frame Buffer Size.

Note : The Frame Buffer Region should not overlap with local memory.

Register Index : **56h**
Register Name : **H2PW - CPU to PCI Write Buffer Option**
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7 (0)	Host to PCI Write Buffered Cycle Selection. 0 : Only CPU Memory Write to PCI Frame Buffer. 1 : All CPU to PCI Memory Write Cycle. If this bit is enabled, all non-local memory cycle will enable the CPU to PCI write buffer. Otherwise, only programmable Frame Buffer or fixed A/B segment Frame Buffer will utilize the Host to PCI write buffer.
6 (0)	Linear-merge for Frame Buffer Cycle. 0 : Disable. 1 : Enable. When this bit is enabled, only the consecutive linear increased addresses can be merged. Otherwise, the second write cycle will write into a new Host to PCI Write Buffer location instead of merging with the previous buffer location posted by the first write cycle.
5 (0)	Word-merge for Frame Buffer Cycle. 0 : Disable. 1 : Enable. This bit is used to enable the word-merge feature for Frame Buffer cycle. When this feature is enabled, the M1531B will merge the latter 16-bit Frame Buffer write data into the previous buffer location posted by the previous 16-bit Frame Buffer write data if the HBEJ[7:0] are mergeable. The M1531B will check the CPU HBEJ[7:0] and determine if they can be merged or not.
4 (0)	Byte-merge for Frame Buffer Cycle. 0 : Disable. 1 : Enable. This bit is used to enable the byte-merge feature for Frame Buffer cycle. When this feature is enabled, the M1531B will merge the latter 8-bit Frame Buffer write data into the previous buffer location posted by the previous Frame Buffer write data if the HBEJ[7:0] are mergeable. The M1531B will check the CPU HBEJ[7:0] and determine if they can be merged or not.
3 (0)	Use PCI Fast Back-to-Back. 0 : Disable. 1 : Enable. This bit is used to enable PCI Fast Back-to-Back capability. If this bit is enabled, consecutive PCI write cycles targeted to the same slave will become fast back-to-back cycle on the PCI bus.
2 (0)	Use PCI Write-Burst. 0 : Disable. 1 : Enable. This bit is used to enable PCI write burst capability. If this bit is enabled, the consecutive PCI write cycles will become a burst cycle on the PCI bus.
1 (0)	VGA 0A0000-0BFFFF Fixed Frame Buffer. 0 : Disable. 1 : Enable. This bit is used to enable 0A0000h-0BFFFFh Frame Buffer and the Host to PCI Write Buffer.
0 (0)	Programmable Frame Buffer. 0 : Disable. 1 : Enable. This bit is used to combine with index 55h-54h to enable the programmable PCI Frame Buffer and the Host to PCI Write Buffer.

Register Index : **57h**
Register Name : **H2PO - CPU to PCI Option**
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7 (0)	Reserved.
6 (0)	APIC Support, Invalidate PCI to DRAM Read Ahead Buffer When PHLDAJ Goes Low. 0 : Disable. 1 : Enable. When APIC is supported in Dual Processor system, this bit must be set to '1' to invalidate PCI to DRAM Read Ahead Buffer since the M1531B cannot realize Interrupt Synchronous event. But in Single Processor systems, the M1531B can detect Interrupt Synchronous event to invalidate PCI to DRAM Read Ahead Buffer automatically. This bit is recommended to be reset to '0' in Single Processor systems.
5 (0)	Translate CPU Shutdown cycle to Port 92 cycle. 0 : Enable. 1 : Disable. When this bit is set to '1', the M1531B will forward a Shut-down Special cycle from CPU bus to PCI bus. When this bit is reset to '0', the M1531B will write 01h to I/O address port 92 on PCI bus.
4-0 (00h)	Reserved.

Register Index : **58h**
Register Name : **P2HO - PCI to Main Memory / PCI Arbiter Option**
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7 (0)	PCI Master GAT mode 0 : Disable 1 : Enable
6-3 (00h)	Reserved.
2 (0)	CPU Access PCI During Passive Release. 0 : Disable. 1 : Enable. This bit controls CPU to PCI access during Passive Release. When it is enabled, CPU to PCI access is allowed during Passive Release. Otherwise, arbiter only accepts another PCI master access to local DRAM.
1 (0)	Passive Release of PHOLD. 0 : Disable. 1 : Enable. When this bit is enabled, the M1531B will recognize Passive Release signaled from M1533/M1543 by de-asserting PHOLDJ for a PCI Clock and then asserting PHOLDJ for a PCI Clock. The M1531B will de-assert the PHLDAJ signal and re-arbitrate PCI bus request and possibly allow the CPU to access PCI depending on the bit 2 setting. When this bit is disabled, the M1531B does not recognize Passive Release, i.e. , PHLDAJ will be continued to be asserted. A value '1' is recommended for normal operation.
0 (0)	Reserved.

Register Index : **59h**
Register Name : **PCIM - PCI Master Time Slice**
Default Value : 20h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-0(00h)	Number of PCI clocks for PCI Master time slice. The Time-Slice will guarantee the minimum clocks that the PCI master is granted the ownership of PCI bus. The time-slice counter is started when PCI grant is asserted and bus is idle. The bits [1:0] are assumed to be "00" and are ignored.

Register Index : **5Ah**
Register Name : **CPUM - CPU Master Time Slice**
Default Value : 20h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-0 (00h)	Number of PCI clocks for CPU Bus time slice. The Time-Slice will guarantee the minimum clocks that the CPU master is granted the ownership of PCI bus. The time-slice counter is started when CPU grant is asserted and bus is idle. The bits [1:0] are assumed to be "00" and are ignored.

Register Index : **5Bh**
Register Name : **PCIRC - PCI Retry control for P2H cycle**
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7 (0h)	Reserved.
6 (0)	Retry PCI Master when address crosses buffer boundary. 0 : disable 1 : enable When this bit is set, PCI arbiter will become more fair to retry the PCI master if it occupies PCI bus too long. A '1' is recommended in normal operation.
5-4 (0h)	Reserved
3-2 (00)	Retry Latency for Second Data Phase Control. 00 : Retry on Second Data Phase if Wait State > 8 PCI Clocks. 01 : Retry on Second Data Phase if Wait State > 4 PCI Clocks. 10 : Retry on Second Data Phase if Wait State > 2 PCI Clocks. 11 : Never Retry on Second Data Phase. These bits are used to retry a PCI master cycle when the latency to the second data phase is about to exceed the programmed number of PCI clocks. When these bits are set to '11', the M1531B will complete the second data transfer regardless of latency.
1-0 (00)	Retry Latency for First Data Phase Control. 00 : Retry on First Data Phase if Wait State > 32 PCI Clocks. 01 : Retry on First Data Phase if Wait State > 16 PCI Clocks. 10 : Retry on First Data Phase if Wait State > 8 PCI Clocks. 11 : Never Retry on first Data phase. These bits are used to retry a PCI master cycle when the latency to the first data phase is about to exceed the programmed number of PCI clocks. When these bits are set to '11', the M1531B will complete the first data transfer regardless of latency.

Register Index : **5Ch**
Register Name : **SDRAMCI - Synchronous DRAM Control Register I**
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-5 (0h)	SDRAM Operation Mode Selection. 000 : Normal Operation(Default). 001 : NOP(No Operation) Command Enable. 010 : PALL(Pre-charge All Banks) Command Enable. 011 : MRS(Mode Register Set) Command Enable. 100 : CBR(CAS Before RAS Refresh) Enable. Others : Reserved. **Note**: (1) Before switching from one mode of SDRAM to another, the BIOS should ensure the DRAM buffer is empty. For example, by issuing a DRAM read cycle to flush the DRAM buffer. (2) In the MRS mode, the MA is translated as the column address and the BIOS should issue the appropriate CPU addresses to program the SDRAMs. NOP mode is used to force all CPU cycles to DRAM to generate an SDRAM NOP command on the memory interface. PALL mode is used to force all CPU cycles to DRAM to generate an SDRAM pre-charge all banks command on the memory interface. MRS command is used to convert all CPU cycles to commands on the memory interface. MA[11:0] lines are used to drive command: MA[2:0]= '010' for burst of 4 mode, MA[3]= '1/0' for interleave/linear wrap mode, MA[4]= '1/0' for the value of CAS Latency (3 HCLKINs / 2 HCLKINs), MA[6:5]= '01' and MA[11:7]= '00000'. All these modes are used to initialize SDRAM. Please refer to the hardware and software setup section.
4 (0)	CAS Latency. 0 : 3 HCLKINs. 1 : 2 HCLKINs. This bit is used to control read data valid wait states after read command has been issued. '0' means the CAS Latency is 3 HCLKINs, and 1 means the CAS Latency is 2 HCLKINs.
3 (0)	RAS Active to Read/Write Command Delay Time(tRCD). 0 : 3 HCLKIN's. 1 : 2 HCLKIN's. This bit is used to control RASJ to CASJ delay. The same programmed value as bit 4 is highly recommended for normal operation.
2-1 (0h)	RAS Pre-charge Timing (in HCLKIN's). RAS Pre-charge RAS Active to Refresh/RAS-Active to Time (tRP) Pre-charge Time (tRAS) Refresh/RAS-Active Time (tRC) tRP tRAS tRC 00 : 3 6 9 01 : 3 5 8 10 : 3 4 7 11 : 2 5 7 These two bits are used to control RAS pre-charge time, RAS active to pre-charge time, refresh to RAS active, refresh to refresh, RASJ active to refresh, and RASJ active to RASJ active time.
0 (0)	Selection of RASJ[7]/SRASJ[0] and RASJ[6]/SCASJ[0]. 0 : SRASJ[0] and SCASJ[0]. 1 : RASJ[7] and RASJ[6]. This bit is used to select the multi-function supported by the RASJ[7]/SRASJ[0] and RASJ[6]/SCASJ[0] pins. When this bit is programmed to be '1', 8 row DRAM configuration is supported. When this bit is programmed to be '0', SDRAM configuration is supported.

Register Index : **5Dh**
Register Name : **SDRAMCII - Synchronous DRAM Control Register II**
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7 (0)	Reserved.
6 (0)	SDRAM Speculative Read. 0 : Disabled. 1 : Enabled. This bit is used to support SDRAM speculative read feature. At the end of T1, M1531B will speculatively read the SDRAM data assuming the memory read cycle is DRAM page hit cycle. If the speculation is not correct (DRAM page miss or non DRAM cycle), M1531B will issue the pre-charge command to reset the SDRAM access after the cycle is decoded correctly (at the end of T2). Since the DRAM address only issues one clock setup time, the feature is suggested to be enabled only when the SDRAM clock is equal or below 60 MHz. In the other condition, this feature should be disabled.
5 (0h)	Reserved
4 (0h)	SDRAM internal Page Hit Detection 0 : Disable 1 : Enable When this bit is enabled, SDRAM state machine detects the cycle as the page hit during SDRAM bank changing. A '1' is recommended to enhance SDRAM performance.
3-2 (0h)	Reserved.
1 (0)	CLKEN[1:0]/PREQJ[4],PGNTJ[4] Select. 0 : CLKEN[1:0] Select. 1 : PREQJ[4], PGNTJ[4] Select. This bit is used to select the function supported by the multi-functional pins CLKEN[1:0]/PREQJ[4],PGNTJ[4]. When this bit is programmed as '0', CLKEN[1:0] are selected, SDRAM Self Refresh feature is supported. When this bit is programmed as '1', the fifth PCI master is supported.
0 (0)	JEDEC "2n rule" Restricted. 0 : Yes. 1 : No. (The Interval Between Two Commands Not Limited to Be Even-numbered.) This bit is used to support TI 2n rule SDRAM, the interval between two commands has to be limited to even-numbers.

Register Index : **5Eh**
Register Name : **Reserved**
Default Value : 00h
Attribute : Read Only
Size : 8 bits

Register Index : **5Fh**
Register Name : **DRAMHP - DRAM Configuration of Half-Populated Banks**
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-6 (0h)	Reserved.
5 (0)	Which Half of Row5 (RAS5J) Is Populated 0 : Lower Dword (MD[31:0]). 1 : Higher Dword (MD[63:32]). **Note**: This bit is valid only if Index-43h bit7 = 1. This bit is used to control Row5 High/Low Dword data swap.
4 (0)	Which Half of Row4 (RAS4J) Is Populated. 0 : Lower Dword (MD[31:0]). 1 : Higher Dword (MD[63:32]). **Note**: This bit is valid only if Index-43h bit6 = 1. This bit is used to control Row4 High/Low Dword data swap.
3 (0)	Which Half of Row3 (RAS3J) Is Populated. 0 : Lower DWord (MD[31:0]). 1 : Higher Dword (MD[63:32]). **Note** : This bit is valid only if Index-43h bit5 = 1. This bit is used to control Row3 High/Low Dword data swap.
2 (0)	Which Half of Row2 (RAS2J) Is Populated. 0 : Lower Dword (MD[31:0]). 1 : Higher Dword (MD[63:32]). **Note**: This bit is valid only if Index-43h bit4 = 1. This bit is used to control Row2 High/Low Dword data swap.
1 (0)	Which Half of Row1 (RAS1J) Is Populated. 0 : Lower Dword (MD[31:0]). 1 : Higher Dword (MD[63:32]). **Note**: This bit is valid only if Index-43h bit3 = 1. This bit is used to control Row1 High/Low Dword data swap.
0 (0)	Which Half of Row0 (RAS0J) Is Populated. 0 : Lower DWord (MD[31:0]). 1 : Higher Dword (MD[63:32]). **Note**: This bit is valid only if Index-43h bit2 = 1. M1531B supports flexible 32-bit access. This bit is used to control Row0 High/Low Dword data swap.

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Register Index : **60h**
Register Name : **DB0CI - DRAM Row0 Configuration -1**
Default Value : 08h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-0 (00h)	Row0 DRAM Top Address Boundary-1. A27-A20 Address Boundary.

Register Index : **61h**
Register Name : **DB0CII - DRAM Row0 Configuration-2**
Default Value : 40h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-6 (01)	DRAM MA Definition. 00 : Row0 DRAM Disable in FPM/EDO or SDRAM when 64Mbits 2 bank is selected. 01 : Row0 DRAM uses standard MA Mapping in FPM/EDO or SDRAM when 16Mbits 2 bank is selected. 10 : Row0 DRAM uses 64M technology MA Mapping in FPM/EDO or SDRAM when 64Mbits 4 bank is selected. (MA[12:11] are used as bank selection). 11 : Row0 DRAM uses 1Mx16 MA Mapping in FPM/EDO or SDRAM when 64Mbits 4 bank is selected. (MA[13:12] are used as bank selection). These two bits are used to program the DRAM MA used on DRAM Row 0. Please refer to the DRAM MA translation table.
5-4 (0h)	Row0 DRAM Type. 00 : Standard Fast-Page Mode DRAM. 01 : EDO DRAM. 10 : Reserved. 11 : Synchronous DRAM. These two bits are used to program the DRAM type used on DRAM Row 0.
3-0 (0h)	Row0 DRAM Top Address Boundary-2. A31-A28 Address Boundary. These four bits are used to combine index-60h to decide the top memory size for DRAM Row 0.

The following types of SDRAMs are supported when bits [7:6] = '00'.

Memory Organization	Memory Size	Row Address	Column Address
2Bx2Mx16	64Mb	13	8
2Bx4Mx8	64Mb	13	9
2Bx8Mx4	64Mb	13	10
2Bx1Mx32	64Mb	12	8

The following types of FPM/EDO DRAMs are supported when bits [7:6] = '01'.

Memory Organization	Memory Size	Row Address	Column Address
512Kx8	4Mb	10	9
1Mx4	4Mb	10	10
1Mx16	16Mb	10	10
2Mx8	16Mb	11	10
4Mx4	16Mb	11	11
4Mx4	16Mb	12	10

The following types of SDRAMs are supported when bits [7:6] = '01'.

Memory Organization	Memory Size	Row Address	Column Address
2Bx512Kx16	16Mb	11	8
2Bx1Mx8	16Mb	11	9
2Bx2Mx4	16Mb	11	10
2Bx512Kx64	64Mb	11	8
2Bx1Mx32	64Mb	11	9
2Bx2Mx16	64Mb	11	10

The following types of FPM/EDO DRAMs are supported when bits [7:6] = '10'.

Memory Organization	Memory Size	Row Address	Column Address
4Mx16	64Mb	11	11
8Mx8	64Mb	12	11
16Mx4	64Mb	12	12

The following types of SDRAMs are supported when bits [7:6] = '10'.

Memory Organization	Memory Size	Row Address	Column Address
4Bx512Kx32	64Mb	11	8
4Bx1Mx16	64Mb	11	9
4Bx2Mx8	64Mb	11	10

The following types of FPM/EDO DRAMs are supported when bits [7:6] = '11'.

Memory Organization	Memory Size	Row Address	Column Address
1Mx16	16Mb	12	8
2Mx8	16Mb	12	9

The following types of SDRAMs are supported when bits [7:6] = '11'.

Memory Organization	Memory Size	Row Address	Column Address
4Bx1Mx16	64Mb	12	8
4Bx2Mx8	64Mb	12	9
4Bx4Mx4	64Mb	12	10

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The M1531B supports 8 rows of DRAM, and each of them can be 32-bit or 64-bit wide. DRAM Rowx Configuration register defines populated DRAM type and Top Address Boundary for each row. DB0CI and DB0CII define for Row 0, DB1CI and DB1CII define for Row 1, DB2CI and DB2CII define for Row 2, DB3CI and DB3CII define for Row 3, DB4CI and DB4CII define for Row 4, DB5CI and DB5CII define for Row 5, B6CI and DB6CII define for Row 6, and DB7CI and DB7CII define for Row 7. Contents of these 8-bit registers represent the boundary address in 1MB granularity and DRAM type populated.

DB0CII[3:0]&DB0CI[7:0] = Total amount of memory in row 0 (Unit: 1MB).

DB0CII[5:4] define different DRAM Type for row 0.

DB0CII[7:6] define different MA Type or unpopulated for row 0.

DB1CII[3:0]&DB1CI[7:0] = Total amount of memory in row 0 + row 1 (Unit: 1MB).

DB1CII[5:4] define different DRAM Type for row 1.

DB1CII[7:6] define different MA Type or unpopulated for row 1.

DB2CII[3:0]&DB2CI[7:0] = Total amount of memory in row 0 + row 1 + row 2 (Unit: 1MB).

DB2CII[5:4] define different DRAM Type for row 2.

DB2CII[7:6] define different MA Type or unpopulated for row 2.

DB3CII[3:0]&DB3CI[7:0] = Total amount of memory in row 0 + row 1 + row 2 + row 3 (Unit: 1MB).

DB3CII[5:4] define different DRAM Type for row 3.

DB3CII[7:6] define different MA Type or unpopulated for row 3.

DB4CII[3:0]&DB4CI[7:0] = Total amount of memory in row 0 + row 1 + row 2 + row 3 + row 4 (Unit: 1MB).

DB4CII[5:4] define different DRAM Type for row 4.

DB4CII[7:6] define different MA Type or unpopulated for row 4.

DB5CII[3:0]&DB5CI[7:0] = Total amount of memory in row 0 + row 1 + row 2 + row 3 + row 4 + row 5 (Unit: 1MB).

DB5CII[5:4] define different DRAM Type for row 5.

DB5CII[7:6] define different MA Type or unpopulated for row 5.

DB6CII[3:0]&DB6CI[7:0] = Total amount of memory in row 0 + row 1 + row 2 + row 3 + row 4 + row 5 + row 6 (Unit: 1MB).

DB6CII[5:4] define different DRAM Type for row 6.

DB6CII[7:6] define different MA Type or unpopulated for row 6.

DB7CII[3:0]&DB7CI[7:0] = Total amount of memory in row 0 + row 1 + row 2 + row 3 + row 4 + row 5 + row 6 + row 7 (in 1MB).

DB7CII[5:4] define different DRAM Type for row 7.

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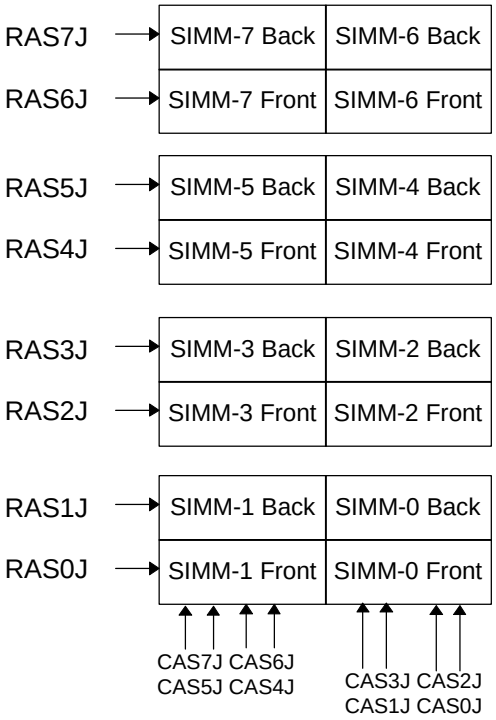
DB7CII[7:6] define different MA Type or unpopulated for row 7.
As an example of a system configuration where 8 physical rows are configured for either single-sided or double-sided SIMMs, the DRAM will be configured like the following figure.



In this configuration, the M1531B will drive two RASJ lines to the SIMM bank. If the single-sided SIMMs are populated, the even RASJ is used and the odd RASJ is not used. If the double-sided SIMMs are populated, both RASJ lines are used.

Example A
Two single-sided 1MB X 32 FPM DRAMs (standard MA mapping) are populated at row 0, a total of 8 MB of DRAM. The DBxCI and DBxCII registers should be programmed as follows:

DB0CI = 08h DB0CII = 40h
DB1CI = 08h DB1CII = 00h
DB2CI = 08h DB2CII = 00h
DB3CI = 08h DB3CII = 00h
DB4CI = 08h DB4CII = 00h
DB5CI = 08h DB5CII = 00h
DB6CI = 08h DB6CII = 00h
DB7CI = 08h DB7CII = 00h

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Example B

Four single-sided 1MB X 32 EDO DRAMs (1Mx16 MA mapping) are populated on row 0 and row 2, a total of 16 MB of DRAM. The DBxCI and DBxCII registers should be programmed as follows:

DB0CI = 08h DB0CII = D0h
DB1CI = 08h DB1CII = 00h
DB2CI = 10h DB2CII = D0h
DB3CI = 10h DB3CII = 00h
DB4CI = 10h DB4CII = 00h
DB5CI = 10h DB5CII = 00h
DB6CI = 10h DB6CII = 00h
DB7CI = 10h DB7CII = 00h

Example C

Two double-sided 2MB X 32 FPM DRAMs (standard MA mapping) are populated on row 4 , row 5, row 6, and row 7, a total of 32 MB of DRAM. The DBxCI and DBxCII registers should be programmed as follows:

DB0CI = 00h DB0CII = 00h
DB1CI = 00h DB1CII = 00h
DB2CI = 00h DB2CII = 00h
DB3CI = 00h DB3CII = 00h
DB4CI = 08h DB4CII = 40h
DB5CI = 10h DB5CII = 40h
DB6CI = 18h DB6CII = 40h
DB7CI = 20h DB7CII = 40h

Example D

One double-sided 2MB X 32 EDO DRAMs (1Mx16 MA mapping) are populated on row 2 and row 3, and one double-sided 8MB X 32 FPM DRAMs (64Mb MA mapping) are populated on row 6 and row 7, a total of 80 MB of DRAM. The DBxCI and DBxCII registers should be programmed as follows:

DB0CI = 00h DB0CII = 00h
DB1CI = 00h DB1CII = 00h
DB2CI = 08h DB2CII = D0h
DB3CI = 10h DB3CII = D0h
DB4CI = 10h DB4CII = 00h
DB5CI = 10h DB5CII = 00h
DB6CI = 30h DB6CII = 80h
DB7CI = 50h DB7CII = 80h

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Register Index : **62h**
Register Name : **DB1CI - DRAM Row1 Configuration -1**
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-0 (00h)	Row1 DRAM Top Address Boundary- 1. A27-A20 Address Boundary.

Register Index : **63h**
Register Name : **DB1CII - DRAM Row1 Configuration-2**
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-6 (0h)	DRAM MA Definition. 00 : Row1 DRAM Disable in FPM/EDO or SDRAM when 64Mbits 2 bank is selected. 01 : Row1 DRAM uses standard MA Mapping in FPM/EDO or SDRAM when 16Mbits 2 bank is selected. 10 : Row1 DRAM uses 64M technology MA Mapping in FPM/EDO or SDRAM when 64Mbits 4 bank is selected. (MA[12:11] are used as bank selection). 11 : Row1 DRAM uses 1Mx16 MA Mapping in FPM/EDO or SDRAM when 64Mbits 4 bank is selected. (MA[13:12] are used as bank selection). These two bits are used to program the DRAM MA used on DRAM Row 1. Please refer to the DRAM MA translation table.
5-4 (0h)	Row1 DRAM Type. 00 : Standard Fast-Page Mode DRAM. 01 : EDO DRAM. 10 : Reserved. 11 : Synchronous DRAM. These two bits are used to program the DRAM type used on DRAM Row 1.
3-0 (0h)	Row1 DRAM Top Address Boundary - 2. A31-A28 Address Boundary. These four bits are used to combine index-62h to decide top memory size for DRAM Row1.

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Register Index : **64h**
Register Name : **DB2CI - DRAM Row2 Configuration-1**
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-0 (00h)	Row2 DRAM Top Address Boundary - 1. A27-A20 Address Boundary.

Register Index : **65h**
Register Name : **DB2CII - DRAM Row2 Configuration-2**
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-6 (0h)	DRAM MA Definition. 00 : Row2 DRAM Disable in FPM/EDO or SDRAM when 64Mbits 2 bank is selected. 01 : Row2 DRAM uses standard MA Mapping in FPM/EDO or SDRAM when 16Mbits 2 bank is selected. 10 : Row2 DRAM uses 64M technology MA Mapping in FPM/EDO or SDRAM when 64Mbits 4 bank is selected. (MA[12:11] are used as bank selection). 11 : Row2 DRAM uses 1Mx16 MA Mapping in FPM/EDO or SDRAM when 64Mbits 4 bank is selected. (MA[13:12] are used as bank selection). These two bits are used to program the DRAM MA used on DRAM Row 2. Please refer to the DRAM MA translation table.
5-4 (0h)	Row2 DRAM Type. 00 : Standard Fast-Page Mode DRAM. 01 : EDO DRAM. 10 : Reserved. 11 : Synchronous DRAM. These two bits are used to program the DRAM type used on DRAM Row 2.
3-0 (0h)	Row2 DRAM Top Address Boundary-2. A31-A28 Address Boundary. These four bits are used to combine index-64h to decide top memory size for DRAM Row2.

Register Index : **66h**
Register Name : **DB3CI - DRAM Row3 Configuration-1**
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-0(00h)	Row3 DRAM Top Address Boundary - 1. A27-A20 Address Boundary.

Register Index : **67h**
Register Name : **DB3CII - DRAM Row3 Configuration-2**
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-6 (0h)	DRAM MA Definition. 00 : Row3 DRAM Disable in FPM/EDO or SDRAM when 64Mbits 2 bank is selected. 01 : Row3 DRAM uses standard MA Mapping in FPM/EDO or SDRAM when 16Mbits 2 bank is selected. 10 : Row3 DRAM uses 64M technology MA Mapping in FPM/EDO or SDRAM when 64Mbits 4 bank is selected. (MA[12:11] are used as bank selection). 11 : Row3 DRAM uses 1Mx16 MA Mapping in FPM/EDO or SDRAM when 64Mbits 4 bank is selected. (MA[13:12] are used as bank selection). These two bits are used to program the DRAM MA used on DRAM Row 3. Please refer to the DRAM MA translation table.
5-4 (0h)	Row3 DRAM Type. 00 : Standard Fast-Page Mode DRAM. 01 : EDO DRAM. 10 : Reserved. 11 : Synchronous DRAM. These two bits are used to program the DRAM type used on DRAM Row 3.
3-0(0h)	Row3 DRAM Top Address Boundary - 2. A31-A28 Address Boundary. These four bits are used to combine index-66h to decide top memory size for DRAM Row3.

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Register Index : **68h**
Register Name : **DB4CI - DRAM Row4 Configuration-1**
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-0(00h)	Row4 DRAM Top Address Boundary - 1. A27-A20 Address Boundary.

Register Index : **69h**
Register Name : **DB4CII - DRAM Row4 Configuration-2**
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-6 (0h)	DRAM MA Definition. 00 : Row4 DRAM Disable in FPM/EDO or SDRAM when 64Mbits 2 bank is selected. 01 : Row4 DRAM uses standard MA Mapping in FPM/EDO or SDRAM when 16Mbits 2 bank is selected. 10 : Row4 DRAM uses 64M technology MA Mapping in FPM/EDO or SDRAM when 64Mbits 4 bank is selected. (MA[12:11] are used as bank selection). 11 : Row4 DRAM uses 1Mx16 MA Mapping in FPM/EDO or SDRAM when 64Mbits 4 bank is selected. (MA[13:12] are used as bank selection). These two bits are used to program the DRAM MA used on DRAM Row 4. Please refer to the DRAM MA translation table.
5-4 (0h)	Row4 DRAM Type. 00 : Standard Fast-Page Mode DRAM. 01 : EDO DRAM. 10 : Reserved. 11 : Synchronous DRAM. These two bits are used to program the DRAM type used on DRAM Row 4.
3-0 (0h)	Row4 DRAM Top Address Boundary - 2. A31-A28 Address Boundary. These four bits are used to combine index-68h to decide top memory size for DRAM Row4.

Register Index : **6Ah**
Register Name : **DB5CI - DRAM Row5 Configuration-1**
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-0(00h)	Row5 DRAM Top Address Boundary - 1. A27-A20 Address Boundary.

Register Index : **6Bh**
Register Name : **DB5CII - DRAM Row0 Configuration-2**
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-6 (0h)	DRAM MA Definition. 00 : Row5 DRAM Disable in FPM/EDO or SDRAM when 64Mbits 2 bank is selected. 01 : Row5 DRAM uses standard MA Mapping in FPM/EDO or SDRAM when 16Mbits 2 bank is selected. 10 : Row5 DRAM uses 64M technology MA Mapping in FPM/EDO or SDRAM when 64Mbits 4 bank is selected. (MA[12:11] are used as bank selection). 11 : Row5 DRAM uses 1Mx16 MA Mapping in FPM/EDO or SDRAM when 64Mbits 4 bank is selected. (MA[13:12] are used as bank selection). These two bits are used to program the DRAM MA used on DRAM Row 5. Please refer to the DRAM MA translation table.
5-4 (0h)	Row5 DRAM Type. 00 : Standard Fast-Page Mode DRAM. 01 : EDO DRAM. 10 : Reserved. 11 : Synchronous DRAM. These two bits are used to program the DRAM type used on DRAM Row 5.
3-0(0h)	Row5 DRAM Top Address Boundary - 2. A31-A28 Address Boundary. These four bits are used to combined index-6Ah to decide top memory size for DRAM Row5.

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Register Index : **6Ch**
Register Name : **DB6CI - DRAM Row6 Configuration-1**
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-0(00h)	Row6 DRAM Top Address Boundary - 1. A27-A20 Address Boundary.

Register Index : **6Dh**
Register Name : **DB6CII - DRAM Row6 Configuration-2**
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-6 (0h)	DRAM MA Definition. 00 : Row6 DRAM Disable in FPM/EDO or SDRAM when 64Mbits 2 bank is selected. 01 : Row6 DRAM uses standard MA Mapping in FPM/EDO or SDRAM when 16Mbits 2 bank is selected. 10 : Row6 DRAM uses 64M technology MA Mapping in FPM/EDO or SDRAM when 64Mbits 4 bank is selected. (MA[12:11] are used as bank selection). 11 : Row6 DRAM uses 1Mx16 MA Mapping in FPM/EDO or SDRAM when 64Mbits 4 bank is selected. (MA[13:12] are used as bank selection). These two bits are used to program the DRAM MA used on DRAM Row 6. Please refer to the DRAM MA translation table.
5-4 (0h)	Row6 DRAM Type. 00 : Standard Fast-Page Mode DRAM. 01 : EDO DRAM. 10 : Reserved. 11 : Synchronous DRAM. These two bits are used to program the DRAM type used on DRAM Row 6.
3-0 (0h)	Row6 DRAM Top Address Boundary-2. A31-A28 Address Boundary. These four bits are used to combine index-6Ch to decide top memory size for DRAM Row6.

Register Index : **6Eh**
Register Name : **DB7CI - DRAM Row7 Configuration-1**
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-0 (00h)	Row7 DRAM Top Address Boundary - 1. A27-A20 Address Boundary.

Register Index : **6Fh**
Register Name : **DB7CII - DRAM Row7 Configuration-2**
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-6 (0h)	DRAM MA Definition. 00 : Row7 DRAM Disable in FPM/EDO or SDRAM when 64Mbits 2 bank is selected. 01 : Row7 DRAM uses standard MA Mapping in FPM/EDO or SDRAM when 16Mbits 2 bank is selected. 10 : Row7 DRAM uses 64M technology MA Mapping in FPM/EDO or SDRAM when 64Mbits 4 bank is selected. (MA[12:11] are used as bank selection). 11 : Row7 DRAM uses 1Mx16 MA Mapping in FPM/EDO or SDRAM when 64Mbits 4 bank is selected. (MA[13:12] are used as bank selection). These two bits are used to program the DRAM MA used on DRAM Row 7. Please refer to the DRAM MA translation table.
5-4 (0h)	Row7 DRAM Type. 00 : Standard Fast-Page Mode DRAM. 01 : EDO DRAM. 10 : Reserved. 11 : Synchronous DRAM. These two bits are used to program the DRAM type used on DRAM Row 7.
3-0 (0h)	Row7 DRAM Top Address Boundary - 2. A31-A28 Address Boundary. These four bits are used to combine index-6Eh to decide top memory size for DRAM Row7.

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Register Index : **71h-70h**
Register Name : **PM2BADR - Base Address of ACPI PM2_CNTL Port**
Default Value : 0022h
Attribute : Read/Write
Size : 16 bits

Bit Number	Bit Function
15-0(00h)	Base Address of ACPI PM2_CNTL Port. This 16-bit register is programmed as the I/O base address of ACPI PM2_CNTL Port. The default value is 0022h, and can be programmed by Software to move the base address of ACPI PM2_CNTL Port.

Register Index : **72h**
Register Name : **PM2C - ACPI PM2_CNTL Function.**
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-4 (0h)	Reserved.
3 (0)	Sub-Vendor & Sub-Device ID Registers Programming. 0 : Disable. 1 : Enable. This bit is used to lock the Sub-Vendor & Sub-Device ID register programming. When this bit is enabled, Software can write the data to the Sub-Vendor & Sub-Device ID registers. When this bit is disabled, the Sub-Vendor & Sub-Device ID registers become Read Only.
2 (0)	Delay for I/O Trap Feature. 0 : Disable. 1 : Enable. M1531B will delay all the PCI I/O cycle by one clock when this bit is enabled. The BRDYJ to CPU will delay one clock compared to normal I/O access.
1-0 (0h)	ACPI PM2_CNTL Function. 00 : Disable. 01 : Enable, Pass the ACPI PM2_CNTL Port Access to PCI Bus. 10 : Enable, Not Pass the ACPI PM2_CNTL Port Access to PCI Bus. 11 : Reserved. M1531B has implemented the ACPI PM2_CNTL I/O Port, and the address is defined by Index 71h-70h. When these two bits are programmed to be '00', M1531B will disable the ACPI PM2_CNTL I/O Port decode, and pass the I/O cycle to PCI bus. When these two bits are programmed to be '01', M1531B will snoop the ACPI PM2_CNTL I/O Port write data, and pass the I/O cycle to PCI bus. In this setting, M1531B just do the snoop write, and all the cycle will be terminated by M1533/M1543. When these two bits are programmed to be '10', M1531B will terminate the ACPI PM2_CNTL I/O Port access, and will not pass the I/O cycle to PCI bus.

Register Index : **73h**
Register Name : **Reserved**
Default Value : 00h
Attribute : Read Only

Register Index : **74h**
Register Name : **RFQU - Refresh Queue Control**
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-6 (00h)	Reserved.
5 (0)	SDRAM Speculative read. 0 : Disable 1 : Enable When this bit is enabled, SDRAM will drive the read command before the cycle is fully decoded. If the CPU bus is running at 66 Mhz or below, a '1' is recommended. Otherwise, a '0' is recommended.
4 (0)	Reserved
3 (0)	Fast L2 Write back 0 : Disable 1 : Enable When this bit is enabled, M1531B will perform a fast L2 Write back cycle. A '1' is recommended for best system performance.
2 (0)	Reserved.
1 (0)	PCI to DRAM Speculative Read. 0 : Disable. 1 : Enable. This bit is used to control the PCI to DRAM speculative read. When this bit is enabled, M1531B will read the DRAM data before L1 & L2 snoop result is ready. If the snoop is dirty hit to L1 or L2, the speculative read data will be dropped and get the data from L1 or L2. If the snoop is not dirty hit to L1 or L2, the speculative read data is available. This feature is used to gain the PCI master read performance. This bit is suggested to be enabled during normal operation.
0 (0)	Refresh Queue. 0 : Disable. 1 : Enable. This bit is used to control the DRAM Refresh Queue. M1531B has implemented 4 DRAM Refresh Queue. When DRAM refresh request collides with DRAM bus activity, this DRAM refresh will be delayed until the DRAM bus activity is finished. If the DRAM Refresh Queues are full, the DRAM refresh request becomes the top priority, and the other DRAM bus activity will be delayed.

Register Index : **75h**
Register Name : **Reserved**
Default Value : 00h
Attribute : Read Only

Register Index: **76h**
Register Name : **POD - Programmable Output Driving Strength**
Default Value: 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7 (0)	MWEJ Driving Capability Select. 0 : 12 mA. 1 : 24 mA. This bit controls the strength of the output buffers driving the MWEJ pins.
6 (0)	MAA[1:0]/MAB[1:0] Driving Capability Select. 0 : 12 mA. 1 : 24 mA This bit controls the strength of the output buffers driving the MAA[1:0] and MAB[1:0] pins.
5 (0)	MA[11:2] Driving Capability Select. 0 : 12 mA. 1 : 24 mA. This bit controls the strength of the output buffers driving the MA[11:2] pins.
4 (0)	CASJ[7:0] Driving Capability Select. 0 : 12 mA. 1 : 24 mA. This bit controls the strength of the output buffers driving the CASJ[7:0] pins.
3 (0)	RASJ[5:0] Driving Capability Select. 0 : 12 mA. 1 : 24 mA. This bit controls the strength of the output buffers driving the RASJ[5:0] pins.
2 (0)	RASJ[7:6]/SRASJ[1:0], SCASJ[1:0] Driving Capability Select. 0 : 12 mA. 1 : 24 mA. This bit controls the strength of the output buffers driving the RASJ[7:6]/SRASJ[1:0], SCASJ[1:0] pins.
1 (0)	MD[63:0] and MPD[7:0] Driving Capability Select. 0 : 8 mA. 1 : 6 mA. This bit controls the strength of the output buffers driving the MD[63:0] and MPD[7:0] pins.
0 (0)	HD[63:0] Driving Capability Select. 0 : 8 mA. 1 : 6 mA. This bit controls the strength of the output buffers driving the HD[63:0] pins.

Register Index: **77h**
Register Name : **SUSC - DRAM Suspend Control Register**
Default Value: 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7 (0)	Memory Data Bus Clock Control. 0 : Disable Gated Clock. 1 : Enable Gated Clock. This bit is used to control the internal clock regarding the Memory Data Bus. When this bit is programmed to be '0', the clock never stops. When this bit is programmed to be '1', M1531B will automatically stop the internal clock when there is no Memory Data Bus activity. This bit is suggested to be '0' in desktop application; to be '1' in notebook application to save more power.
6 (0)	DRAM & Cache Controller Clock Control. 0 : Disable Gated Clock. 1 : Enable Gated Clock. This bit is used to control the internal clock regarding the DRAM & Cache Controller. When this bit is programmed to be '0', the clock never stops. When this bit is programmed to be '1', M1531B will automatically stop the internal clock when there is no Host Bus activity. This bit is suggested to be '0' in desktop application; to be '1' in notebook application to save more power.
5 (0)	Host to PCI Interface Logic Clock Control. 0 : Disable Gated Clock. 1 : Enable Gated Clock. This bit is used to control the internal clock regarding the Host to PCI Interface Logic. When this bit is programmed to be '0', the clock never stops. When this bit is programmed to be '1', M1531B will automatically stop the internal clock when there is no Host to PCI activity. This bit is suggested to be '0' in desktop application; to be '1' in notebook application to save more power.
4 (0)	PCI to Host Buffer Clock Control. 0 : Disable Gated Clock. 1 : Enable Gated Clock. This bit is used to control the internal clock regarding the PCI to Host Buffer. When this bit is programmed to be '0', the clock never stops. When this bit is programmed to be '1', M1531B will automatically stop the internal clock when there is no PCI master activity. This bit is suggested to be '0' in desktop application; to be '1' in notebook application to save more power.
3 (0)	DRAM Suspend Self Refresh Mode. 0 : Disable. 1 : Enable. This bit is used to support EDO Self Refresh mode during DRAM suspend. When this bit is enabled, M1531B will issue EDO Self Refresh timing during DRAM Suspend.
2-1 (00)	DRAM Suspend Refresh Period. 00 : 15 us. 01 : 30 us. 10 : 60 us. 11 : 120 us. These 2 bits define the DRAM suspend refresh period.
0 (0)	CLKRUNJ/SERRJ Function Select. 0 : SERRJ. 1 : CLKRUNJ. This bit is used to define the CLKRUNJ/SERRJ pin function. When this bit is programmed to '0', SERRJ function is selected. In this configuration, M1531B can support DRAM ECC/PARITY and the PCI Parity check error report. When this bit is programmed to '1', CLKRUNJ function is selected. M1531B can support Mobile PCI Specification 2.0 CLKRUNJ function through this configuration.

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Register Index : **7Fh-78h**
Register Name : **Reserved**
Default Value : 00h
Attribute : Read Only

Register Index : **80h**
Default Value : 00h
Attribute : Read/Write

Bit Number	Bit Function
7 (0)	MA output LATCH 0 : MA latch. 1 : MA don't latch. M1531B has two ways to drive MA bus. When this bit is reset as '0', M1531B will drive MA bus through a latch to avoid MA bus glitch since MA bus is decoded directly from CPU address or write buffer address. In this mode, M1531B will drive MA bus at the beginning of T3. When this bit is set as '1', M1531B will drive MA bus directly through the decoding circuit. In this mode, MA will drive earlier. A '1' is recommended in normal operation.
6-3 (0h)	Reserved.
2	RASJ asserted point in ROW Miss Cycle 0 : T3 End 1 : T2 End This bit is used to control the RASJ assertion point in Row miss cycle. A '1' recommended in normal operation for best system performance
1-0 (0h)	Reserved.

Register Index : **81h**
Default Value : 00h
Attribute : Read/Write

Bit Number	Bit Function
7 (0)	DRAM Pipe Read falling change MA for next line 0 : Disable 1 : Enable When this bit is enabled, M1531B will change MA early half clock in DRAM. A '1' is recommended in normal operation for best reliability.
6-1 (00h)	Reserved.
0	Refresh function 0 : Enable 1 : Disable

Register Index : **83h**
Default Value : 00h
Attribute : Read/Write

Bit Number	Bit Function
4 (0)	SDRAM command drive 2T in high frequency bus 0 : Disable 1 : Enable When this bit is enabled, SDRAM command will drive 2T instead of 1T in high SDRAM bus frequency. If SDRAM bus is running at 66 Mhz or below, a '0' is recommended. Otherwise, a '1' is recommended.

Register Index : **FFh-84h**
Register Name : **Reserved**
Default Value : 00h
Attribute : Read Only

III. ACPI PM2_CNTL I/O Port

Register Name : **PM2_CNTL - ACPI PM2_CNTL I/O Port**
I/O Address : **0000h - FFFFh Movable**
Default Value : 00h
Attribute : Read/Write
Size : This register must be 8-bit I/O access.

Bit Number	Bit Function
7-1 (00h)	Reserved.
0 (0)	PCI Master Arbiter Function. 0 : Enable. 1 : Disable. This bit is used to control the PCI Master Arbiter Function. When this bit is set to be '1', the M1531B internal PCI master arbiter will be disabled, and the M1531B on behalf of the CPU host is the only one master in the system. In normal operation, the bit must be set to '0'.

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Section 5 : Hardware and Software Programming Guide

5.1 Hardware Setup Table :

The M1531B will strobe the hardware setting value in the respective registers when the RSTJ goes inactive. BIOS can utilize the register value to save the software programming time to detect L2 type, size, and the bus frequency. For notebook applications, it is recommended to use software programming to reduce power consumption since the pull-up and pull-down resistors will continuously consume system power. If the BIOS wants to utilize the hardware setting value, the system board designer must make sure the strobing value is identical to their definition. Otherwise, the software programming must be used to detect the hardware configuration.

Pin Name	Description	Pull-up	Pull-down	Register	Note
HA[31..27]	Cache module detect bits	—	—	Index-52h bits[7:3]	(1)
HA[26..25]	Indicate host frequency	—	—	Index-52h bits[2:1]	(2)
HA24	L2 cache bank select	1-bank	2-bank	Index-41h bit[7]	
HA[22..21]	Cache size detect	—	—	Index-41h bits[2:1]	(3)

Note : (1) Please refer to cache module specification for detailed setting or the system designer can define their own meaning.

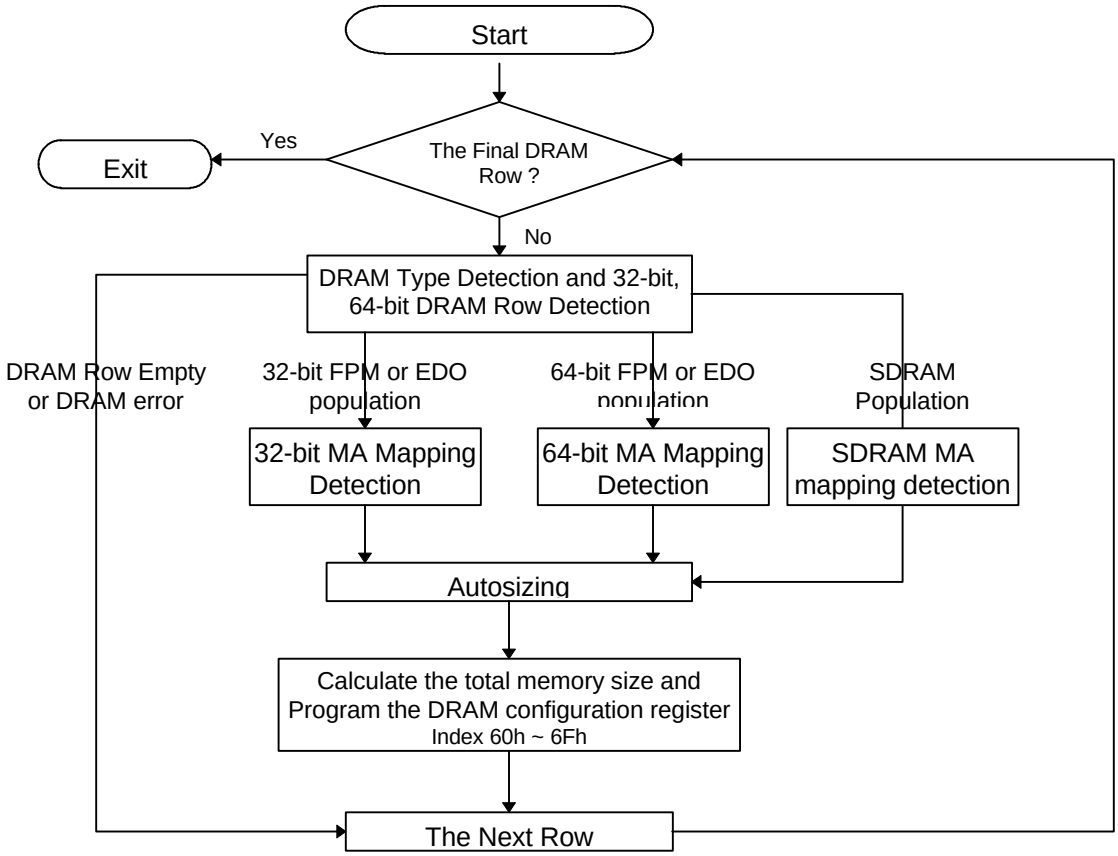
(2)

HA26	HA25	Host frequency
0	0	60 MHz
0	1	66 MHz
1	0	75 MHz
1	1	83 MHz

(3)

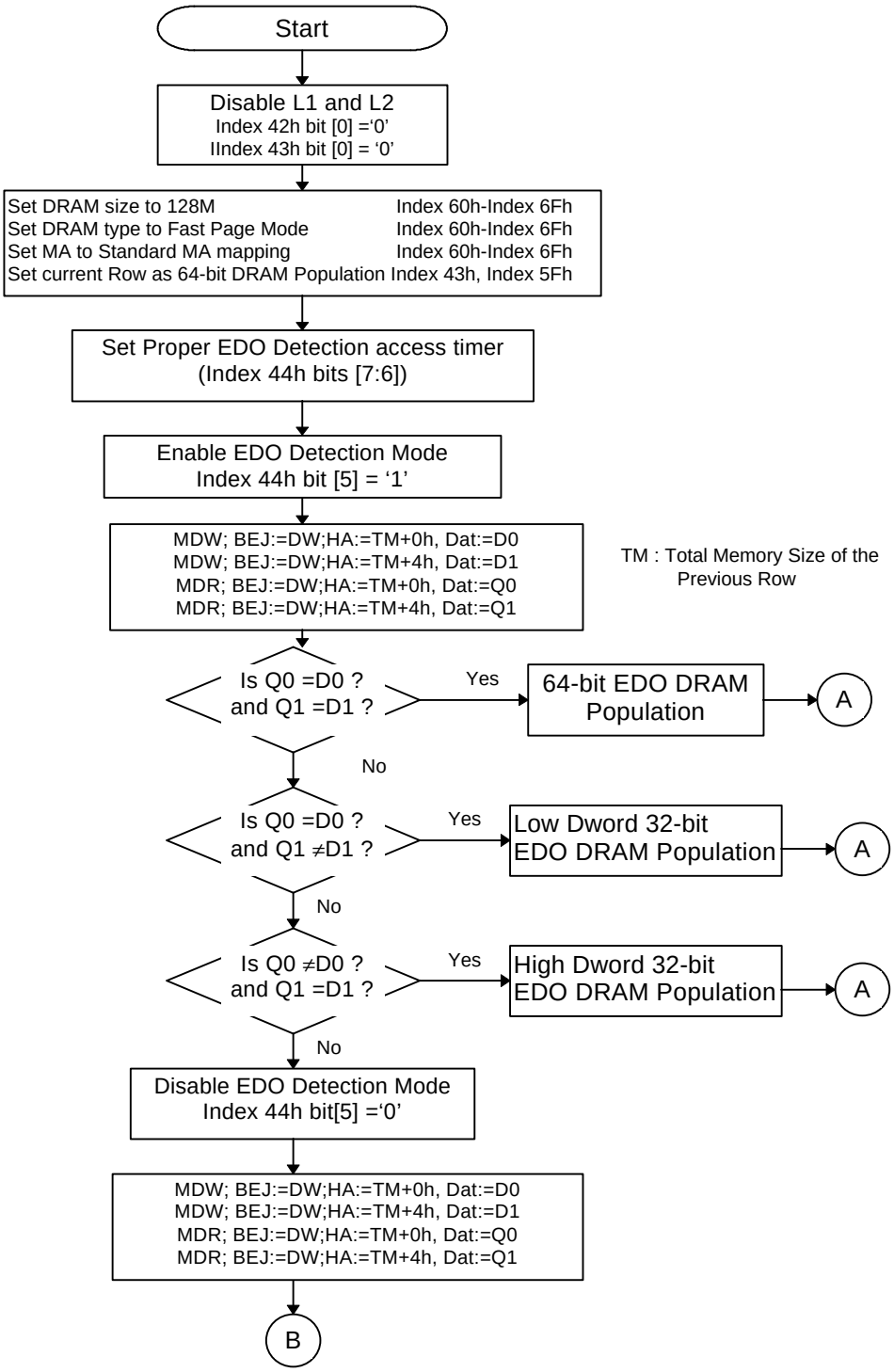
HA22	HA21	Cache size
0	0	None
0	1	256KB
1	0	512KB
1	1	1MB

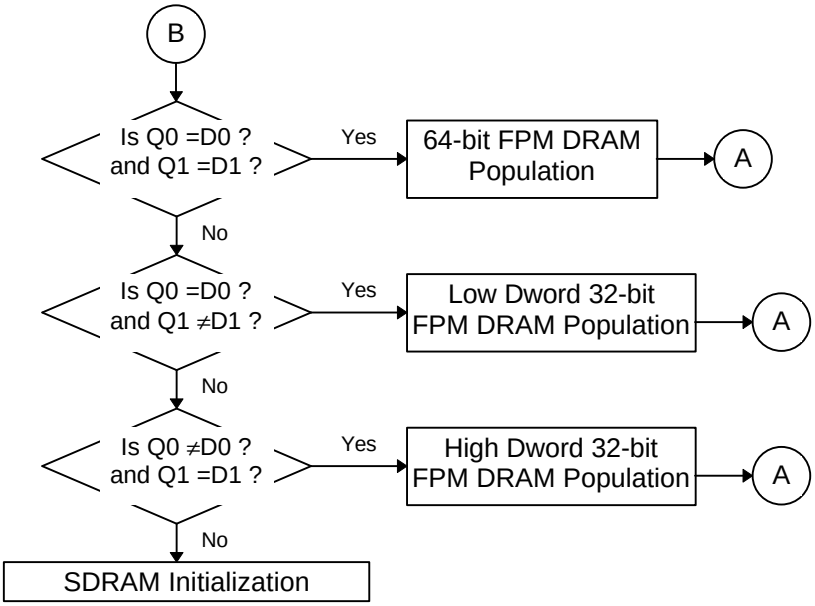
5.2 DRAM Detection Flow :

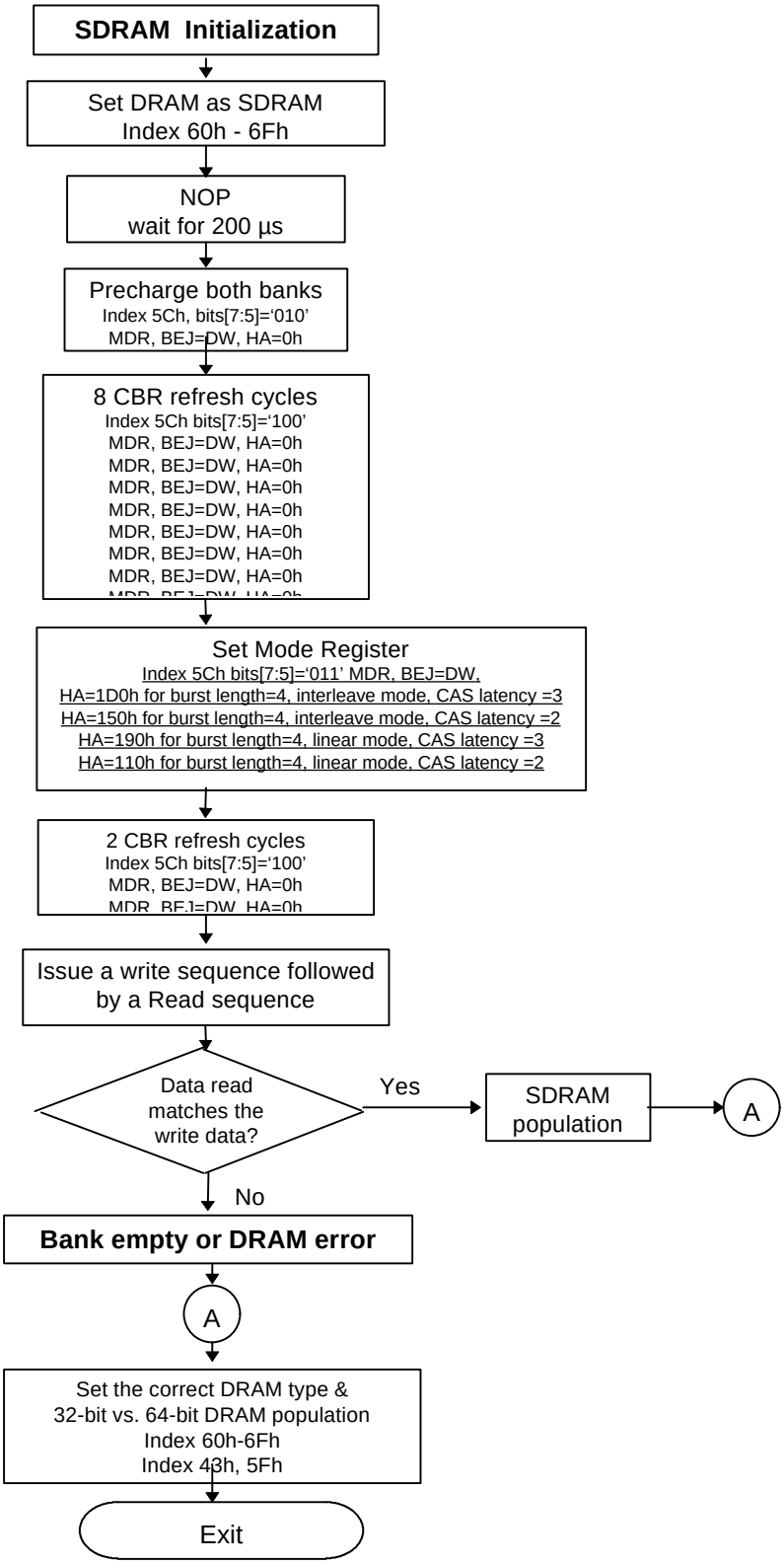


The “DRAM Detection Flow” is a row-by-row basis algorithm. The flow starts from Row 0 and then up to the final row depending on the motherboard configuration. The “DRAM Type Detection” is used to detect the DRAM type including Fast Page Mode (FPM) DRAM, EDO and SDRAM. The “32-bit or 64-bit DRAM Row Detection” is used to detect the 32-bit or 64-bit DRAM Population on this Row. The M1531B supports 32-bit DRAM Population, the MA table will be different. The 32-bit or 64-bit MA Mapping Detection is used to detect the MA mapping as the standard or 64MB or 1Mx16 or 2M x8 (12x9). The “Autosizing” is used to detect the Row size. The M1531B can support from 2MB to 128MB per Row.

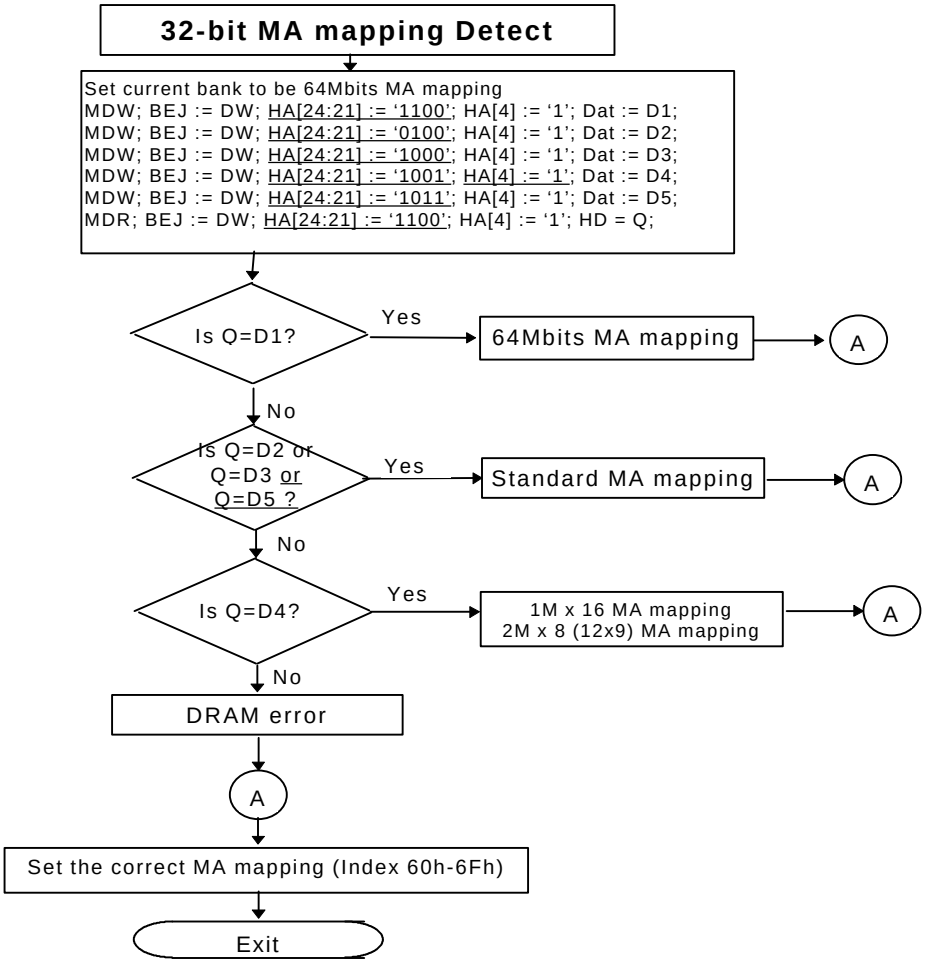
5.2.1 DRAM Type Detection and 32-bit vs.64-bit Row Detect :




B
Is Q0 =D0 ?
and Q1 =D1 ?
Yes
64-bit FPM DRAM
Population
A
No
Is Q0 =D0 ?
and Q1 ≠D1 ?
Yes
Low Dword 32-bit
FPM DRAM Population
A
No
Is Q0 ≠D0 ?
and Q1 =D1 ?
Yes
High Dword 32-bit
FPM DRAM Population
A
No
SDRAM Initialization


SDRAM Initialization
Set DRAM as SDRAM
Index 60h - 6Fh
NOP
wait for 200 µs
Precharge both banks
Index 5Ch, bits[7:5]='010'
MDR, BEJ=DW, HA=0h
8 CBR refresh cycles
Index 5Ch bits[7:5]='100'
MDR, BEJ=DW, HA=0h
MDR, BEJ=DW, HA=0h
MDR, BEJ=DW, HA=0h
MDR, BEJ=DW, HA=0h
MDR, BEJ=DW, HA=0h
MDR, BEJ=DW, HA=0h
MDR, BEJ=DW, HA=0h
Set Mode Register
Index 5Ch bits[7:5]='011' MDR, BEJ=DW,
HA=1D0h for burst length=4, interleave mode, CAS latency =3
HA=150h for burst length=4, interleave mode, CAS latency =2
HA=190h for burst length=4, linear mode, CAS latency =3
HA=110h for burst length=4, linear mode, CAS latency =2
2 CBR refresh cycles
Index 5Ch bits[7:5]='100'
MDR, BEJ=DW, HA=0h
Issue a write sequence followed
by a Read sequence
Data read
matches the
write data?
Yes
SDRAM
population
A
No
Bank empty or DRAM error
A
Set the correct DRAM type &
32-bit vs. 64-bit DRAM population
Index 60h-6Fh
Index 43h, 5Fh
Exit

5.2.2 32-bit MA Mapping Detection



	Din	D1	D2	D3	D4	D5		
	Command	MDW	MDW	MDW	MDW		MDR	Dout
	MA Row	800	000	800	800	C00	800	Q
	Column	500	500	100	300	300	500	
64Mb	12x12 Row	800	000	800	800	C00	800	D1
	Column	500	500	100	300	300	500	
	12x11 Row	800	000	800	800	C00	800	D1
	Column	500	500	100	300	300	500	
	11x11 Row	000	000	000	000	400	000	D2
	Column	500	500	100	300	300	500	
STD	12x10 Row	800	000	800	800	C00	800	D3
	Column	100	100	100	300	300	100	
	11x11 Row	000	000	000	000	400	000	D2
	Column	500	500	100	300	300	500	
	11x10 Row	000	000	000	000	400	000	D3
	Column	100	100	100	300	300	100	
	10x10 Row	000	000	000	000	000	000	D3
	Column	100	100	100	300	300	100	
	10x9 Row	000	000	000	000	000	000	D5
	Column	100	100	100	100	100	100	
1Mx16	12x8 Row	800	000	800	800	C00	800	D4
	Column	000	000	000	000	000	000	
2Mx8	12x9 Row	800	000	800	800	C00	800	D4
	Column	100	100	100	100	100	100	

32-bit bank DRAM Address Translation Table

MA[11:0]	11	10	9	8	7	6	5	4	3	2	1	0
Row	A23/A24	A22	A11	A20	A19	A18	A17	A16	A15	A14	A13	A12
Column	A25	A23	A21	A4	A10	A9	A8	A7	A6	A5	(A2)	A3

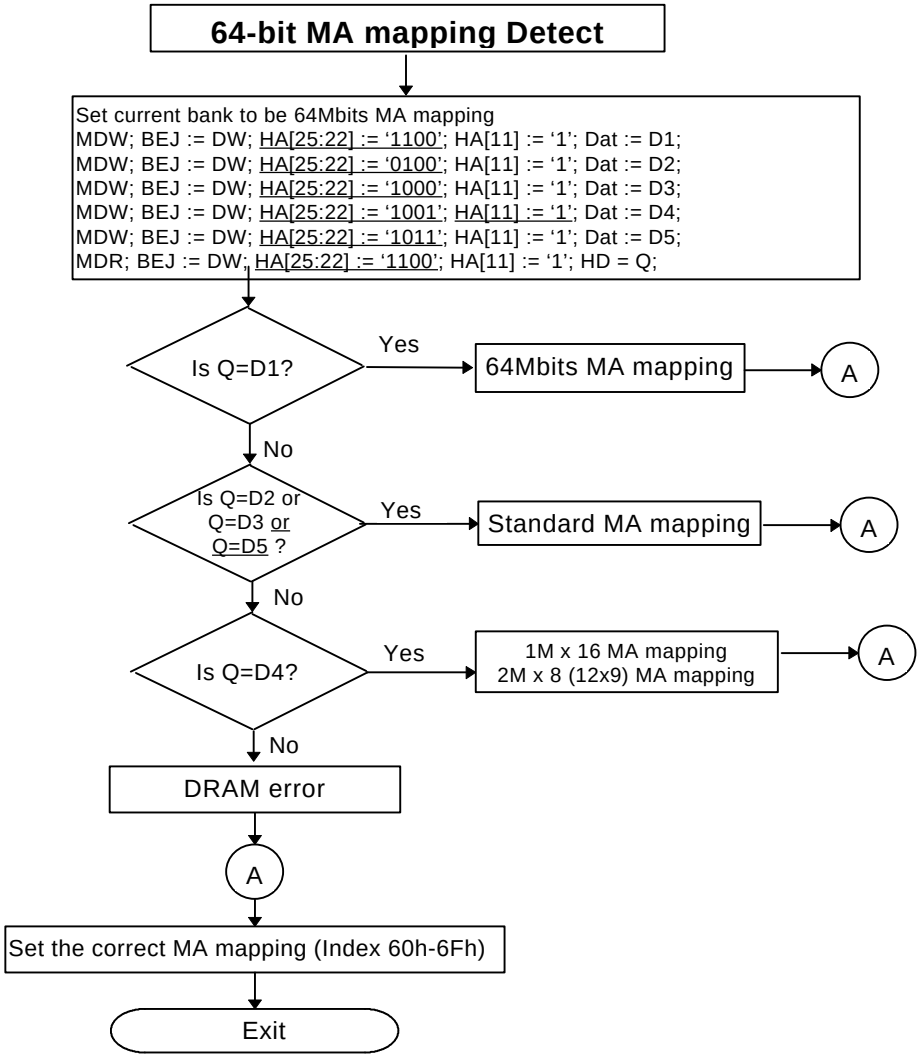
Row MA[11] : if 64Mbits DRAM is not populated, then A23 is driven; if 64Mbits DRAM is populated, then A24 is driven

32-bit Bank 1M x 16, 2M x 8 DRAM Address Translation Table

MA[11:0]	11	10	9	8	7	6	5	4	3	2	1	0
Row	A10	A21	A11	A20	A19	A18	A17	A16	A15	A14	A13	A12
Column				A22	A4	A9	A8	A7	A6	A5	(A2)	A3

Address Size = 12 x 8, 12 x 9

5.2.3 64-bit MA Mapping Detection



	Din	D1	D2	D3	D4	D5		
	Command	MDW	MDW	MDW	MDW		MDR	Dout
	MA	800	000	800	800	C00	800	Q
		500	500	100	300	300	500	
64Mb	12x12	800	000	800	800	C00	800	D1
		500	500	100	300	300	500	
	12x11	800	000	800	800	C00	800	D1
		500	500	100	300	300	500	
	11x11	000	000	000	000	400	000	D2
		500	500	100	300	300	500	
STD	12x10	800	000	800	800	C00	800	D3
		100	100	100	300	300	100	
	11x11	000	000	000	000	400	000	D2
		500	500	100	300	300	500	
	11x10	000	000	000	000	400	000	D3
		100	100	100	300	300	100	
	10x10	000	000	000	000	000	000	D3
		100	100	100	300	300	100	
	10x9	000	000	000	000	000	000	D5
		100	100	100	100	100	100	
1Mx16	12x8	800	000	800	800	C00	800	D4
		000	000	000	000	000	000	
2Mx8	12x9	800	000	800	800	C00	800	D4
		100	100	100	100	100	100	

Normal DRAM Address Translation Table

MA[11:0]	11	10	9	8	7	6	5	4	3	2	1	0
Row	A24/25	A23	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12
Column	A26	A24	A22	A11	A10	A9	A8	A7	A6	A5	A4	A3

Row MA[11] : If 64Mbits DRAM is not populated, then A24 is driven; if 64Mbits DRAM is populated, then A25 is driven

1M x 16, 2M x 8 DRAM Address Translation Table

Specific DRAM Address Translation Table for Asymmetric 1M x 16

MA[11:0]	11	10	9	8	7	6	5	4	3	2	1	0
Row	A22	A21	A11	A20	A19	A18	A17	A16	A15	A14	A13	A12
Column				A23	A10	A9	A8	A7	A6	A5	A4	A3

Address Size = 12 x 8, 12 x 9

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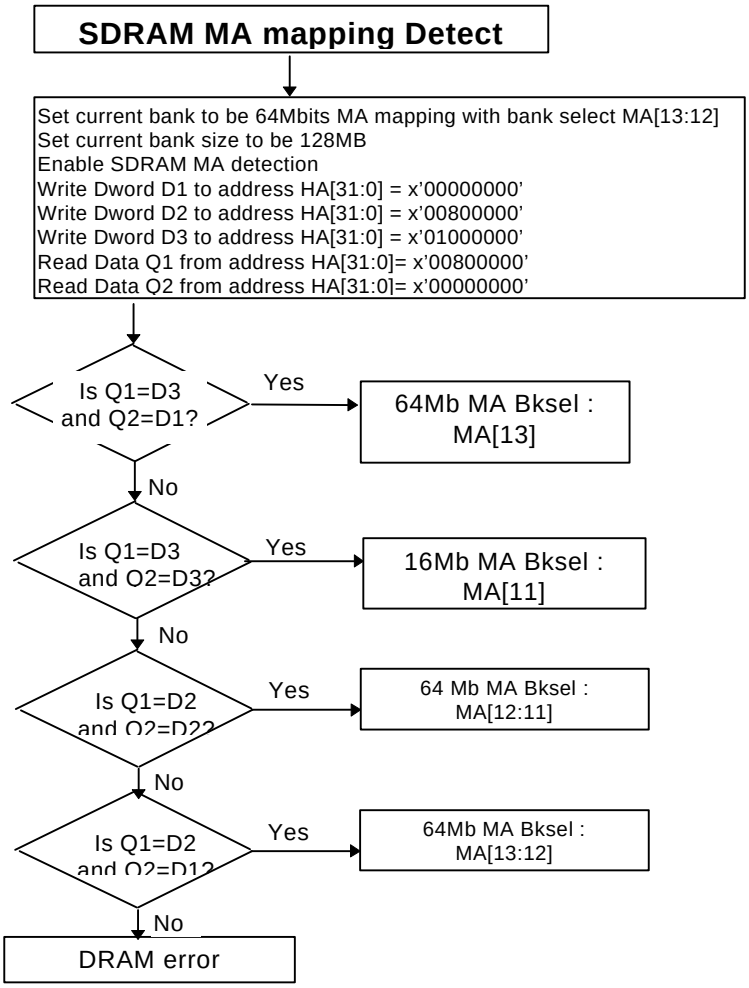
5.2.4 Synchronous DRAM MA Mapping and Bank Select Detection



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	Data	D1	D2	D3	Q1		Q2	
	Command	MDW	MDW	MDW	MDR	Dout	MDR	Dout
	MA[13:6]	0000-0000	1000-0000	0100-0000	1000-0000		0000-0000	
		0000-0000	1000-0000	0100-0000	1000-0000		0000-0000	
64Mb	13x10	0000-0000	0010-0000	0100-0000	xxxx-xxxx	D3	0000-0000	D1
		0xx0-0000	0xx0-0000	0xx0-0000	0xx0-0000		0xx0-0000	
	13x9	0000-0000	0010-0000	0100-0000	xxxx-xxxx	D3	0000-0000	D1
		0xx0-x000	0xx0-x000	0xx0-x000	0xx0-x000		0xx0-x000	
	13x8	0000-0000	0010-0000	0100-0000	xxxx-xxxx	D3	0000-0000	D1
		0xx0-xx00	0xx0-xx00	0xx0-xx00	0xx0-xx00		0xx0-xx00	
	12x8	0x00-0000	0x10-0000	0x00-0000	xxxx-xxxx	D3	0x00-0000	D1
		0xx0-xx00	0xx0-xx00	0xx0-xx00	0xx0-xx00		0xx0-xx00	
	11x9	xx00-0000	xx00-0000	xx00-0000	xxxx-xxxx	D3	xx00-0000	D3
		xx00-x000	xx00-x000	xx00-x000	xx00-x000		xx00-x000	
	12x10	0000-0000	0010-0000	0100-0000	xxxx-xxxx	D2	0000-0000	D1
		00x0-0000	00x0-0000	01x0-0000	00x0-0000		00x0-0000	
	12x9	0000-0000	0010-0000	0100-0000	xxxx-xxxx	D2	0000-0000	D1
		00x0-x000	00x0-x000	01x0-x000	00x0-x000		00x0-x000	
	12x8	0000-0000	0010-0000	0100-0000	xxxx-xxxx	D2	0000-0000	D1
		00x0-xx00	00x0-xx00	01x0-xx00	00x0-xx00		00x0-xx00	
	11x10	x000-0000	x000-0000	x010-0000	xxxx-xxxx	D2	x000-0000	D2
		x000-0000	x000-0000	x010-0000	x000-0000		x000-0000	
	11x9	x000-0000	x000-0000	x010-0000	xxxx-xxxx	D2	x000-0000	D2
		x000-x000	x000-x000	x010-x000	x000-x000		x000-x000	
	11x8	x000-0000	x000-0000	x010-0000	xxxx-xxxx	D2	x000-0000	D2
		x000-xx00	x000-xx00	x010-xx00	x000-xx00		x000-xx00	
16Mb	11x10	xx00-0000	xx00-0000	xx00-0000	xxxx-xxxx	D3	xx00-0000	D3
		xx00-0000	xx00-0000	xx00-0000	xx00-0000		xx00-0000	
	11x9	xx00-0000	xx00-0000	xx00-0000	xxxx-xxxx	D3	xx00-0000	D3
		xx00-x000	xx00-x000	xx00-x000	xx00-x000		xx00-x000	
	11x8	xx00-0000	xx00-0000	xx00-0000	xxxx-xxxx	D3	xx00-0000	D3
		xx00-xx00	xx00-xx00	xx00-xx00	xx00-xx00		xx00-xx00	

64Mbits(2bank, 4bank)

MA[11:0]	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Row	A23	A24	A11	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12
Column	A23	A24	A11	L	A26	A25	A10	A9	A8	A7	A6	A5	A4	A3

64Mbits (4bank)

MA[11:0]	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Row	X	A23	A11	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12
Column	X	A23	A11	L	A25	A24	A10	A9	A8	A7	A6	A5	A4	A3

16Mbits (2bank); 64Mbits(2bank)

MA[11:0]	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Row	X	X	A11	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12
Column	X	X	A11	L	A24	A23	A10	A9	A8	A7	A6	A5	A4	A3

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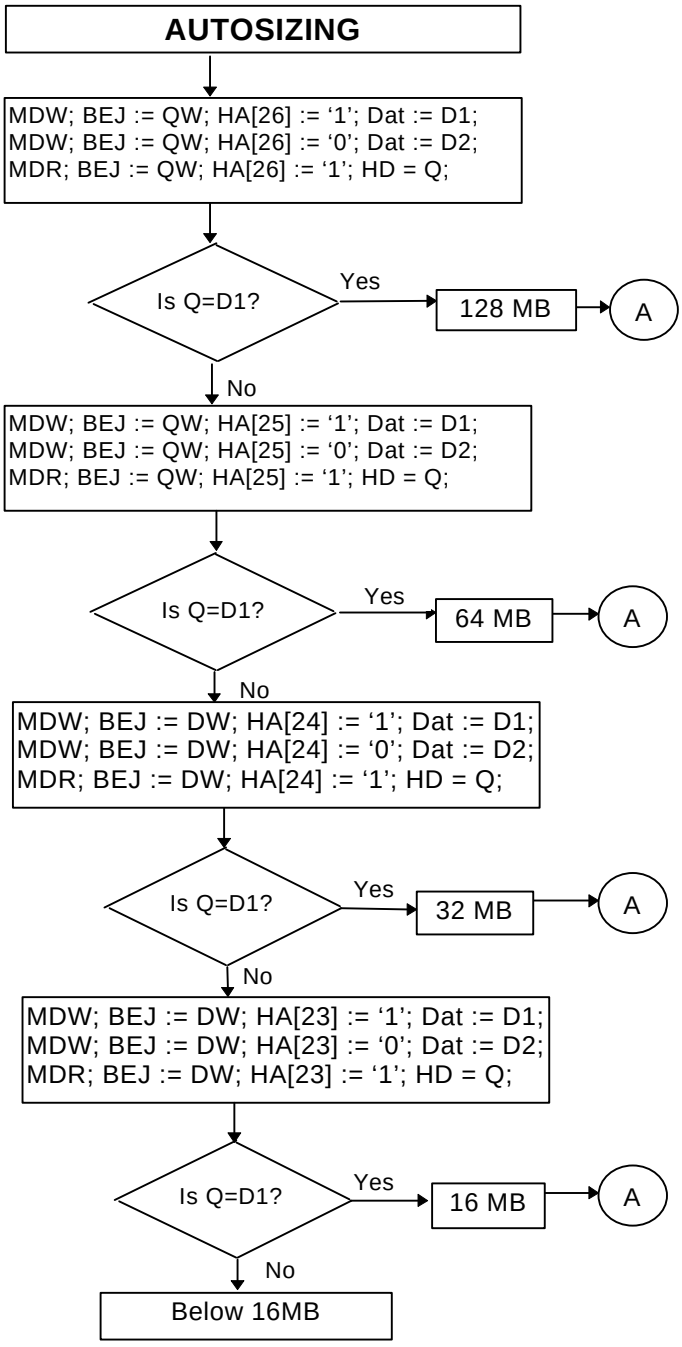
5.2.5 DRAM Autosizing



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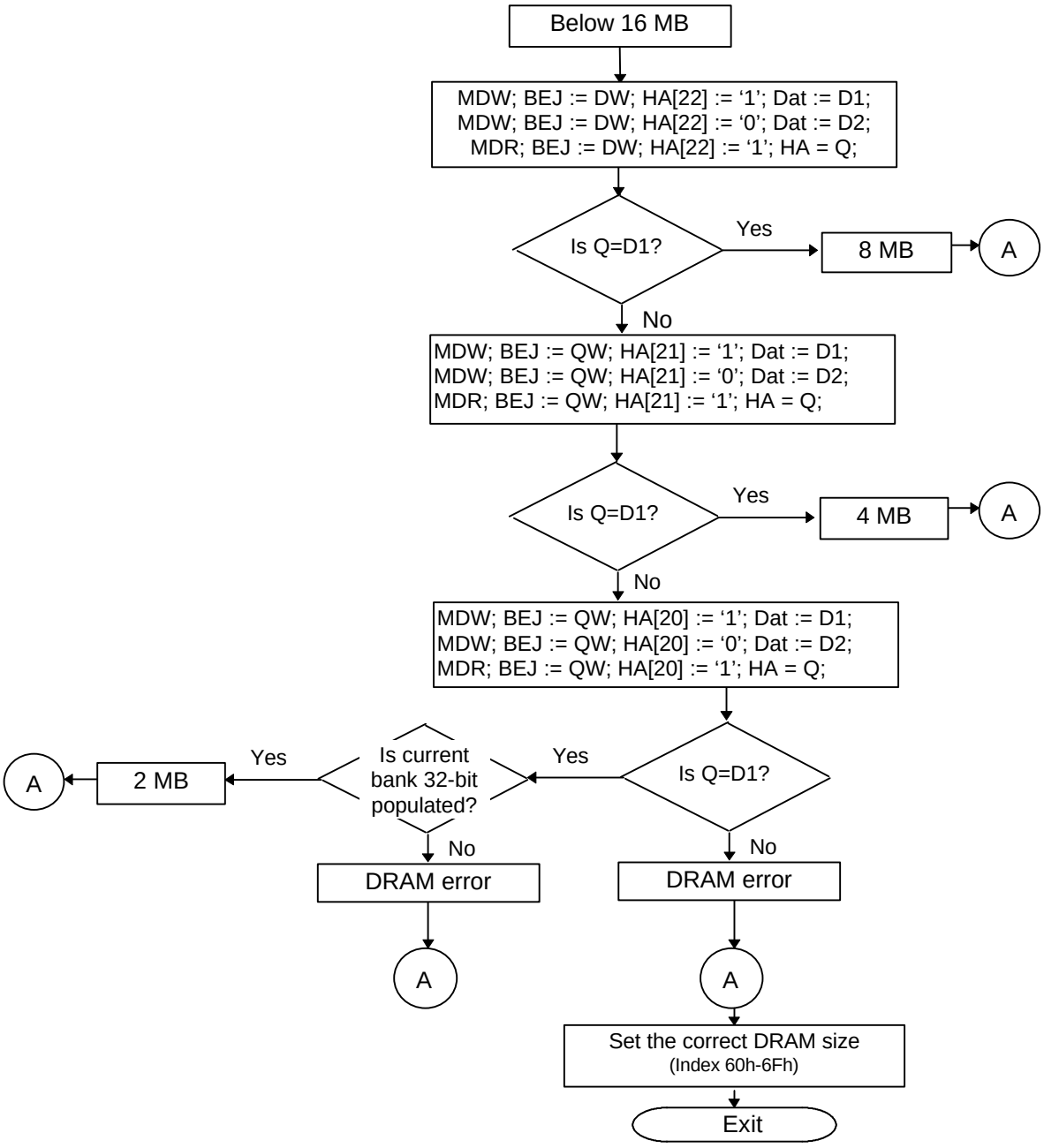
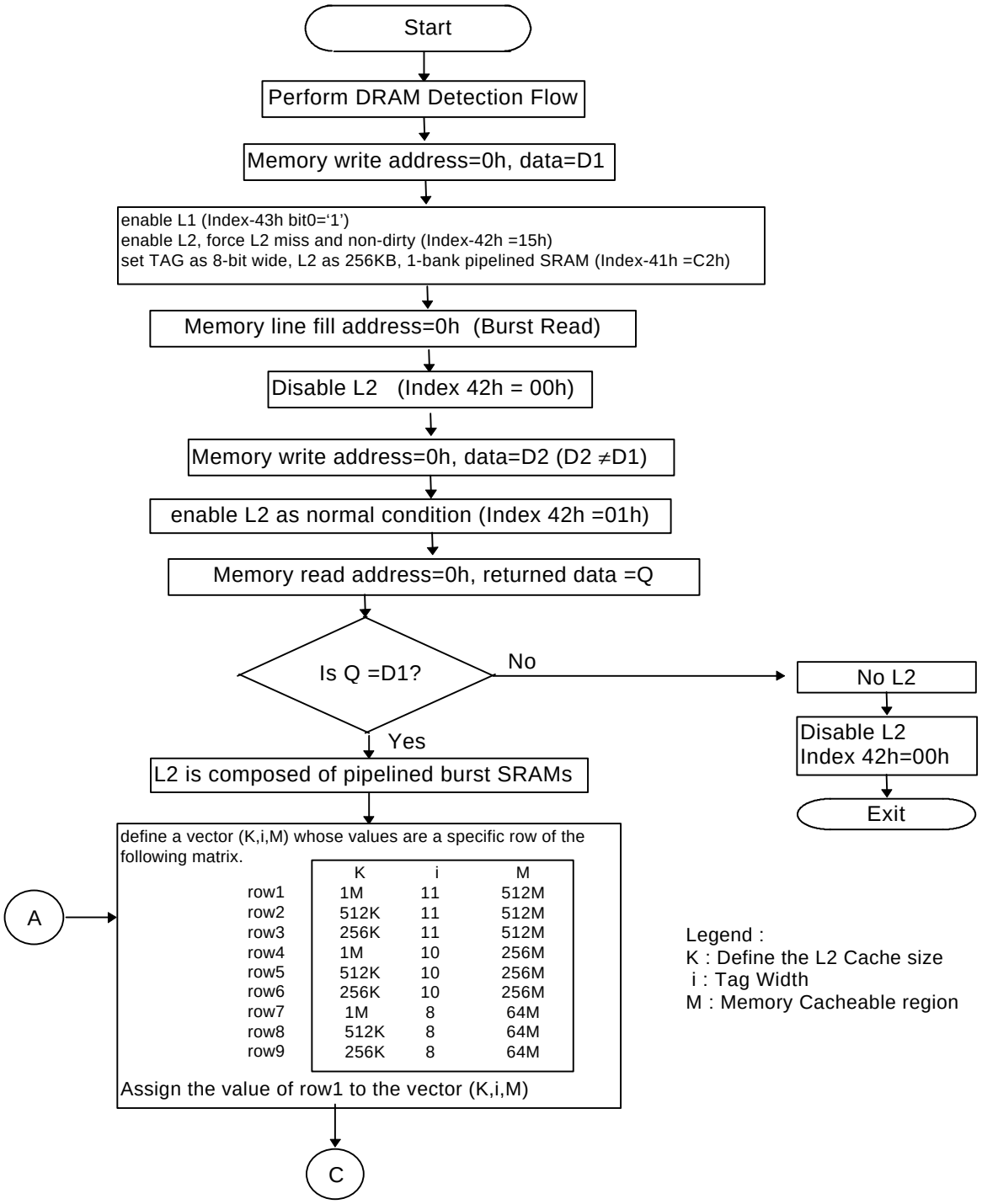
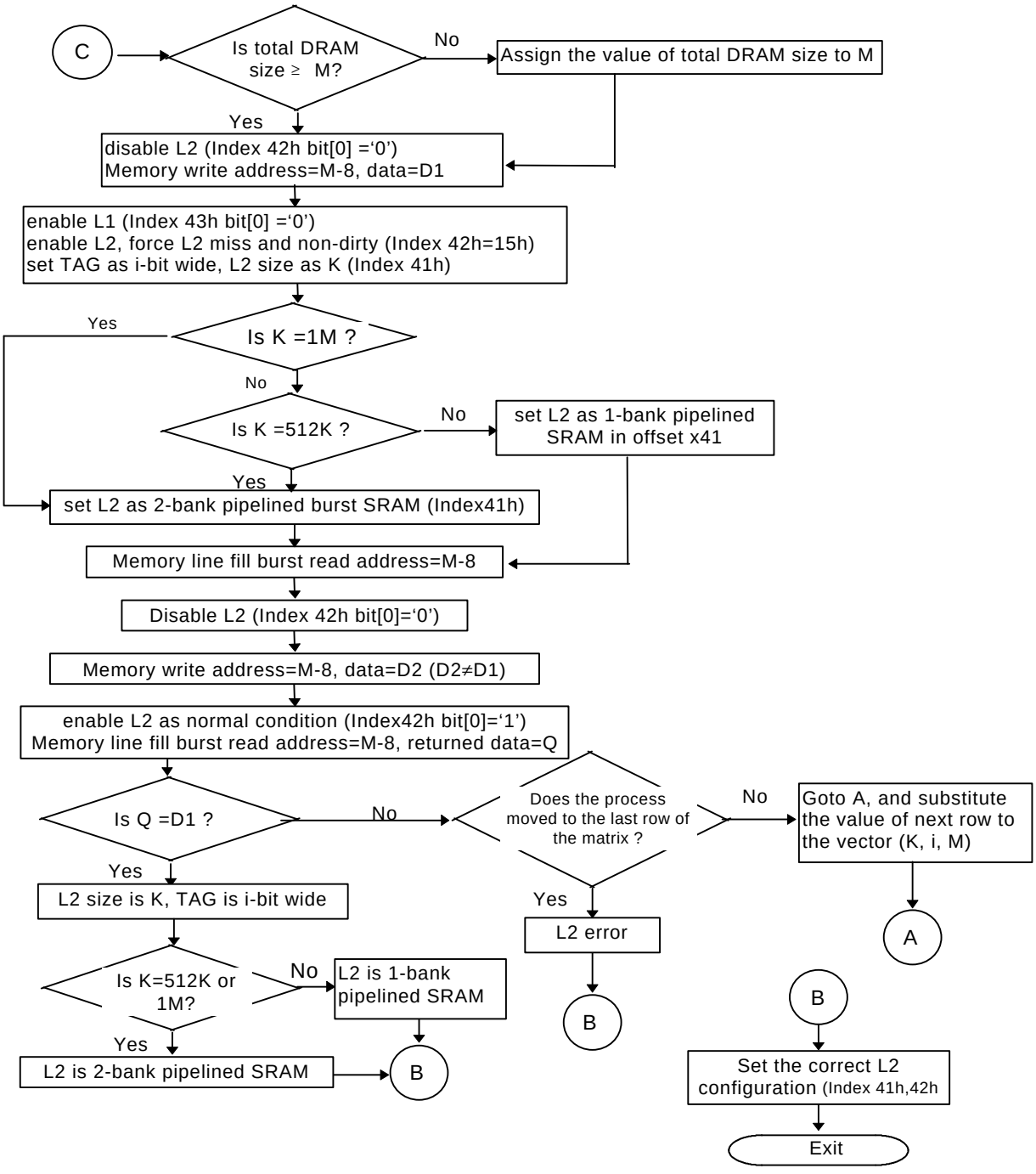
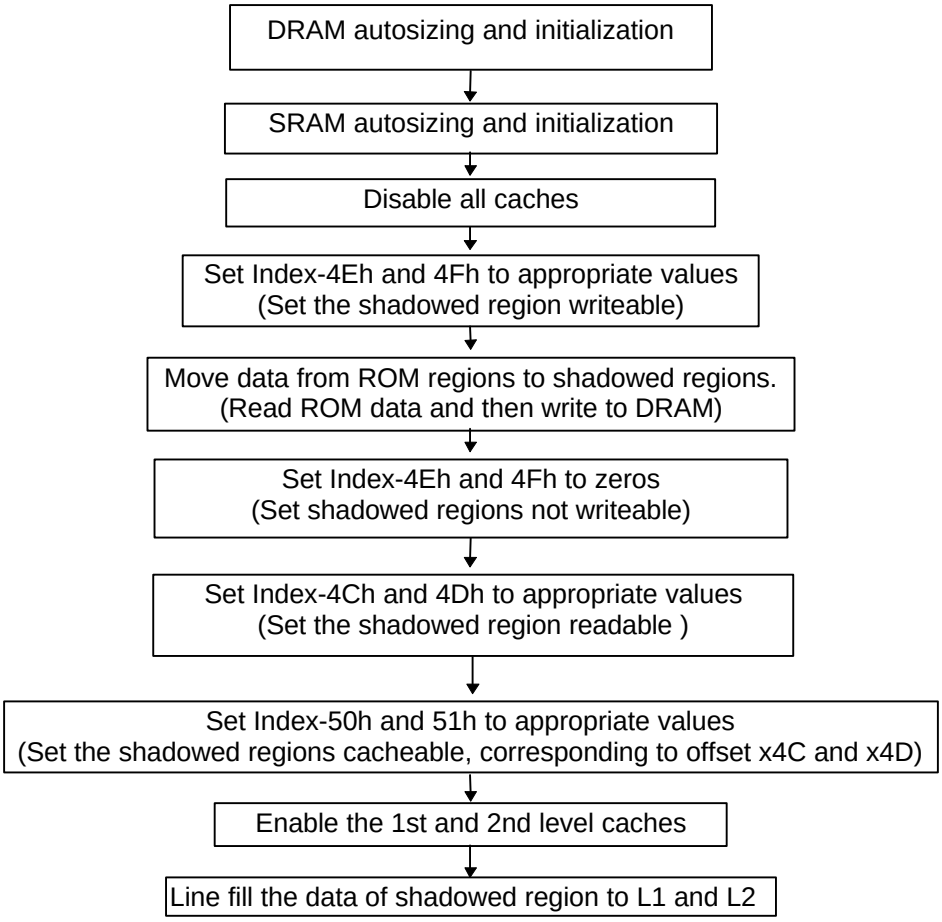

Below 16 MB
MDW; BEJ := DW; HA[22] := '1'; Dat := D1;
MDW; BEJ := DW; HA[22] := '0'; Dat := D2;
MDR; BEJ := DW; HA[22] := '1'; HA = Q;
Is Q=D1?
Yes
8 MB
A
No
MDW; BEJ := QW; HA[21] := '1'; Dat := D1;
MDW; BEJ := QW; HA[21] := '0'; Dat := D2;
MDR; BEJ := QW; HA[21] := '1'; HA = Q;
Is Q=D1?
Yes
4 MB
A
No
MDW; BEJ := QW; HA[20] := '1'; Dat := D1;
MDW; BEJ := QW; HA[20] := '0'; Dat := D2;
MDR; BEJ := QW; HA[20] := '1'; HA = Q;
Is Q=D1?
Yes
Is current bank 32-bit populated?
Yes
2 MB
A
No
DRAM error
A
No
DRAM error
A
Set the correct DRAM size
(Index 60h-6Fh)
Exit

5.3 L2 Cache Autosizing Flowchart




C
Is total DRAM size ≥ M?
No
Assign the value of total DRAM size to M
Yes
disable L2 (Index 42h bit[0] ='0')
Memory write address=M-8, data=D1
enable L1 (Index 43h bit[0] ='0')
enable L2, force L2 miss and non-dirty (Index 42h=15h)
set TAG as i-bit wide, L2 size as K (Index 41h)
Yes
Is K =1M ?
No
Is K =512K ?
No
set L2 as 1-bank pipelined SRAM in offset x41
Yes
set L2 as 2-bank pipelined burst SRAM (Index41h)
Memory line fill burst read address=M-8
Disable L2 (Index 42h bit[0]='0')
Memory write address=M-8, data=D2 (D2≠D1)
enable L2 as normal condition (Index42h bit[0]='1')
Memory line fill burst read address=M-8, returned data=Q
Is Q =D1 ?
No
Does the process moved to the last row of the matrix ?
No
Goto A, and substitute the value of next row to the vector (K, i, M)
Yes
L2 size is K, TAG is i-bit wide
Yes
L2 error
A
Is K=512K or 1M?
No
L2 is 1-bank pipelined SRAM
B
B
Yes
L2 is 2-bank pipelined SRAM
B
Set the correct L2 configuration (Index 41h,42h
Exit

5.4 Enable Shadow Region



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5.5 Software MESI Test

M1531B integrates an 8K by2 MESI SRAM. Before the chips are shipped out, the RAM cells are tested meticulously. However, for system board debugging and troubleshooting, M1531B has a software test mode for testing internal MESI-SRAM cells. System makers can probe the internal RAM cell by this software scheme, and the BIOS writer is suggested to do so. The procedure is illustrated as below :

1. Initialize :
   - Set index-41h bits [7:6] = '11' (Set PBSRAM)
   - Set index-41h bit [4] = '1' (Enable MESI Software Test Mode)
   - Set index-41h bits [2:1] = '01' (Set Cache size 256K)
   - Set index-41h bit [0] = '0' (Set 8-Bit Tag)

2. Write/Read RAM cell via memory write/read command.

   Write SRAM cell :
   Command : Memory Data Write
   Address : HA[15:5] as RAM address, HA[31:17] as don't care
   Data : HD[7:0] as RAM write data.

   Read SRAM cell :
   Command : Memory Data Read
   Address : HA[15:5] as RAM address, HA[31:17] as don't care
   Data : HD[63:0] as don't care.
   Read Index-53h bits 7-0 for read data.

When the M1531B is set to the internal MESI-RAM software test mode, only the CPU Memory-Code-Read/Write cycles can be passed to (access) the system memory. Memory-Data-Read/Write cycles are used to access internal MESI-RAM.

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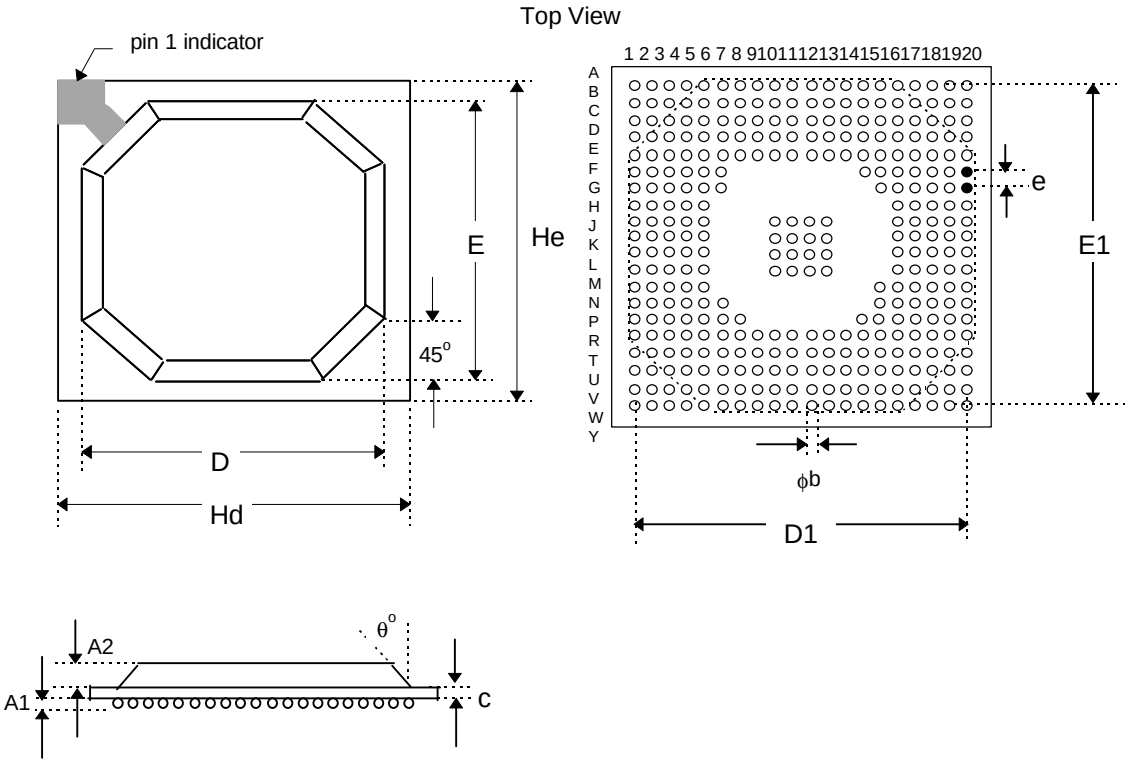
Section 6 : Packaging Information

328L BGA Dimension Spec (27 x 27 mm)



Symbol	Min.	Nom.	Max.
A1	0.55	0.60	0.65
A2	1.12	1.17	1.22
ϕb	0.60	0.75	0.90
c	0.51	0.56	0.61
D	23.80	24.00	24.20
D1	23.93	24.13	24.33
E	23.80	24.00	24.20
E1	23.93	24.13	24.33
e		1.27	
Hd	26.80	27.00	27.20
He	26.80	27.00	27.20
θ°	23°	30°	37°
Y (radius of ball)			0.25

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Section 7 : Revision History

Note : Text in shaded areas or underlined indicate differences with previous version.

p.49,62	05/26/97
p.91,92	05/29/97
P.84,91-93	06/11/97

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Subject: **M1531B and DRAM Implementation**

Date: **March 6, 1997**

Part & Version: **M1531B**

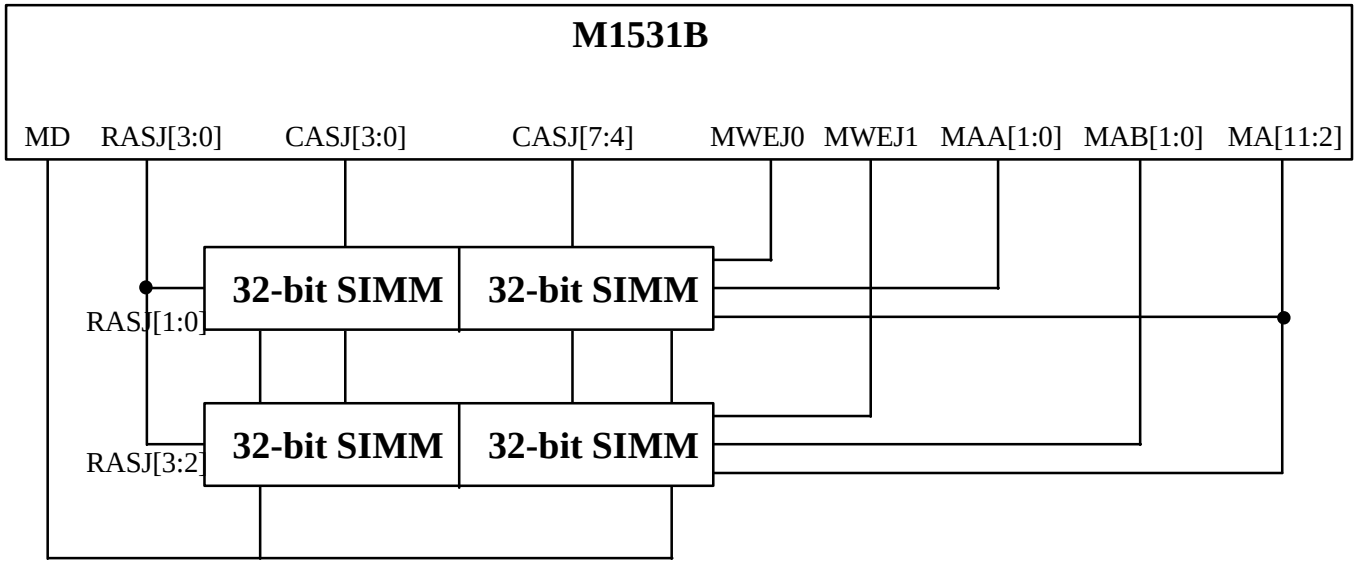
Prepared by: **Bruce Hsueh**

Approved by: **Charles Chiang**

1. The pinout difference between M1531 & M1531B:

Pinout	M1531	M1531B
U15	MAB1	MAB1/MA13
U14	MAB0	MAB0/MA12
V20	RASJ5	RASJ5/TIO9
U18	RASJ4	RASJ4/TIO10
Y20	NC	TIO8
T17	TIO10/MWEJ1/MKREFRQJ	MWEJ1
T16	TIO9/SRASJ1	SRASJ1
T15	TIO8/SCASJ1	SCASJ1

2. SIMM x 4 implementation :



2 Double-Sided DRAM Bank (EDO/FPM)

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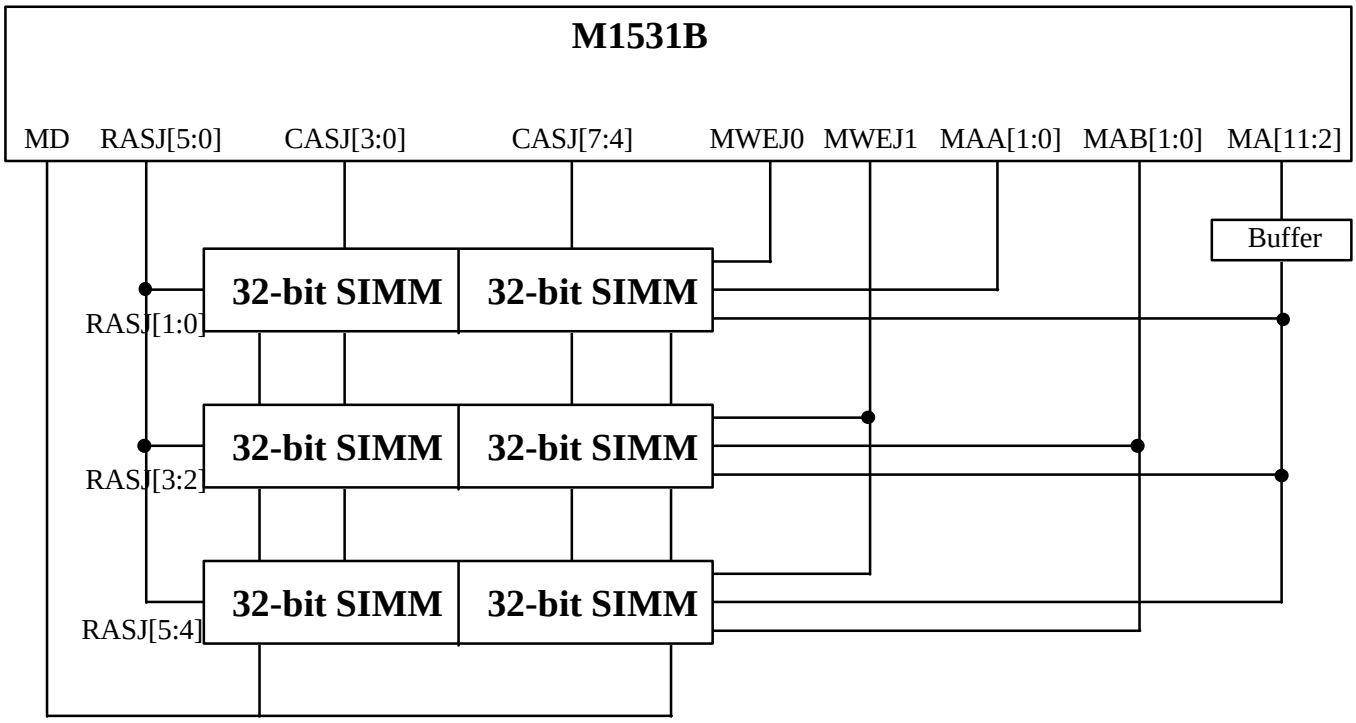
3. SIMM x 6 implementation:



3 Double-Sided DRAM Bank (EDO/FPM)

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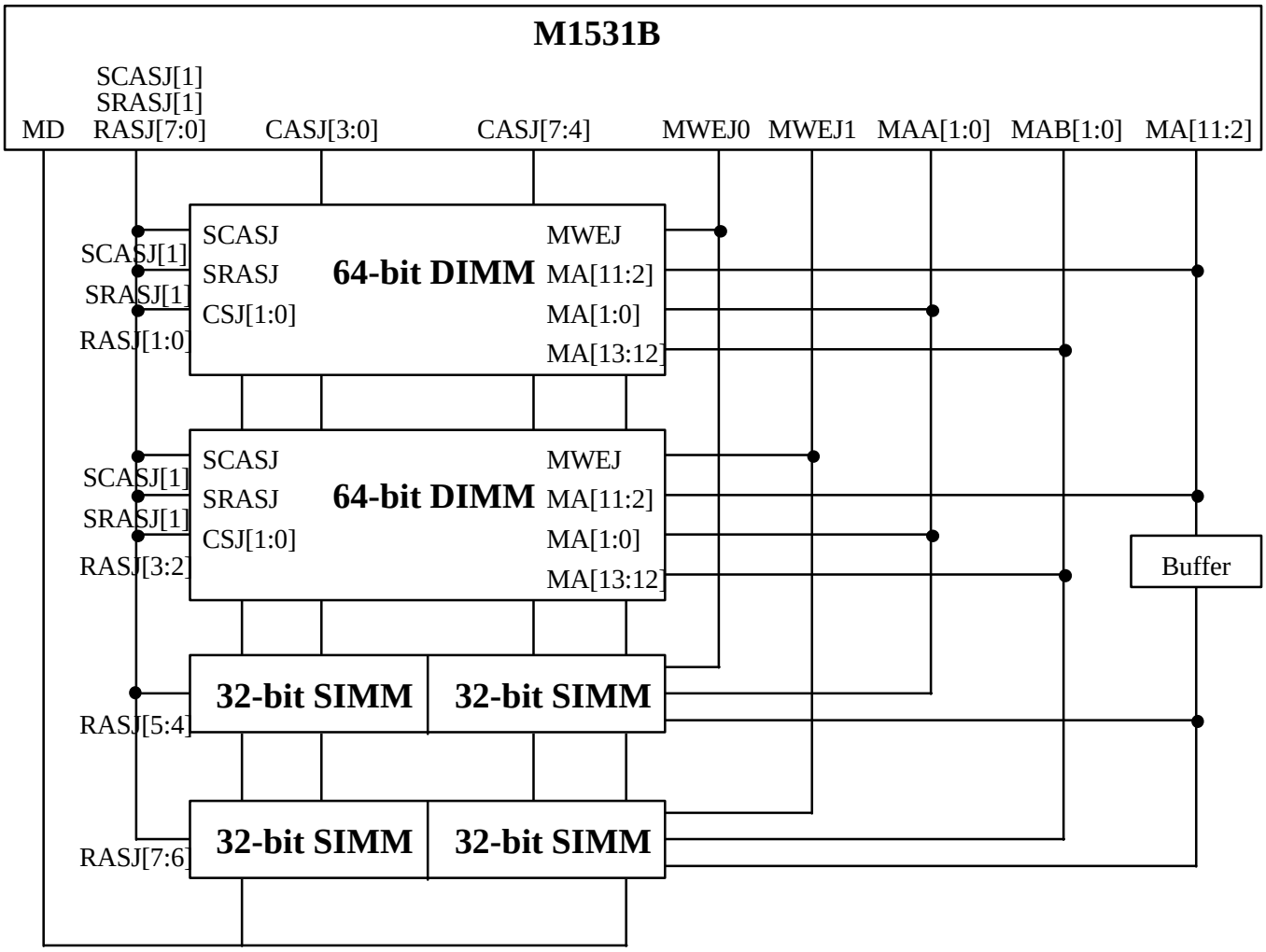
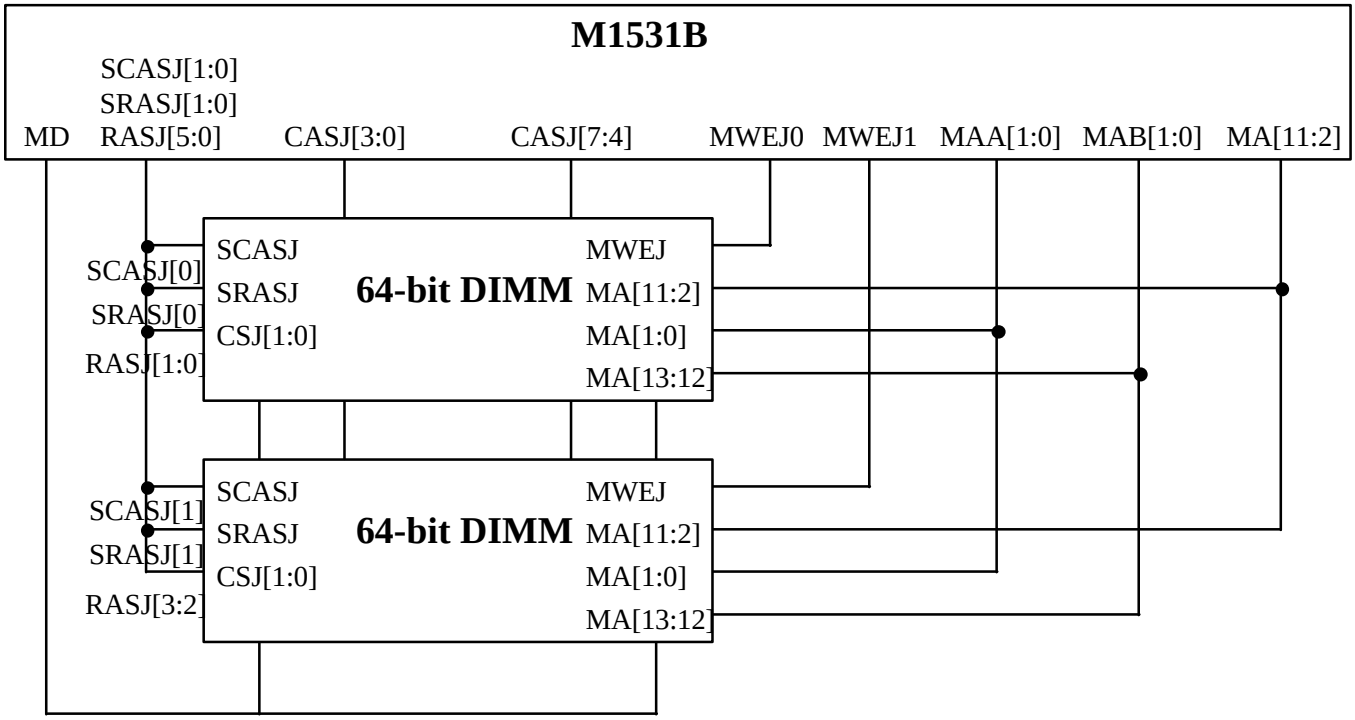
4. SIMM x4 + DIMM x 2 implementation:



2 Double-Sided DRAM Bank (EDO/FPM) +
2 Double-Sided SDRAM Bank

5. **DIMM x 2 implementation:**



2 Double-Sided SDRAM Bank

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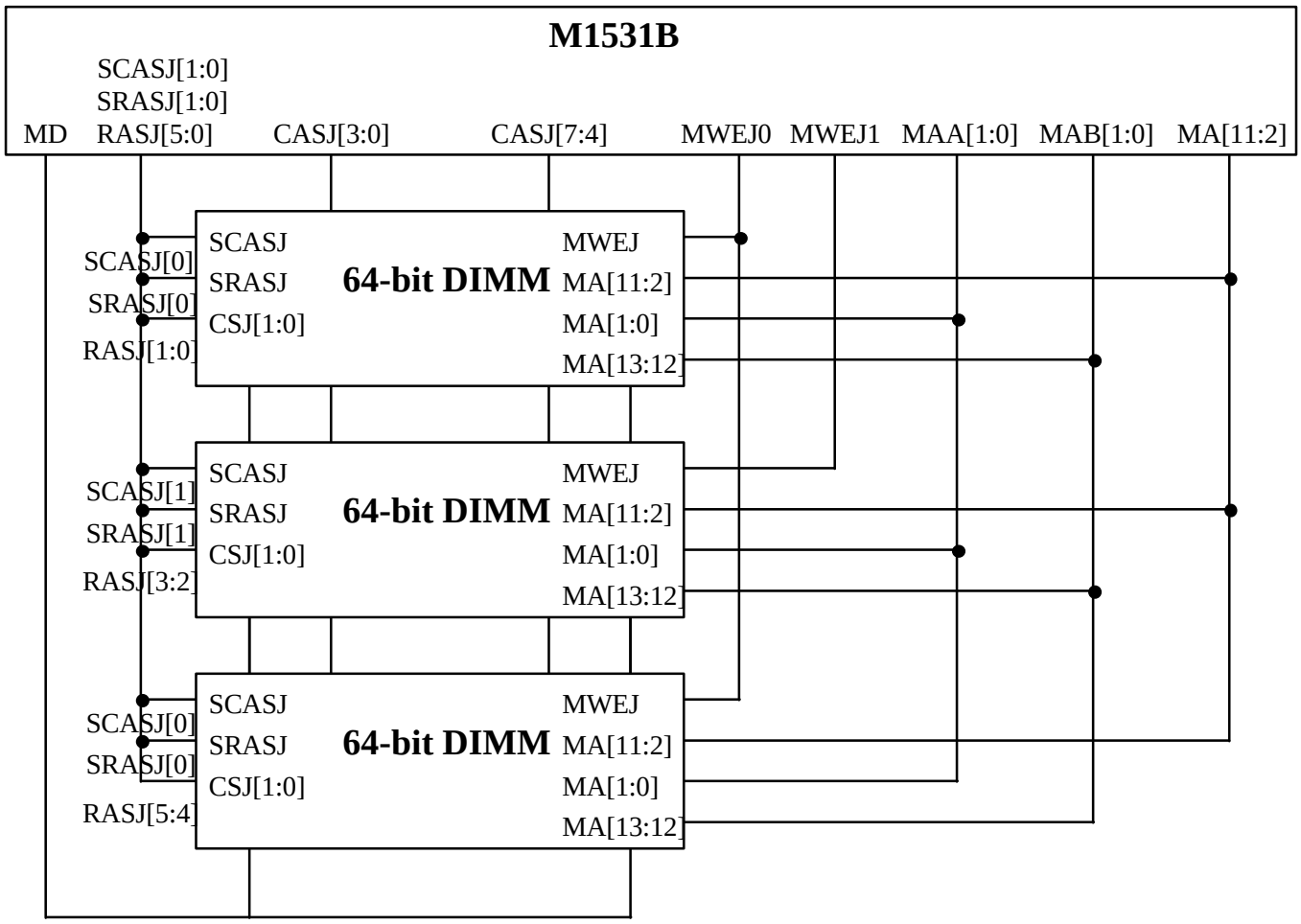
6. DIMM x 3 implementation:



3 Double-Sided SDRAM Bank

Subject: **M1531B Memory Cacheable Size Implementation**

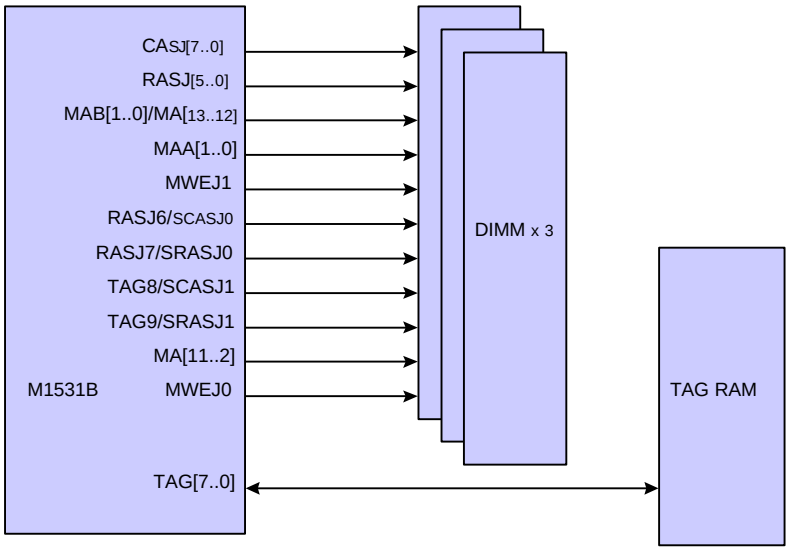
Date: **March 6, 1997**

Part & Version: **M1531B**

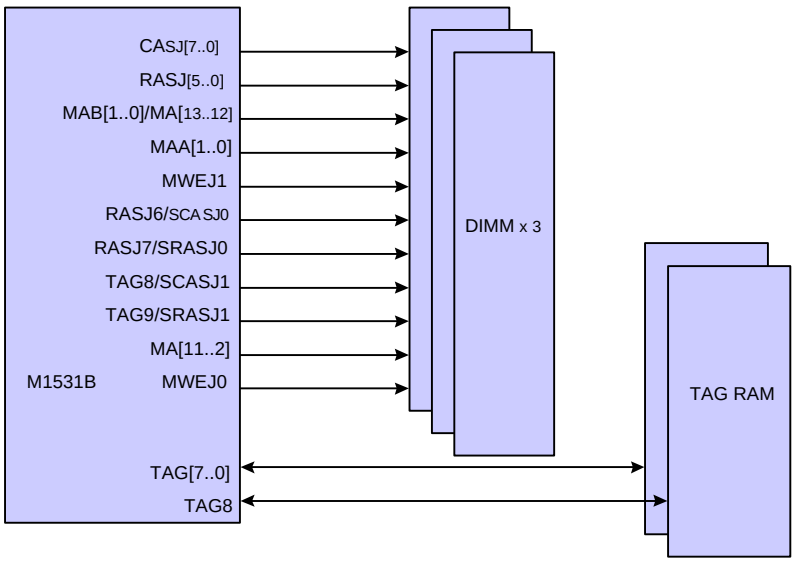
Prepared by: **Bruce Hsueh**

Approved by: **Charles Chiang**

1. 64M byte cacheable size implementation:



2. 128M byte cacheable size implementation:



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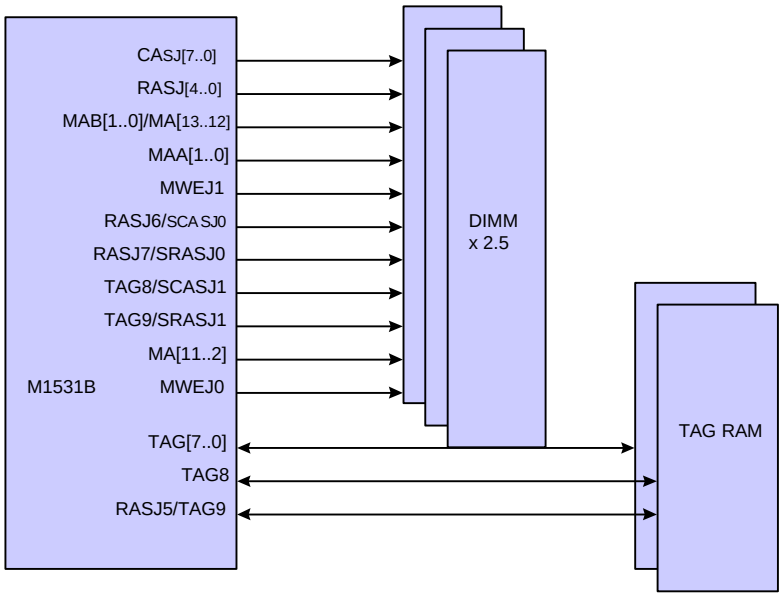
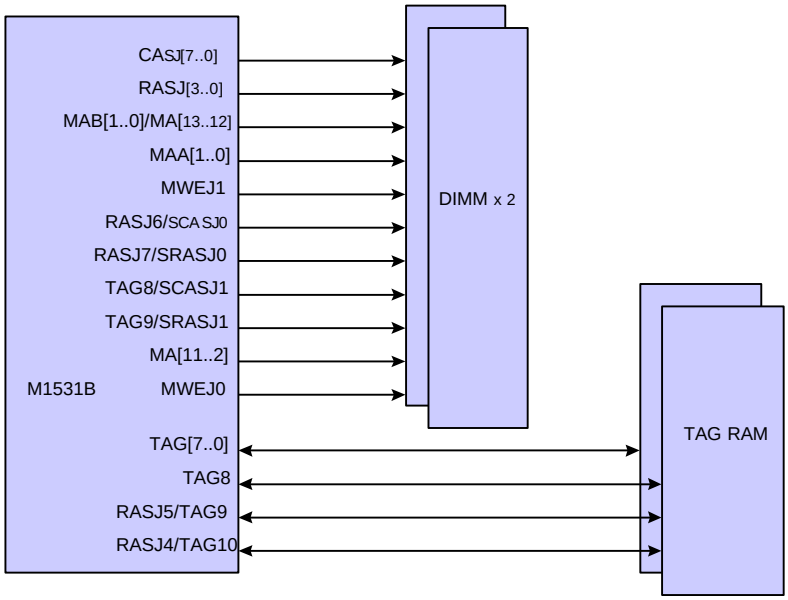
3. 256M byte cacheable size implementation :



4. 512M byte cacheable size implementation:



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