Intel® Desktop Board D820LP
Technical Product Specification

April 2000

Order Number A15751-001

The Intel® Desktop Board D820LP may contain design defects or errors known as errata that may cause the product to deviate from published specifications. Current characterized errata are documented in the Intel Desktop Board D820LP Specification Update.

Revision History

Revision	Revision History	Date
-001	First release of the Intel® Desktop Board D820LP Technical Product Specification.	April 2000

This product specification applies only to standard D820LP desktop boards with BIOS identifier VC82010A.86A (see page 75).

Changes to this specification will be published in the *Intel® Desktop Board D820LP Specification Update* before being incorporated into a revision of this document.

Preface

This Technical Product Specification (TPS) specifies the board layout, components, connectors, power and environmental requirements, and the BIOS for the Intel® Desktop Board D820LP. The TPS describes the standard D820LP board product.

Intended Audience

The TPS is intended to provide detailed, technical information about the D820LP board and its components to the vendors, system integrators, and other engineers and technicians who need this level of information. It is specifically *not* intended for general audiences.

What This Document Contains

Chapter	Description
1	A description of the hardware used on this board
2	A map of the resources of this board
3	The features supported by the BIOS Setup program
4	The contents of the BIOS Setup program's menus and submenus
5	A description of the BIOS error messages, beep codes, POST codes, and enhanced diagnostics

Typographical Conventions

This section contains information about the conventions used in this specification. Not all of these symbols and abbreviations appear in all specifications of this type.

Notes, Cautions, and Warnings

NOTE

Notes call attention to important information.

CAUTION

Cautions are included to help you avoid damaging hardware or losing data.

WARNING

Warnings indicate conditions that if not observed can cause personal injury.

Other Common Notation

#	Used after a signal name to identify an active-low signal (such as USBP0#)
(NxnX)	When used in the description of a component, N indicates component type, xn are the relative coordinates of its location on the board, and X is the instance of the particular part at that general location. For example, J5J1 is a connector, located at 5J. It is the first connector in the 5J area.
KB	Kilobyte (1024 bytes)
Kbit	Kilobit (1024 bits)
MB	Megabyte (1,048,576 bytes)
Mbit	Megabit (1,048,576 bits)
GB	Gigabyte (1,073,741,824 bytes)
xxh	An address or data value ending with a lowercase h indicates a hexadecimal value.
x.x V	Volts. All voltages are DC unless otherwise specified.
†	This symbol is used to indicate third-party brands and names that are the property of their respective owners.

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4 BIOS Setup Program

5 Error Messages and Beep Codes

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1 Product Description

What This Chapter Contains

1.1 Overview

1.1.1 Feature Summary

Table 1 summarizes the D820LP board's major features.

Table 1. Feature Summary

Form Factor	ATX (12.0 inches by 9.6 inches)
Processor	Support for Intel® Pentium® III processors in Flip Chip Pin Grid Array (FC-PGA) packages
Memory	• Two 168-pin RIMM† sockets • Support for up to 512 MB
Chipset	Intel® 82820, consisting of: • Intel 82820 Memory Controller Hub (MCH) with AHA (Accelerated Hub Architecture) bus • Intel® 82801AA I/O Controller Hub (ICH) with AHA bus • Intel® 82802AB 4 Mbit Firmware Hub (FWH)
I/O Control	LPC47M102 SIO low pin count (LPC) interface I/O controller
Accelerated Graphics Port (AGP) Video	AGP universal connector supporting 1X, 2X, and 4X AGP boards
Peripheral Interfaces	• Two serial ports • Two Universal Serial Bus (USB) ports • One parallel port • Two IDE interfaces with Ultra DMA and ATA-66 support • One diskette drive interface • PS/2† keyboard and mouse
Expansion Capabilities	Six add-in board expansion slots: • Five PCI bus add-in board connectors (SMBus routed to PCI connector J4D1) • One AGP universal connector
BIOS	• Intel/AMI BIOS • Intel® 4 Mbit symmetrical flash memory • Support for Advanced Configuration and Power Interface (ACPI), Advanced Power Management (APM), Plug and Play, and SMBIOS
Enhanced Diagnostics	Four dual-color LEDs on the back panel
Hardware Monitor Subsystem	Hardware monitor with: • Two fan sensing inputs used to monitor fan activity • Remote diode temperature sensing • Voltage sensing to detect out-of-range values

continued

Table 1. Feature Summary (continued)

Instantly Available PC	• Support for *PCI Local Bus Specification Revision 2.2* • Suspend to RAM support • Wake on PS/2 keyboard, PS/2 mouse, and USB ports
Wake on LAN† Technology Connector	Support for system wake up using an add-in network interface board with remote wake up capability
Wake on Ring Connector	Support for system wake up using an add-in telephony device, such as a modem

For information about	Refer to
The D820LP board's compliance level with ACPI, APM, Plug and Play, and SMBIOS	Section 1.3, page 16

1.1.2 Manufacturing Options

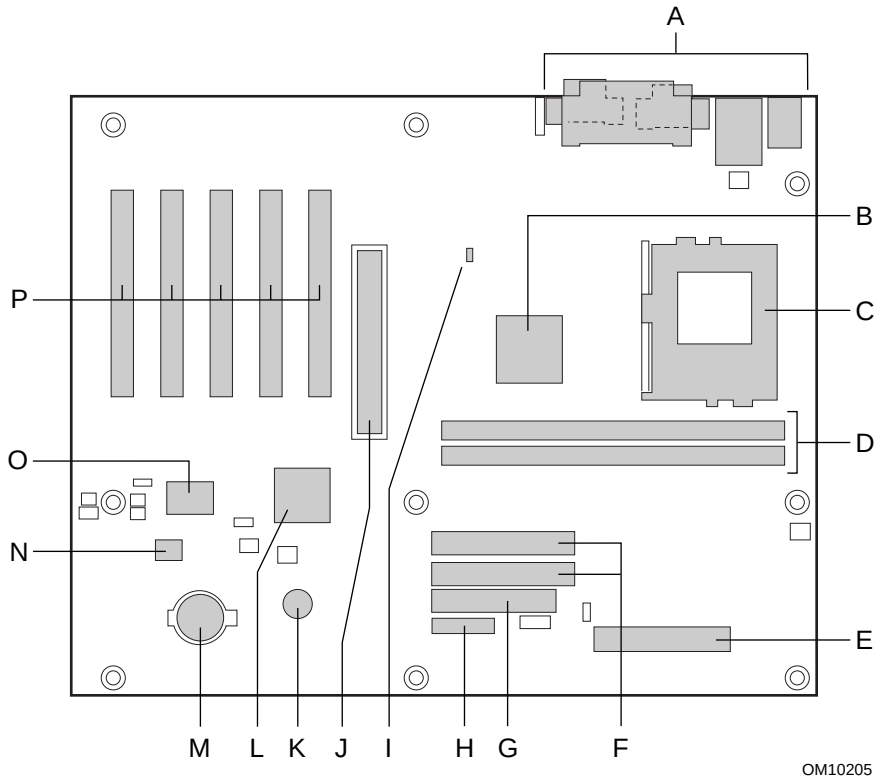
Table 2 summarizes the D820LP board's manufacturing options. The manufacturing options may not be available in all channels.

Table 2. Manufacturing Options

USB Port 1 Routing	A jumper block routes USB port 1 to a back panel connector or to a connector near the front of the board.
Fixed Speed on Fan Connector J7M1	For a non-monitored fan that is always powered on when the computer is powered on.
Fixed Speed on Fan Connector J2L1	For a non-monitored fan that is always powered on when the computer is powered on.

1.1.3 D820LP Board Layout

Figure 1 shows the location of the major components on the D820LP board.



A	Back panel connectors	I	Hardware monitor
B	Intel 82820 Memory Controller Hub (MCH)	J	AGP universal connector
C	370-pin PGA processor connector	K	Speaker
D	RIMM sockets	L	Intel 82801AA I/O Controller Hub (ICH)
E	Power connector	M	Battery
F	IDE connectors	N	Intel 82802AB 4 Mbit Firmware Hub (FWH)
G	Diskette drive connector	O	SMSC LPC47M102 I/O controller
H	Front panel connector	P	PCI bus add-in board connectors

Figure 1. D820LP Board Components

1.1.4 Block Diagram

Figure 2 is a block diagram of the major functional areas of the D820LP board.

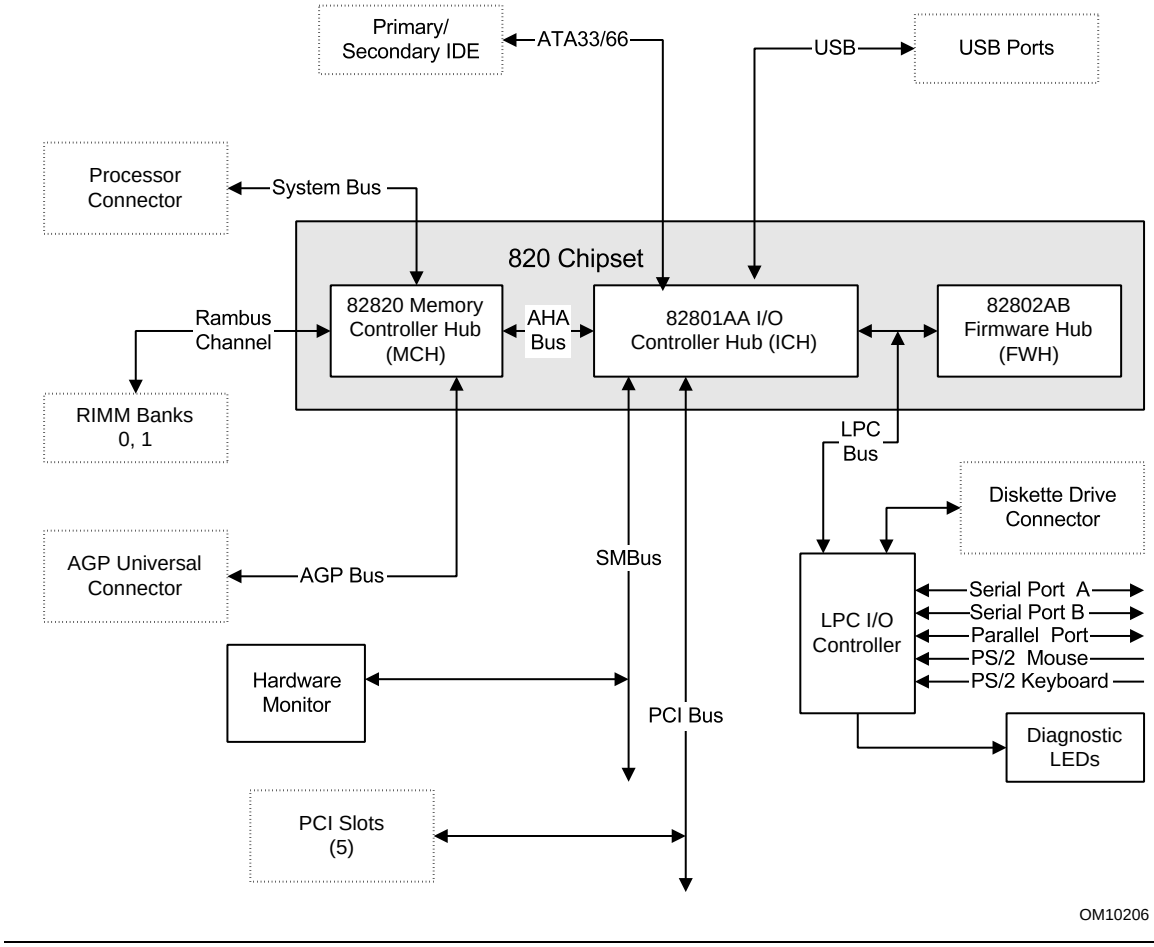


Figure 2. Block Diagram

1.2 Online Support

Find information about Intel desktop boards under “Products” or “Support” at the following World Wide Web site:

http://www.intel.com/design/motherbd

Find processor data sheets, specification updates, and information about proper date access in systems with Intel desktop boards at these World Wide Web sites:

http://www.intel.com/design/litcentr
http://support.intel.com/support/year2000

Find information about the ICH addressing at this World Wide Web site:

http://developer.intel.com/design/chipsets/datashts/

1.3 Design Specifications

Table 3 lists the specifications applicable to the D820LP board.

Table 3. Specifications

Reference Name	Specification Title	Version, Revision Date, and Ownership	The information is available from…
ACPI	*Advanced Configuration and Power Interface Specification*	Version 1.0b, February 2, 1999, Intel Corporation, Microsoft Corporation, and Toshiba Corporation.	http://www.teleport.com/~acpi/
AGP	*Accelerated Graphics Port Interface Specification*	Version 2.0, May 4, 1998, Intel Corporation.	the Accelerated Graphics Implementers Forum at: http://www.agpforum.org/
AMI BIOS	*American Megatrends BIOS Specification*	AMIBIOS 99, 1999 American Megatrends, Inc.	http://www.amibios.com, or http://www.ami.com/download/amibios99.pdf
APM	*Advanced Power Management BIOS Interface Specification*	Version 1.2, February 1996, Intel Corporation, Microsoft Corporation.	http://www.microsoft.com/hwdev/busbios/amp_12.htm

continued

Table 3. Specifications (continued)

Description	Specification Title	Version, Revision Date and Ownership	The information is available from…
ATA-3	*Information Technology - AT Attachment-3 Interface, X3T10/2008D*	Version 6, October 1995, ASC X3T10 Technical Committee	http://www.t13.org/
ATAPI	*Information Technology AT Attachment with Packet Interface Extensions T13/1153D*	Version 18, August 19, 1998, Contact: T13 Chair, Seagate Technology	http://www.t13.org
ATX	*ATX Specification*	Version 2.01, February 1997, Intel Corporation.	http://developer.intel.com/design/motherbd/atx.htm
EPP	*Enhanced Parallel Port IEEE std 1284.1-1997*	Version 1.7, 1997, Institute of Electrical and Electronic Engineers	http://standards.ieee.org/catalog/bus.html
El Torito	*Bootable CD-ROM format specification*	Version 1.0, January 25, 1995, Phoenix Technologies Ltd., and IBM Corporation.	the Phoenix Web site at: http://www.ptltd.com/techs/specs.html
IrDA†	*Serial Infrared Physical Layer Link specification*	Version 1.3, October 15, 1998, Infrared Data Association.	http://www.irda.org/standards/specifications.asp
LPC	*Low Pin Count Interface Specification*	Version 1.0, September 29, 1997, Intel Corporation.	http://www.intel.com/design/chipsets/industry/lpc.htm
PCI	*PCI Local Bus Specification*	Version 2.2, December 18, 1998, PCI Special Interest Group.	http://www.pcisig.com/
	PCI Bus Power Management Interface Specification	Version 1.1, December 18, 1998, PCI Special Interest Group.	http://www.pcisig.com/
Plug and Play	*Plug and Play BIOS specification*	Version 1.0a, May 5, 1994, Compaq Computer Corp., Phoenix Technologies Ltd., and Intel Corporation.	http://www.microsoft.com/hwdev/respec/pnpspecs.htm
RIMM	*Direct Rambus† Serial Presence Detect (SPD) Specification*	Version 1.0, March 1999, Rambus Corp.	http://www.rambus.com/developer/support_rimm.html
	Rambus RIMM specification	Version 1.0 July 1999 Rambus Corp.	http://www.rambus.com/developer/development_support.html

continued

Table 3. Specifications (continued)

Description	Specification Title	Version, Revision Date and Ownership	The information is available from…
SMBIOS	*System Management BIOS Reference Specification*	Version 2.3.1, March 16, 1999, Award Software International Inc., Dell Computer Corporation, Hewlett-Packard Company, Intel Corporation, International Business Machines Corporation, Phoenix Technologies Limited, American Megatrends Inc., and SystemSoft Corporation.	http://developer.intel.com/ial/wfm/design/smbios
UHCI	*Universal Host Controller Interface Design Guide*	Version 1.1, March 1996, Intel Corporation.	http://developer.intel.com/design/USB/UHCI11D.htm
USB	*Universal Serial Bus Specification*	Version 1.1, September 23, 1998, Compaq Computer Corporation, Intel Corporation, Microsoft Corporation, and NEC.	http://www.usb.org/developers
WfM	*Wired for Management Baseline*	Version 2.0, December 18, 1998, Intel Corporation	http://developer.intel.com/ial/WfM/wfmspecs.htm

1.4 Processor

CAUTIONS

The D820LP desktop board supports processors that have a 26 A maximum current draw (1.7 V core). Using a processor not in compliance with these guidelines can damage the processor, the board, and the power supply. See the processor's data sheet for current usage requirements.

Before installing or removing the processor, make sure that AC power has been removed by unplugging the power cord from the computer (the standby power LED should not be lit). Failure to do so could damage the processor and the board. See Figure 5, page 37 for the location of the standby power LED.

NOTE

66 MHz system bus frequency processors are not supported in this product. A hardware lockout is provided so that if such a processor is installed, the D820LP board will not power-up.

The D820LP board supports a single Pentium III processor at system bus frequencies of 100 or 133 MHz. The system bus frequency for the processor is automatically selected.

All supported onboard memory can be cached up to the cachability limit of the processor. See the processor's data sheet for cachability limits.

The D820LP board supports Pentium III processors in FC-PGA packages. The supported processor frequencies are listed in Table 4.

Table 4. Supported Processors

Processor Type	Processor Frequency (MHz)	System Bus Frequency (MHz)	L2 Cache Size (KB)
Pentium III processor	866	133	256
	800EB	133	256
	733	133	256
	667	133	256
	600EB	133	256
	533EB	133	256
	850	100	256
	800	100	256
	750	100	256
	700	100	256
	650	100	256
	600E	100	256
	550E	100	256
	500E	100	256

For information about	Refer to
Processor support for the D820LP boards	Section 1.2, page 16
Processor data sheets	Section 1.2, page 16

1.5 System Memory

⚠ CAUTIONS

A Continuity RIMM module must be installed in any unused memory connector or the desktop board will not boot.

Incorrect insertion of a RIMM module or a Continuity RIMM module in a RIMM connector can damage the D820LP board.

Before installing or removing RIMM modules, make sure that AC power has been removed by unplugging the power cord from the computer (the standby power indicator LED should not be lit). Failure to do so could damage the memory and the board. See Figure 5, page 37 for the location of the standby power indicator LED.

1.5.1 RDRAM† Terminology

The D820LP board uses Direct Rambus DRAM (RDRAM) technology. The following list clarifies some RDRAM terms used in this document.

- For simplicity, Direct Rambus is referred to as Rambus.
- The Rambus memory module for desktop systems is referred to as the RIMM module.
- The RIMM module and RIMM connector use a form factor similar to the DIMM module and connector. They do not, however, work interchangeably.

1.5.2 Memory Features

The Intel 82820 Memory Controller Hub (MCH) integrates a single Rambus channel as an electrically pipelined serial bus (16 data bits in width) with uniform impedance of 28 ohms and single-ended termination. This Rambus channel is capable of providing a processor-to-memory bandwidth up to 1.6 GB/sec.

The board supports the following memory features:

- Up to two 2.5 V, 168-pin, RIMM modules
- 512 MB maximum onboard capacity using 128 or 144 Mbit technology
- Single- or double-sided RIMM modules
- Serial Presence Detect (SPD) memory only
- Non-ECC memory with 16-bit components (128 Mbit technology)
- ECC memory with 18-bit components (144 Mbit technology)

For information about	Refer to
The *Rambus RIMM Specification*	Section 1.3, page 16
The *Direct Rambus Serial Presence Detect (SPD) Specification*	Section 1.3, page 16

1.5.3 Continuity RIMM Modules

All RIMM connectors must be populated to achieve continuity for termination at the Rambus interface. A Continuity RIMM module, sometimes referred to as a "pass-through" module, must be installed in any unused RIMM connector.

1.5.4 RDRAM Memory Configuration

CAUTION

The board supports a total of 32 RDRAM components across the installed RIMM modules. If the total RDRAM component count exceeds 32, the computer will not boot. The number of RDRAM components per RIMM module is indicated on the RIMM module label.

NOTE

To obtain best memory bus loading characteristics, RIMM modules should be installed in Bank 0 first and then in Bank 1. Bank 0 is closest to the processor.

1.5.5 Memory Bus Frequencies

The BIOS automatically selects the memory bus frequency from the Serial Presence Detect (SPD) information in the RIMM module. The D820LP board supports only Serial Presence Detect (SPD) memory. Serial Presence Detect (SPD) information is required to properly configure the Rambus interface. Table 5 describes the memory frequencies supported with standard configurations of the board. The BIOS configures the Rambus interface to the speed of the slowest RIMM module installed.

NOTE

Intel recommends using only tested memory. For a list of tested memory, see the User-Installable Upgrades Web page at:

http://developer.intel.com/design/motherbd/lp/lp_user.htm

Table 5. Memory Bus Frequency with DRCG (Rambus Clock Generator)

	PC600	PC700	PC800
System bus frequency: 100 MHz	300 MHz	(Note)	400 MHz
System bus frequency: 133 MHz	266 MHz	356 MHz	400 MHz

Note: The BIOS configures the Rambus interface to a memory bus frequency of 300 MHz for PC700 memory when configured with a system bus speed of 100 MHz. This is equivalent to PC600 performance.

1.5.6 ECC Memory

ECC memory detects multiple-bit errors and corrects single-bit errors. When ECC memory is installed, the BIOS will support both ECC and non-ECC mode. The BIOS automatically detects if ECC memory is installed and provides the Setup option for selecting ECC mode. ECC mode must be enabled in the Setup program; the default setting is disabled. If any non-ECC memory is installed, ECC operation is not available.

Table 6 describes the effect of using Setup to put each memory type in each supported mode.

Table 6. Memory Error Detection Mode Established in Setup Program

Memory Type	ECC Disabled	ECC Enabled
Non-ECC RIMM	No error detection	N/A
ECC RIMM	No error detection	Single-bit error correction, multiple-bit error detection

NOTE

Whenever ECC mode is selected in Setup, some performance loss may occur.

1.6 Intel® 820 Chipset

The Intel® 820 chipset consists of the following devices:

- 82820 Memory Controller Hub (MCH) with Accelerated Hub Architecture (AHA) bus
- 82801AA I/O Controller Hub (ICH) with AHA bus
- 82802AB Firmware Hub (FWH)

The chipset provides the system, memory, AGP, and I/O interfaces shown in Figure 3.

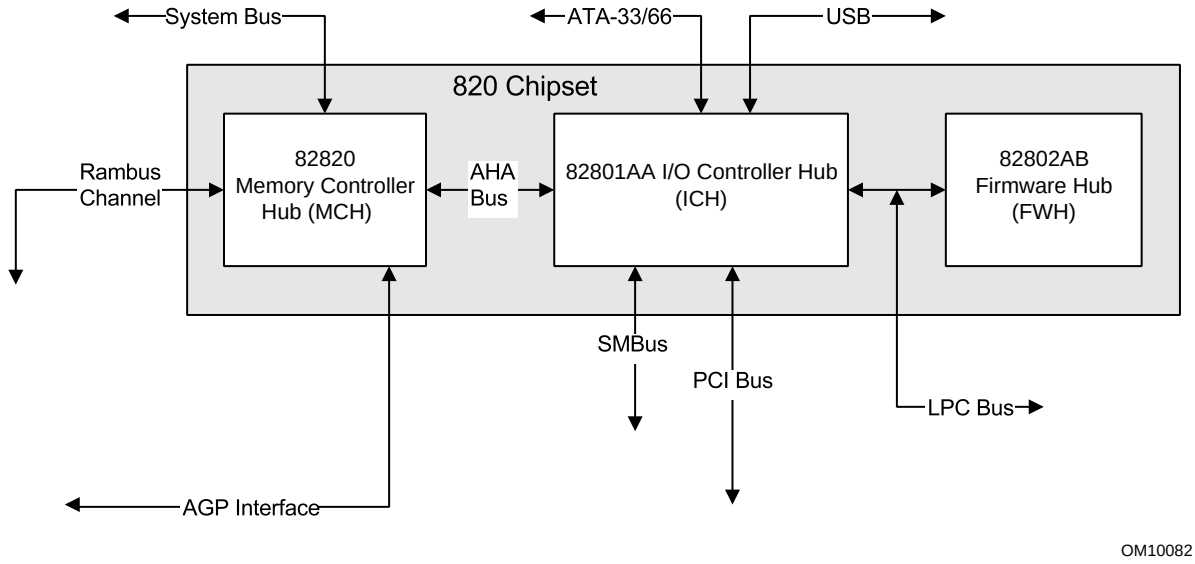


Figure 3. Intel 820 Chipset Block Diagram

For information about	Refer to
The Intel 820 chipset	http://developer.intel.com
The resources used by the chipset	Chapter 2
The chipset's compliance with ACPI, APM, AC '97	Section 1.3, page 16

1.6.1 AGP

The D820LP board supports 1X, 2X, and 4X AGP boards. AGP is a high-performance bus for graphics-intensive applications, such as 3-D applications. AGP, while based on the *PCI Local Bus Specification*, Rev. 2.1, is independent of the PCI bus and is intended for exclusive use with graphical display devices. AGP overcomes certain limitations of the PCI bus related to handling large amounts of graphics data with the following features:

- Pipelined memory Read and Write operations that hide memory access latency
- De-multiplexing of address and data in the bus for nearly 100 percent bus efficiency

For information about	Refer to
Obtaining the *Accelerated Graphics Port Interface Specification*	Section 1.3, page 16

1.6.2 USB

The D820LP board has two USB ports; one USB peripheral can be connected to each port. For more than two USB devices, an external hub can be connected to either port. The two USB ports are implemented with stacked back panel connectors. As a manufacturing option, one USB port can be routed by a jumper to a connector near the front of the board. D820LP board fully supports UHCI and uses UHCI-compatible software drivers. USB features include:

- Self-identifying peripherals that can be plugged in while the computer is running
- Automatic mapping of function to driver and configuration
- Support for isochronous and asynchronous transfer types over the same set of wires
- Support for up to 127 physical devices
- Guaranteed bandwidth and low latencies appropriate for telephony, audio, and other applications
- Error-handling and fault-recovery mechanisms built into the protocol

NOTE

Computer systems that have an unshielded cable attached to a USB port may not meet FCC Class B requirements, even if no device or a low-speed USB device is attached to the cable. Use shielded cable that meets the requirements for full-speed devices.

For information about	Refer to
The location of the USB connectors on the back panel	Figure 6, page 46
The signal names of the back panel USB connectors	Table 18, page 47
The manufacturing option to route USB port 1 signals to a connector near the front of the board:	
• Location of the USB routing jumper block	Figure 10, page 61
• USB routing jumper block settings	Table 41, page 63
• Location of the front USB connector	Figure 9, page 57
• Signal names of the front USB connector	Table 37, page 60
The USB specification and UHCI	Section 1.3, page 16

1.6.3 IDE Support

1.6.3.1 IDE Interfaces

The D820LP board has two independent bus-mastering IDE interfaces. These interfaces support:

- ATAPI devices (such as CD-ROM drives)
- ATA devices using the transfer modes listed in Table 62 on page 95

The BIOS supports logical block addressing (LBA) and extended cylinder head sector (ECHS) translation modes. The drive reports the transfer rate and translation mode to the BIOS.

The D820LP board supports laser servo (LS-120) diskette technology through its IDE interfaces. The LS-120 drive can be configured as a boot device by setting the BIOS Setup program's Boot menu to one of the following:

- ARMD-FDD (ATAPI removable media device – floppy disk drive)
- ARMD-HDD (ATAPI removable media device – hard disk drive)

For information about	Refer to
The location of the IDE connectors	Figure 7, page 49
The signal names of the IDE connectors	Table 21, page 50
The BIOS Setup program's Boot menu	Table 68, page 101
Ultra ATA/66	Section 3.3.2, page 77

1.6.3.2 SCSI Hard Drive Activity LED Connector

The SCSI hard drive activity LED connector is a 1 x 2-pin connector that allows an add-in SCSI controller to use the same LED as the IDE controller. This connector can be attached to the LED output of the add-in controller board. The LED will indicate when data is being read or written using the add-in controller.

For information about	Refer to
The location of the SCSI hard drive activity LED connector	Figure 7, page 49
The signal names of the SCSI hard drive activity LED connector	Table 25, page 50

1.6.4 Real-Time Clock, CMOS SRAM, and Battery

The real-time clock is compatible with DS1287 and MC146818 components. The clock provides a time-of-day clock and a multi-century calendar with alarm features and century rollover. The real-time clock supports 256 bytes of battery-backed CMOS SRAM in two banks that are reserved for BIOS use.

A coin-cell battery (CR2032) powers the real-time clock and CMOS memory. When the computer is not plugged into a wall socket, the battery has an estimated life of three years. When the computer is plugged in, the standby current from the power supply extends the life of the battery. The clock is accurate to ± 13 minutes/year at 25 ºC with 3.3 VSB applied.

The time, date, and CMOS values can be specified in the BIOS Setup program. The CMOS values can be returned to their defaults by using the BIOS Setup program.

NOTES

If the battery and AC power fail, standard defaults, not custom defaults, will be loaded into CMOS RAM at power-on.

The recommended method of accessing the date in systems with D820LP boards is indirectly from the Real-Time Clock (RTC) via the BIOS. The BIOS on D820LP boards contains a century checking and maintenance feature. This feature checks the two least significant digits of the year stored in the RTC during each BIOS request (INT 1Ah) to read the date and, if less than 80 (i.e., 1980 is the first year supported by the PC), updates the century byte to 20. This feature enables operating systems and applications using the BIOS date/time services to reliably manipulate the year as a four-digit value.

For information about	Refer to
Proper date access in systems with D820LP boards	Paragraph 1.2, page 16

1.7 I/O Controller

The SMSC LPC47M102 I/O Controller provides the following features:

- Low pin count (LPC) interface
- 3.3 V operation
- Two serial ports
- One parallel port with Extended Capabilities Port (ECP) and Enhanced Parallel Port (EPP) support
- Serial IRQ interface compatible with serialized IRQ support for PCI systems
- PS/2-style mouse and keyboard interfaces
- Interface for one 1.2 MB, 1.44 MB, or 2.88 MB diskette drive
- Intelligent power management, including a programmable wake up event interface
- PME (Power Management Event) Interface
- IrDA 1.0 compliant
- Fan control:
  - Two fan control outputs
  - Two fan tachometer inputs

The BIOS Setup program provides configuration options for the I/O controller.

For information about	Refer to
SMSC LPC47M102 I/O controller	http://www.smsc.com

1.7.1 Serial Ports

The D820LP board has two 9-pin D-Sub serial port connectors located on the back panel. The serial ports' NS16C550-compatible UARTs support data transfers at speeds up to 115,200 bits / sec with BIOS support. The serial ports can be assigned as COM1 (3F8h), COM2 (2F8h), COM3 (3E8h), or COM4 (2E8h).

For information about	Refer to
The location of the serial port connectors	Figure 6, page 46
The signal names of the serial port connectors	Table 20, page 48

1.7.2 Infrared Support

On the front panel connector, there are four pins that support Hewlett Packard HSDL-1000 compatible infrared (IR) transmitters and receivers. In the BIOS Setup program, serial port B can be directed to a connected IR device. (In this case, the serial port B connector on the back panel cannot be used.) The IR connection can be used to transfer files to or from portable devices like laptops, PDAs, and printers. The Infrared Data Association (IrDA) specification supports data transfers of 115,200 bits / second at a distance of 1 meter.

For information about	Refer to
The infrared port connector	Table 34, page 58
Configuring serial port B for infrared applications	Section 4.4.3, page 92
The IrDA specification	Section 1.3, page 16

1.7.3 Parallel Port

The connector for the multimode bidirectional parallel port is a 25-pin D-Sub connector located on the back panel. In the BIOS Setup program, the parallel port can be configured for the following:

- Output only (PC-AT† -compatible mode)
- Bi-directional (PS/2 compatible)
- EPP
- ECP

For information about	Refer to
The location of the parallel port connector	Figure 6, page 46
The signal names of the parallel port connector	Table 19, page 47

1.7.4 Diskette Drive Controller

The I/O controller supports one diskette drive that is compatible with the 82077 diskette drive controller and supports both PC-AT and PS/2 modes.

NOTE

The I/O controller also supports a 1.2 MB, 3.5-inch diskette drive. A special driver is required for this configuration.

For information about	Refer to
The location of the diskette drive connector	Figure 7, page 49
The signal names of the diskette drive connector	Table 23, page 52
The supported diskette drive capacities and sizes	Table 63, page 96

1.7.5 Keyboard and Mouse Interface

PS/2 keyboard and mouse connectors are located on the back panel. The +5 V lines to these connectors are protected with a PolySwitch† circuit that, like a self-healing fuse, re-establishes the connection after an overcurrent condition is removed.

NOTE

The keyboard is supported in the bottom PS/2 connector and the mouse is supported in the top PS/2 connector. Power to the computer should be turned off before a keyboard or mouse is connected or disconnected.

The keyboard controller contains the AMI keyboard and mouse controller code, provides the keyboard and mouse control functions, and supports password protection for power-on/reset. A power-on/reset password can be specified in the BIOS Setup program.

The keyboard controller also supports the hot-key sequence <Ctrl><Alt><Del>, which initiates a soft reset unless the keystrokes are trapped by the operating system.

For information about	Refer to
The location of the keyboard and mouse connectors	Figure 6, page 46
The signal names of the keyboard and mouse connectors	Table 17, page 47

1.8 Hardware Management Features

The hardware management features enable the D820LP board to be compatible with the Wired for Management (WfM) specification. The D820LP board has several hardware management features, including the following:

- Hardware monitor component
- Chassis intrusion detection
- Fan control and monitoring (implemented on the SMSC LPC47M102 I/O controller)

For information about	Refer to
The WfM specification	Table 3, page 16
The SMSC LPC47M102 I/O controller	Section 1.7, page 26

1.8.1 Hardware Monitor Component

The hardware monitor component provides low-cost instrumentation capabilities. The features of the component include:

- Internal ambient temperature sensing
- Remote thermal diode sensing for direct monitoring of processor temperature (if supported in the processor)
- Power supply monitoring (+12, +5, +3.3, +2.5, 3.3 VSB, V_{CCP}) to detect levels above or below acceptable values
- SMBus interface

1.8.2 Chassis Intrusion Detect Connector

The D820LP board supports a chassis security feature that detects if the chassis cover is removed. For the chassis intrusion circuit to function, the chassis' power supply must be connected to AC power. The security feature uses a mechanical switch on the chassis that attaches to the chassis intrusion detect connector. The mechanical switch is closed for normal computer operation.

For information about	Refer to
The location of the chassis intrusion detect connector	Figure 8, page 54
The signal names of the chassis intrusion detect connector	Table 32, page 56

1.9 Power Management Features

Power management is implemented at several levels, including:

- Software support:
  - Advanced Configuration and Power Interface (ACPI)
  - Advanced Power Management (APM)
- Hardware support:
  - Power connector
  - Fan connectors
  - Wake on LAN technology
  - Instantly Available technology
  - Wake on Ring
  - Resume on Ring
  - Wake from USB
  - Wake from PS/2 keyboard or PS/2 mouse
  - PME# wakeup support

1.9.1 Software Support

The software support for power management includes:

- ACPI
- APM

If the D820LP board is used with an ACPI-aware operating system, the BIOS can provide ACPI support. Otherwise, it defaults to APM support.

1.9.1.1 APM

APM makes it possible for the computer to enter an energy-saving standby mode. The standby mode can be initiated in the following ways:

- Time-out period specified in the BIOS Setup program
- From the operating system, such as the Standby menu item in Windows† 98

In standby mode, the D820LP board can reduce power consumption by spinning down hard drives, and reducing power to or turning off VESA† DPMS-compliant monitors. Power management mode can be enabled or disabled in the BIOS Setup program

While in standby mode, the system retains the ability to respond to external interrupts and service requests, such as incoming faxes or network messages. Any keyboard or mouse activity brings the system out of standby mode and immediately restores power to the monitor.

The BIOS enables APM by default; but the operating system must support an APM driver for the power management features to work. For example, Windows 98 supports the power management features upon detecting that APM is enabled in the BIOS.

For information about	Refer to
Enabling or disabling power management in the BIOS Setup program	Section 4.6, page 100
The D820LP board's compliance level with APM	Table 3, page 16

1.9.1.2 ACPI

ACPI gives the operating system direct control over the power management and Plug and Play functions of a computer. The use of ACPI with the D820LP board requires an operating system that supports ACPI. ACPI features include:

- Plug and Play (including bus and device enumeration) and APM support normally contained in the BIOS
- Power management control of individual devices, add-in boards (some add-in boards may require an ACPI-aware driver), video displays, and hard disk drives
- Methods for achieving less than 30-watt system operation in the power-on/standby sleeping state
- A Soft-off feature that enables the operating system to power off the computer
- Support for multiple wake up events (see Table 9 on page 33)
- Support for a front panel power and sleep mode switch. Table 7 lists the system states based on how long the power switch is pressed, depending on how ACPI is configured with an ACPI-aware operating system.

Table 7. Effects of Pressing the Power Switch

If the system is in this state…	…and the power switch is pressed for…	…the system enters this state
Off (ACPI G2/S5 – Soft off)	Less than four seconds	Power-on (ACPI G0 – working state)
On (ACPI G0 – working state)	Less than four seconds	Soft-off/Standby (ACPI G1 – sleeping state)
On (ACPI G0 – working state)	More than four seconds	Fail safe power-off (ACPI G2/S5 – Soft off)
Sleep (ACPI G1 – sleeping state)	Less than four seconds	Wake up (ACPI G0 – working state)
Sleep (ACPI G1 – sleeping state)	More than four seconds	Power-off (ACPI G2/S5 – Soft off)

For information about	Refer to
The D820LP board's compliance level with ACPI	Section 1.3, page 16

1.9.1.2.1 System States and Power States

Under ACPI, the operating system directs all system and device power state transitions. The operating system puts devices in and out of low-power states based on user preferences and knowledge of how devices are being used by applications. Devices that are not being used can be turned off. The operating system uses information from applications and user settings to put the system as a whole into a low-power state.

Table 8 lists the power states supported by the D820LP board along with the associated system power targets. See the ACPI specification for a complete description of the various system and power states.

Table 8. Power States and Targeted System Power

Global States	Sleeping States	CPU States	Device States	Targeted System Power (Note 1)
G0 – working state	S0 – working	C0 – working	D0 – working state	Full power > 30 W
G1 – sleeping state	S1 – CPU stopped	C1 – stop grant	D1, D2, D3 – device specification specific.	5 W < power < 30 W
G1 – sleeping state	S3 – Suspend to RAM. Context saved to RAM.	No power	D3 – no power except for wake up logic.	Power < 5 W (Note 2)
G2/S5	S5 – Soft off. Context not saved. Cold boot is required.	No power	D3 – no power except for wake up logic.	Power < 5 W (Note 2)
G3 – mechanical off. AC power is disconnected from the computer.	No power to the system.	No power	D3 – no power for wake up logic, except when provided by battery or external source.	No power to the system so that service can be performed.

Notes:

1. Total system power is dependent on the system configuration, including add-in boards and peripherals powered by the system chassis' power supply.
2. This is dependent on the standby power consumption of wake up devices used in the system.

1.9.1.2.2 Wake Up Devices and Events

Table 9 lists the devices or specific events that can wake the computer from specific states.

Table 9. Wake Up Devices and Events

These devices/events can wake up the computer…	…from this state
Power switch	S1, S3, S5
RTC alarm	S1, S3, S5 (Note 1)
PME# (including PCI 2.2 compliant add-in boards)	S1, S3, S5 (Note 2)
LAN (through Wake on LAN technology connector)	S5 (Note 2)
Modem (through COM port connector)	S1, S3
IR command	S1, S3
USB	S1, S3
PS/2 keyboard	S1, S3
PS/2 mouse	S1

Notes:

1. Wakes from the S5 state only if the sleep state was entered by setting the SLP_EN and SLP_TYP bits via software. For information about setting these bits, see the ICH datasheet at the following Intel World Wide Web site: *http://developer.intel.com/design/chipsets/datashts/290655.htm*
2. Wakes from the S5 state only if the S5 jumper block has pins 1 and 2 connected. See Table 39 on page 62.

1.9.1.2.3 Plug and Play

In addition to power management, ACPI provides controls and information so that the operating system can facilitate Plug and Play device enumeration and configuration. ACPI is used only to enumerate and configure D820LP board devices that do not have other hardware standards for enumeration and configuration. PCI devices on the D820LP board, for example, are not enumerated by ACPI.

1.9.2 Hardware Support

CAUTION

If the Wake on LAN, Wake from USB, and Instantly Available technology features are used, ensure that the power supply provides adequate +5 V standby current. Failure to do so can damage the power supply. The total amount of standby current required depends on the wake devices supported. Refer to Section 2.11.3 on page 67 for additional information.

The D820LP board provides hardware features that support power management, including:

- Power connector
- Fan connectors
- Wake on LAN technology
- Instantly Available technology
- Wake on Ring
- Resume on Ring
- Wake from USB
- Wake from PS/2 keyboard and mouse
- PME# wakeup support

Both Wake on LAN technology and Instantly Available technology require power from the +5 V standby line. The sections discussing these features describe the incremental standby power requirements for each.

Wake on Ring and Resume on Ring enable telephony devices to access the computer when it is in a power-managed state. The method used depends on the type of telephony device (external or internal) and the power management mode being used (APM or ACPI).

NOTE

The use of Wake from USB and Resume on Ring technologies from an ACPI state requires an operating system that provides full ACPI support.

1.9.2.1 Power Connector

When used with an ATX-compliant power supply that supports remote power-on and power-off, the D820LP board can turn off the system power through software control. To enable soft-off control in software, power management must be enabled in the BIOS Setup program's Power menu and in the operating system. When the system BIOS receives the correct APM command from the operating system, the BIOS turns off power to the computer.

For information about	Refer to
The location of the power connector	Figure 8, page 54
The signal names of the power connector	Table 28, page 55
The ATX specification	Section 1.3, page 16
BIOS Setup's Power menu	Table 67, page 100

1.9.2.2 Fan Connectors

The D820LP board has three fan connectors. The functions of these connectors are described in Table 10.

Table 10. Fan Connector Descriptions

Connector	Function
Processor fan (J7M1)	Provides +12 VDC. The fan voltage can be switched on or off, depending on the power management state of the computer. A tachometer feedback connection is also provided. The fan speed is variable. As a manufacturing option, the fan is not monitored and is always powered on when the computer is powered on.
Chassis fan (J2L1)	Provides +12 VDC. The fan voltage can be switched on or off, depending on the power management state of the computer. A tachometer feedback connection is also provided. The fan speed is variable. As a manufacturing option, the fan is not monitored and is always powered on when the computer is powered on.
Chassis fan (J8D1)	Provides +12 VDC.

For information about	Refer to
The location of the fan connectors	Figure 8, page 54
The signal names of the fan connectors	Section 2.8.3, page 54

1.9.2.3 Wake on LAN Technology

CAUTION

For Wake on LAN technology, the 5 V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to provide adequate standby current when implementing Wake on LAN technology can damage the power supply. Refer to Section 2.11.3 on page 67 for additional information.

Wake on LAN technology enables remote wakeup of the computer through a network. The LAN subsystem PCI bus network adapter monitors network traffic at the Media Independent Interface. Upon detecting a Magic Packet† frame, the LAN subsystem asserts a wakeup signal that powers up the computer. Depending on the LAN implementation, the D820LP board supports Wake on LAN technology in one of two ways:

- Through the Wake on LAN technology connector (APM or ACPI S5 only)
- Through the PCI bus PME# signal (for PCI 2.2 compliant LAN designs)

The Wake on LAN technology connector can be used with PCI bus network adapters that have a remote wake up connector, as shown in Figure 4. Network adapters that are PCI 2.2 compliant assert the wakeup signal through the PCI bus signal PME# (pin A19 on the PCI bus connectors).

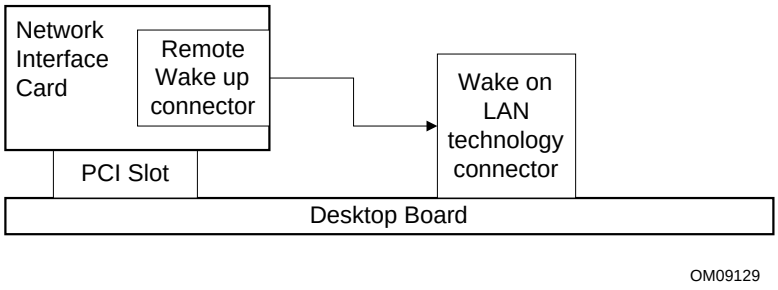


Figure 4. Using the Wake on LAN Technology Connector

For information about	Refer to
The location of the Wake on LAN technology connector	Figure 8, page 54
The signal names of the Wake on LAN technology connector	Table 30, page 56

1.9.2.4 Instantly Available Technology

⚠ CAUTION

For Instantly Available technology, the 5 V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to provide adequate standby current when implementing Instantly Available technology can damage the power supply. Refer to Section 2.11.3 on page 67 for additional information.

Instantly Available technology enables the D820LP board to enter the ACPI S3 (Suspend-to-RAM) sleep-state. While in the S3 sleep-state, the computer will appear to be off (the power supply is off, the fans are off, and the front panel LED is amber if dual-color or off if single-color). When signaled by a wake up device or event, the system quickly returns to its last known wake state. Table 9 on page 33 lists the devices and events that can wake the computer from the S3 state.

The D820LP board supports the *PCI Bus Power Management Interface Specification*. For information on the versions of this specification, see Section 1.3. Add-in boards that also support this specification can participate in power management and can be used to wake the computer.

The use of Instantly Available technology requires operating system support and PCI 2.2 compliant add-in boards and drivers.

The standby power LED (located between the AGP universal connector and the RIMM Bank 0 connector) provides an indication that power is still present to the RIMM modules and PCI bus connectors, even when the computer appears to be off. Figure 5 shows the location of the standby power LED.

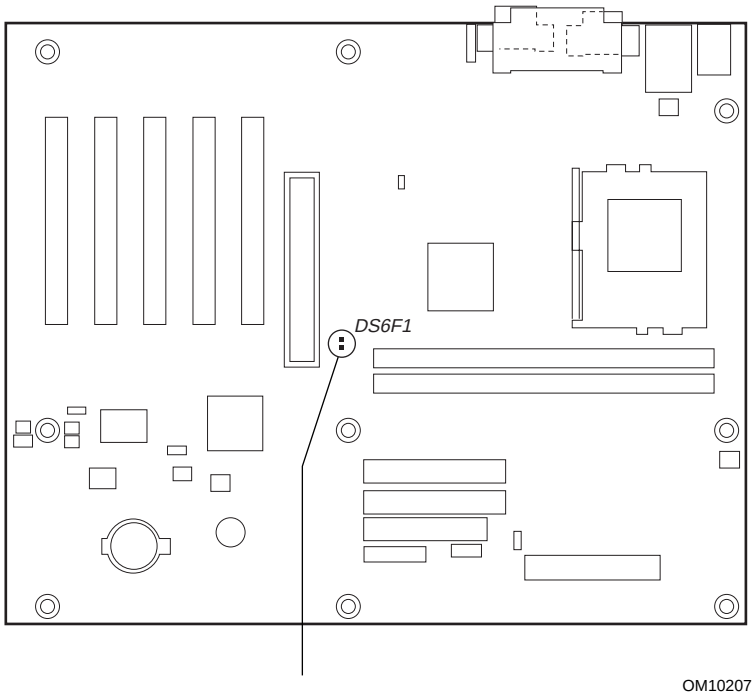


Figure 5. Location of Standby Power LED

1.9.2.5 Wake on Ring

The operation of Wake on Ring can be summarized as follows:

- Powers up the computer from the APM soft-off mode.
- Requires two calls to access the computer:
  - First call restores the computer.
  - Second call enables access (when supporting software is installed).
- Detects incoming call differently for external as opposed to internal modems:
  - For external modems, D820LP board hardware monitors the ring indicator (RI) input of serial port A (serial port B does not support this feature).
  - For internal modems that do not support PME#, a cable must be routed from the modem to the Wake on Ring connector.

For information about	Refer to
The location of the Wake on Ring connector	Figure 8, page 56
The signal names of the Wake on Ring connector	Table 31, page 56

1.9.2.6 Resume on Ring

The operation of Resume on Ring can be summarized as follows:

- Resumes operation from either the APM sleep mode or the ACPI S1 state
- Requires only one call to access the computer
- Detects incoming call similarly for external and internal modems; does not use the Wake on Ring connector
- Requires that the modem interrupt be unmasked for correct operation

1.9.2.7 Wake from USB

USB bus activity wakes the computer from an ACPI S1 or S3 state.

NOTE

Wake from USB requires the use of a USB peripheral that supports Wake from USB.

1.9.2.8 Wake from PS/2 Keyboard or PS/2 Mouse

PS/2 keyboard activity wakes the computer from the ACPI S1 or S3 states. PS/2 mouse activity wakes the computer from the ACPI S1 state.

1.9.2.9 PME# Wake Up Support

When the PME# signal on the PCI bus is asserted, the computer wakes from these ACPI states: S1, S3, or S5 (if pins 1 and 2 are connected on the S5 remote control jumper block at J4A2).

For information about	Refer to
The location of the S5 remote control jumper block	Figure 10, page 61
Jumper setting for the S5 remote control jumper block	Section 2.9.1, page 62

2 Technical Reference

What This Chapter Contains

2.1 Introduction

Sections 2.2 - 2.6 contain several standalone tables. Table 11 describes the system memory map, Table 12 shows the I/O map, Table 13 lists the DMA channels, Table 14 defines the PCI configuration space map, and Table 15 describes the interrupts. The remaining sections in this chapter are introduced by text found with their respective section headings.

2.2 Memory Map

Table 11. System Memory Map

Address Range (decimal)	Address Range (hex)	Size	Description
1024 K - 524288 K	100000 - 1FFFFFFF	511 MB	Extended memory
960 K - 1024 K	F0000 - FFFFF	64 KB	Runtime BIOS
896 K - 960 K	E0000 - EFFFF	64 KB	Reserved
800 K - 896 K	C8000 - DFFFF	96 KB	Available high DOS memory
640 K - 800 K	A0000 - C7FFF	160 KB	Video memory and BIOS
639 K - 640 K	9FC00 - 9FFFF	1 KB	Extended BIOS data (movable by memory manager software)
512 K - 639 K	80000 - 9FBFF	127 KB	Extended conventional memory
0 K - 512 K	00000 - 7FFFF	512 KB	Conventional memory

2.3 I/O Map

Table 12. I/O Map

Address (hex)	Size	Description
0000 - 000F	16 bytes	DMA controller
0020 - 0021	2 bytes	Programmable Interrupt Control (PIC)
0040 - 0043	4 bytes	System timer
0060	1 byte	Keyboard controller byte—reset IRQ
0061	1 byte	System speaker
0064	1 byte	Keyboard controller, CMD/STAT byte
0070 - 0071	2 bytes	System CMOS/Real Time Clock
0072 - 0073	2 bytes	System CMOS
0080 - 008F	16 bytes	DMA controller
0092	1 byte	Fast A20 and PIC
00A0 - 00A1	2 bytes	PIC
00B2 - 00B3	2 bytes	APM control
00C0 - 00DF	32 bytes	DMA
00F0	1 byte	Numeric data processor
0170 - 0177	8 bytes	Secondary IDE channel
01F0 - 01F7	8 bytes	Primary IDE channel
0228 - 022F (Note 1)	8 bytes	LPT3
0278 - 027F (Note 1)	8 bytes	LPT2
02E8 - 02EF (Note 1)	8 bytes	COM4/video (8514A)
02F8 - 02FF (Note 1)	8 bytes	COM2
0376	1 byte	Secondary IDE channel command port
0377, bits 6:0	7 bits	Secondary IDE channel status port
0378 - 037F	8 bytes	LPT1
03B0 - 03BB	12 bytes	Intel 82820 - Memory Controller Hub (MCH)
03C0 - 03DF	32 bytes	Intel 82820 - Memory Controller Hub (MCH)
03E8 - 03EF	8 bytes	COM3

continued

Table 12. I/O Map (continued)

Address (hex)	Size	Description
03F0 - 03F5	6 bytes	Diskette channel 1
03F6	1 byte	Primary IDE channel command port
03F8 - 03FF	8 bytes	COM1
04D0 - 04D1	2 bytes	Edge/level triggered PIC
LPTn + 400h	8 bytes	ECP port, LPTn base address + 400h
0CF8 - 0CFB (Note 2)	4 bytes	PCI configuration address register
0CF9 (Note 3)	1 byte	Turbo and reset control register
0CFC - 0CFF	4 bytes	PCI configuration data register
FFA0 - FFA7	8 bytes	Primary bus master IDE registers
FFA8 – FFAF	8 bytes	Secondary bus master IDE registers
96 contiguous bytes starting on a 128-byte divisible boundary		ICH (ACPI + TCO)
64 contiguous bytes starting on a 64-byte divisible boundary		D820LP board resource
32 contiguous bytes starting on a 32-byte divisible boundary		ICH (USB)
16 contiguous bytes starting on a 16-byte divisible boundary		ICH (SMBus)
4096 contiguous bytes starting on a 4096-byte divisible boundary		Intel 82801AA PCI bridge

Notes:

1. Default, but can be changed to another address range.
2. Dword access only.
3. Byte access only.

NOTE

Some additional I/O addresses are not available due to ICH address aliassing. For information about the ICH addressing, refer to Section 1.2 on page 16.

2.4 DMA Channels

Table 13. DMA Channels

DMA Channel Number	Data Width	System Resource
0	8- or 16-bits	Open
1	8- or 16-bits	Parallel port
2	8- or 16-bits	Diskette drive
3	8- or 16-bits	Parallel port (for ECP or EPP)
4	8- or 16-bits	DMA controller
5	16-bits	Open
6	16-bits	Open
7	16-bits	Open

2.5 PCI Configuration Space Map

Table 14. PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	Description
00	00	00	Memory controller (of Intel 82820 component)
00	01	00	PCI to AGP bridge
00	1E	00	Link to PCI bridge
00	1F	00	PCI-to-LPC bridge
00	1F	01	IDE controller
00	1F	02	USB controller
00	1F	03	SMBus controller
01	00	00	AGP connector
02	08	00	PCI slot 1
02	09	00	PCI slot 2
02	0A	00	PCI slot 3
02	0B	00	PCI slot 4
02	0C	00	PCI slot 5

2.6 Interrupts

Table 15. Interrupts

IRQ	System Resource
NMI	I/O channel check
0	Reserved, interval timer
1	Reserved, keyboard buffer full
2	Reserved, cascade interrupt from slave PIC
3	COM2 (if enabled, else user available)
4	COM1 (if enabled, else user available)
5	LPT2 (Plug and Play option) / User available
6	Diskette drive
7	LPT1 (if enabled, else user available)
8	Real-time clock
9	Reserved for ICH system management bus
10	User available
11	User available
12	Onboard mouse port (if mouse used, else user available)
13	Reserved, math coprocessor
14	Primary IDE (if present, else user available)
15	Secondary IDE (if present, else user available)

2.7 PCI Interrupt Routing Map

This section describes interrupt sharing and how the interrupt signals are connected between the PCI bus connectors and onboard PCI devices. The PCI specification defines how interrupts can be shared between devices attached to the PCI bus. In most cases, the small amount of latency added by interrupt sharing does not affect the operation or throughput of the devices. In some special cases where maximum performance is needed from a device, a PCI device should not share an interrupt with other PCI devices. Use the following information to avoid sharing an interrupt with a PCI add-in board.

PCI devices are categorized as follows to specify their interrupt grouping:

- INTA: By default, all add-in boards that require only one interrupt are in this category. For almost all boards that require more than one interrupt, the first interrupt on the board is also classified as INTA.
- INTB: Generally, the second interrupt on add-in boards that require two or more interrupts is classified as INTB. (This is not an absolute requirement.)
- INTC and INTD: Generally, a third interrupt on add-in boards is classified as INTC and a fourth interrupt is classified as INTD.

The ICH PCI-to-LPC bridge has four programmable interrupt request (PIRQ) input signals. All PCI interrupt sources, either onboard or from a PCI add-in board, connect to one of these PIRQ signals. Because there are only four signals, some PCI interrupt sources are electrically tied together on the D820LP board and therefore share the same interrupt.

For example, using Table 16 as a reference, assume an add-in board using INTA is plugged into PCI bus connector 4. In PCI bus connector 4, INTA is connected to PIRQD. Since PIRQD is already connected to PCI audio and the ICH USB controller, the add-in board now shares interrupts with these onboard interrupt sources.

Table 16 lists the PIRQ signals used on the D820LP board and shows how the signals are connected to the PCI bus connectors and to the onboard PCI interrupt sources.

Table 16. PCI Interrupt Routing Map

PCI Interrupt Source	ICH PIRQ Signal Name			
	PIRQA	**PIRQB**	**PIRQC**	**PIRQD**
AGP Connector	INTA	INTB		
ICH SMBus		INTB		
ICH USB Controller				INTD
PCI Bus Connector 1 (J4E1)	INTA	INTB	INTC	INTD
PCI Bus Connector 2 (J4D1)	INTD	INTA	INTB	INTC
PCI Bus Connector 3 (J4C1)	INTC	INTD	INTA	INTB
PCI Bus Connector 4 (J4B1)	INTB	INTC	INTD	INTA
PCI Bus Connector 5 (J4A1)	INTC	INTD	INTA	INTB

NOTE

The ICH can connect each PIRQ line internally to one of the IRQ signals (3, 4, 5, 7, 9, 10, 11, 12, 14, and 15). Typically, a device that does not share a PIRQ line will have a unique interrupt. However, in certain interrupt-constrained situations, it is possible for two or more of the PIRQ lines to be connected to the same IRQ signal.

2.8 Connectors

CAUTION

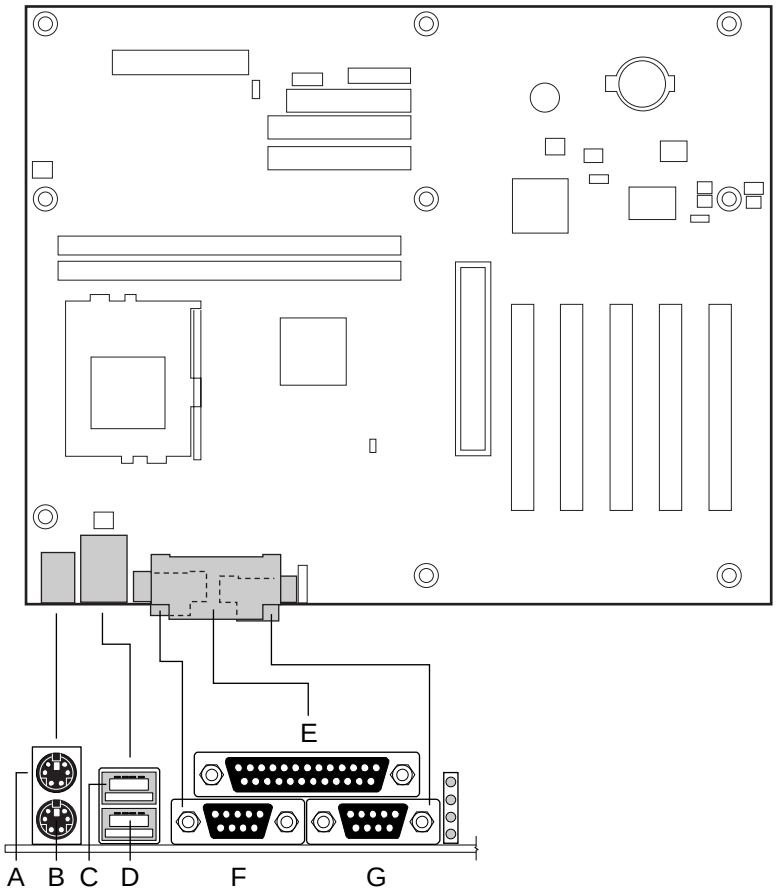
Only the back panel connectors of this D820LP board have overcurrent protection. The internal D820LP board connectors are not overcurrent protected, and should connect only to devices inside the computer's chassis, such as fans and internal peripherals. Do not use these connectors to power devices external to the computer's chassis. A fault in the load presented by the external devices could cause damage to the computer, the interconnecting cable, and the external devices themselves.

The board's connectors are divided into the following functional groups:

- Back panel (see page 46)
  - PS/2 mouse and keyboard
  - USB ports (2)
  - Parallel port
  - Serial ports (2)
- Peripheral interfaces and add-in boards (see page 48)
  - PCI bus add-in boards (5)
  - AGP
  - Diskette drive
  - Primary IDE
  - Secondary IDE
  - SCSI LED
- Hardware control and power (see page 54)
  - Processor fan (J7M1)
  - Chassis fans (2) (J2L1 and J8C1)
  - Power
  - Wake on LAN technology
  - Wake on Ring
  - Chassis intrusion
  - PC/PCI
- Front panel (see page 57)
  - Front panel connector
  - Auxiliary power LED
  - USB port 1

2.8.1 Back Panel Connectors

Figure 6 shows the location of the back panel connectors. The back panel connectors are color-coded in compliance with PC 99 recommendations. The figure legend below lists the colors used.



Item	Description	Color	For more information see:
A	PS/2 mouse	Lime Green	Table 17
B	PS/2 keyboard	Purple	Table 17
C	USB port 0	Black	Table 18
D	USB port 1	Black	Table 18
E	Parallel port	Burgundy	Table 19
F	Serial port A	Teal	Table 20
G	Serial port B	Teal	Table 20

Figure 6. Back Panel Connectors

Table 17. PS/2 Keyboard/Mouse Connectors

Pin	Signal Name
1	Data
2	No connect
3	Ground
4	+5 V (fused)
5	Clock
6	No connect

Table 18. USB Connectors

Pin	Signal Name
1	+5 V (fused)
2	USBP0# [USBP1#]
3	USBP0 [USBP1]
4	Ground

Signal names in brackets ([ ]) are for USB port 1.

Table 19. Parallel Port Connector

Pin	Standard Signal Name	ECP Signal Name	EPP Signal Name
1	STROBE#	STROBE#	WRITE#
2	PD0	PD0	PD0
3	PD1	PD1	PD1
4	PD2	PD2	PD2
5	PD3	PD3	PD3
6	PD4	PD4	PD4
7	PD5	PD5	PD5
8	PD6	PD6	PD6
9	PD7	PD7	PD7
10	ACK#	ACK#	INTR
11	BUSY	BUSY#, PERIPHACK	WAIT#
12	PERROR	PE, ACKREVERSE#	PE
13	SELECT	SELECT	SELECT
14	AUTOFD#	AUTOFD#, HOSTACK	DATASTB#
15	FAULT#	FAULT#, PERIPHREQST#	FAULT#
16	INIT#	INIT#, REVERSERQST#	RESET#
17	SLCTIN#	SLCTIN#	ADDRSTB#
18 - 25	GND	GND	GND

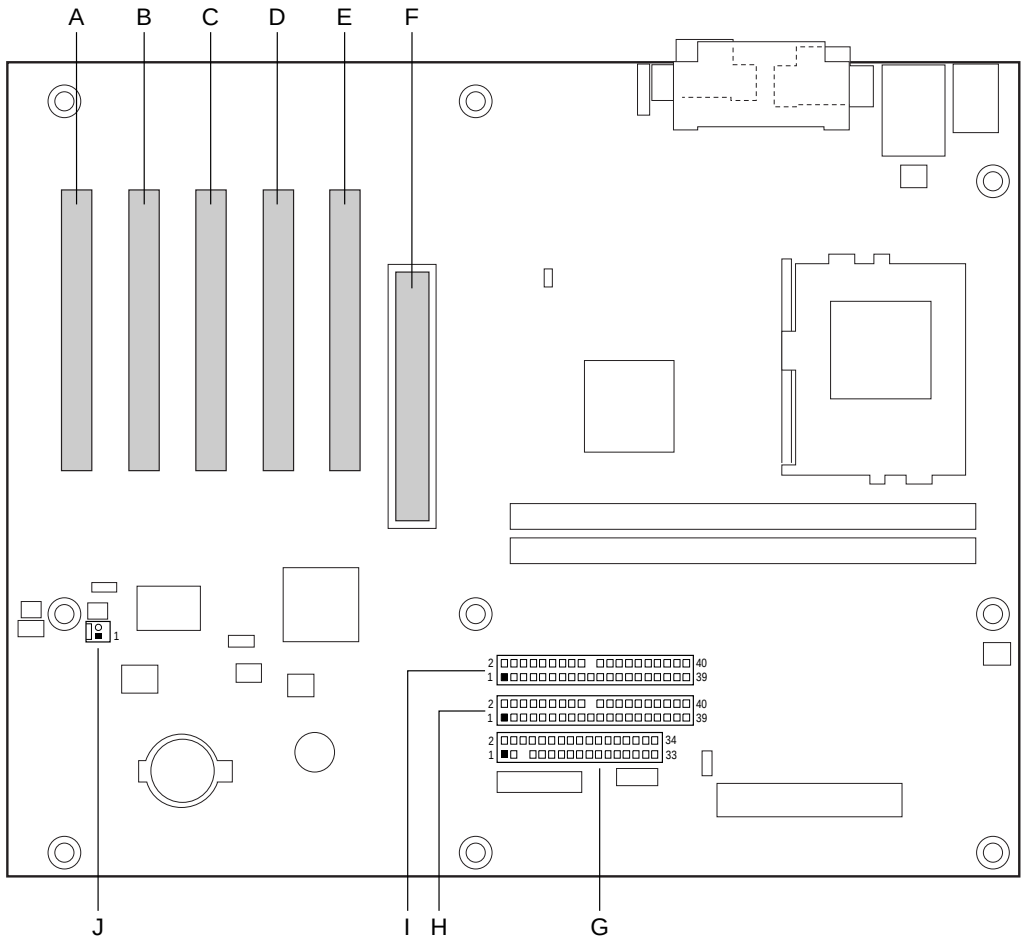
Table 20. Serial Port Connectors

Pin	Signal Name
1	DCD (Data Carrier Detect)
2	SIN# (Serial Data In)
3	SOUT# (Serial Data Out)
4	DTR (Data Terminal Ready)
5	Ground
6	DSR (Data Set Ready)
7	RTS (Request to Send)
8	CTS (Clear to Send)
9	RI (Ring Indicator)

2.8.2 Peripheral Interface and Add-in Board Connectors

Figure 7 shows the location of the peripheral interface and add-in board connectors. Note the following considerations for the PCI bus connectors:

- All of the PCI bus connectors are bus master capable.
- SMBus signals are routed to PCI bus connector J4D1. This enables PCI bus add-in boards with SMBus support to access sensor data on the D820LP board. The specific SMBus signals are as follows:
  - The SMBus clock line is connected to pin A40
  - The SMBus data line is connected to pin A41



Item	Description	Reference Designator
A	PCI bus connector 5 (see Table 21)	J4A1
B	PCI bus connector 4 (see Table 21)	J4B1
C	PCI bus connector 3 (see Table 21)	J4C1
D	PCI bus connector 2 (see Table 21)	J4D1
E	PCI bus connector 1 (see Table 21)	J4E1
F	AGP universal connector (see Table 22)	J5E1
G	Diskette drive connector (see Table 23)	J9G1
H	Primary IDE connector (see Table 24)	J8G2
I	Secondary IDE connector (see Table 24)	J8G1
J	SCSI LED connector (see Table 25)	J7B3

Figure 7. Peripheral Interface and Add-in Board Connectors

Table 21. PCI Bus Connectors (J4A1, J4B1, J4C1, J4D1, J4E1)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	Ground (TRST#) (Note 1)	B1	-12 V	A32	AD16	B32	AD17
A2	+12 V	B2	Ground (TCK) (Note 1)	A33	+3.3 V	B33	C/BE2#
A3	+5 V (TMS) (Note 1)	B3	Ground	A34	FRAME#	B34	Ground
A4	+5 V (TDI) (Note 1)	B4	No connect (TDO) (Note 1)	A35	Ground	B35	IRDY#
A5	+5 V	B5	+5 V	A36	TRDY#	B36	+3.3 V
A6	INTA#	B6	+5 V	A37	Ground	B37	DEVSEL#
A7	INTC#	B7	INTB#	A38	STOP#	B38	Ground
A8	+5 V	B8	INTD#	A39	+3.3 V	B39	LOCK#
A9	Reserved	B9	No connect (PRSNT1#) (Note 1)	A40	Reserved (Note 2)	B40	PERR#
A10	+5 V (I/O)	B10	Reserved	A41	Reserved (Note 3)	B41	+3.3 V
A11	Reserved	B11	No connect (PRSNT2#) (Note 1)	A42	Ground	B42	SERR#
A12	Ground	B12	Ground	A43	PAR	B43	+3.3 V
A13	Ground	B13	Ground	A44	AD15	B44	C/BE1#
A14	+3.3 V Aux	B14	Reserved	A45	+3.3 V	B45	AD14
A15	RST#	B15	Ground	A46	AD13	B46	Ground
A16	+5 V (I/O)	B16	CLK	A47	AD11	B47	AD12
A17	GNT#	B17	Ground	A48	Ground	B48	AD10
A18	Ground	B18	REQ#	A49	AD09	B49	Ground
A19	PME#	B19	+5 V (I/O)	A50	Key	B50	Key
A20	AD30	B20	AD31	A51	Key	B51	Key
A21	+3.3 V	B21	AD29	A52	C/BE0#	B52	AD08
A22	AD28	B22	Ground	A53	+3.3 V	B53	AD07
A23	AD26	B23	AD27	A54	AD06	B54	+3.3 V
A24	Ground	B24	AD25	A55	AD04	B55	AD05
A25	AD24	B25	+3.3 V	A56	Ground	B56	AD03
A26	IDSEL	B26	C/BE3#	A57	AD02	B57	Ground
A27	+3.3 V	B27	AD23	A58	AD00	B58	AD01
A28	AD22	B28	Ground	A59	+5 V (I/O)	B59	+5 V (I/O)
A29	AD20	B29	AD21	A60	REQ64#	B60	ACK64#
A30	Ground	B30	AD19	A61	+5 V	B61	+5 V
A31	AD18	B31	+3.3 V	A62	+5 V	B62	+5 V

Notes:

1. These signals (in parentheses) are optional in the PCI specification and are not currently implemented.
2. On PCI bus connector J4D1, this pin is connected to the SMBus clock line.
3. On PCI bus connector J4D1, this pin is connected to the SMBus data line.

Table 22. AGP Bus Connector (J5E1)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	+12V	B1	No Connect	A34	Vcc3.3	B34	Vcc3.3
A2	TYPEDET#	B2	Vcc	A35	AD22	B35	AD21
A3	Reserved	B3	Vcc	A36	AD20	B36	AD19
A4	No Connect	B4	No Connect	A37	Ground	B37	Ground
A5	Ground	B5	Ground	A38	AD18	B38	AD17
A6	INTA#	B6	INTB#	A39	AD16	B39	C/BE2#
A7	RST#	B7	CLK	A40	Vcc3.3	B40	Vcc3.3
A8	GNT1#	B8	REQ#	A41	FRAME#	B41	IRDY#
A9	Vcc3.3	B9	Vcc3.3	A42	Reserved	B42	+3.3 V Aux
A10	ST1	B10	ST0	A43	Ground	B43	Ground
A11	Reserved	B11	ST2	A44	Reserved	B44	Reserved
A12	PIPE#	B12	RBF#	A45	Vcc3.3	B45	Vcc3.3
A13	Ground	B13	Ground	A46	TRDY#	B46	DEVSEL#
A14	WBF#	B14	No Connect	A47	STOP#	B47	Vcc3.3
A15	SBA1	B15	SBA0	A48	PME#	B48	PERR#
A16	Vcc3.3	B16	Vcc3.3	A49	Ground	B49	Ground
A17	SBA3	B17	SBA2	A50	PAR	B50	SERR#
A18	SBSTB#	B18	SB_STB	A51	AD15	B51	C/BE1#
A19	Ground	B19	Ground	A52	Vcc3.3	B52	Vcc3.3
A20	SBA5	B20	SBA4	A53	AD13	B53	AD14
A21	SBA7	B21	SBA6	A54	AD11	B54	AD12
A22	Key	B22	Key	A55	Ground	B55	Ground
A23	Key	B23	Key	A56	AD9	B56	AD10
A24	Key	B24	+3.3 V Aux	A57	C/BE0#	B57	AD8
A25	Key	B25	Key	A58	Vcc3.3	B58	Vcc3.3
A26	AD30	B26	AD31	A59	AD_STB0#	B59	AD_STB0
A27	AD28	B27	AD29	A60	AD6	B60	AD7
A28	Vcc3.3	B28	Vcc3.3	A61	Ground	B61	Ground
A29	AD26	B29	AD27	A62	AD4	B62	AD5
A30	AD24	B30	AD25	A63	AD2	B63	AD3
A31	Ground	B31	Ground	A64	Vcc3.3	B64	Vcc3.3
A32	AD_STB1#	B32	AD_STB1	A65	AD0	B65	AD1
A33	C/BE3#	B33	AD23	A66	VRREFG_C	B66	VREFC_G

Table 23. Diskette Drive Connector (J9G1)

Pin	Signal Name	Pin	Signal Name
1	Ground	2	DENSEL
3	Ground	4	Reserved
5	Key	6	FDEDIN
7	Ground	8	FDINDX# (Index)
9	Ground	10	FDM00# (Motor Enable A)
11	Ground	12	No connect
13	Ground	14	FDDS0# (Drive Select A)
15	Ground	16	No connect
17	No connect	18	FDDIR# (Stepper Motor Direction)
19	Ground	20	FDSTEP# (Step Pulse)
21	Ground	22	FDWD# (Write Data)
23	Ground	24	FDWE# (Write Enable)
25	Ground	26	FDTRK0# (Track 0)
27	No connect	28	FDWPD# (Write Protect)
29	Ground	30	FDRDATA# (Read Data)
31	Ground	32	FDHEAD# (Side 1 Select)
33	Ground	34	DSKCHG# (Diskette Change)

Table 24. PCI IDE Connectors (Primary at J8G2 and Secondary at J8G1)

Pin	Signal Name	Pin	Signal Name
1	Reset IDE	2	Ground
3	Data 7	4	Data 8
5	Data 6	6	Data 9
7	Data 5	8	Data 10
9	Data 4	10	Data 11
11	Data 3	12	Data 12
13	Data 2	14	Data 13
15	Data 1	16	Data 14
17	Data 0	18	Data 15
19	Ground	20	Key
21	DDRQ0 [DDRQ1]	22	Ground
23	I/O Write#	24	Ground
25	I/O Read#	26	Ground
27	IOCHRDY	28	P_ALE (Cable Select Pullup)
29	DDACK0# [DDACK1#]	30	Ground
31	IRQ 14 [IRQ 15]	32	Reserved
33	DAG1 (Address 1)	34	GPIO_DMA66_Detect_Pri (GPIO_DMA66_Detect_Sec)
35	DAG0 (Address 0)	36	DAG2 (Address 2)
37	Chip Select 1P# [Chip Select 1S#]	38	Chip Select 3P# [Chip Select 3S#]
39	Activity#	40	Ground

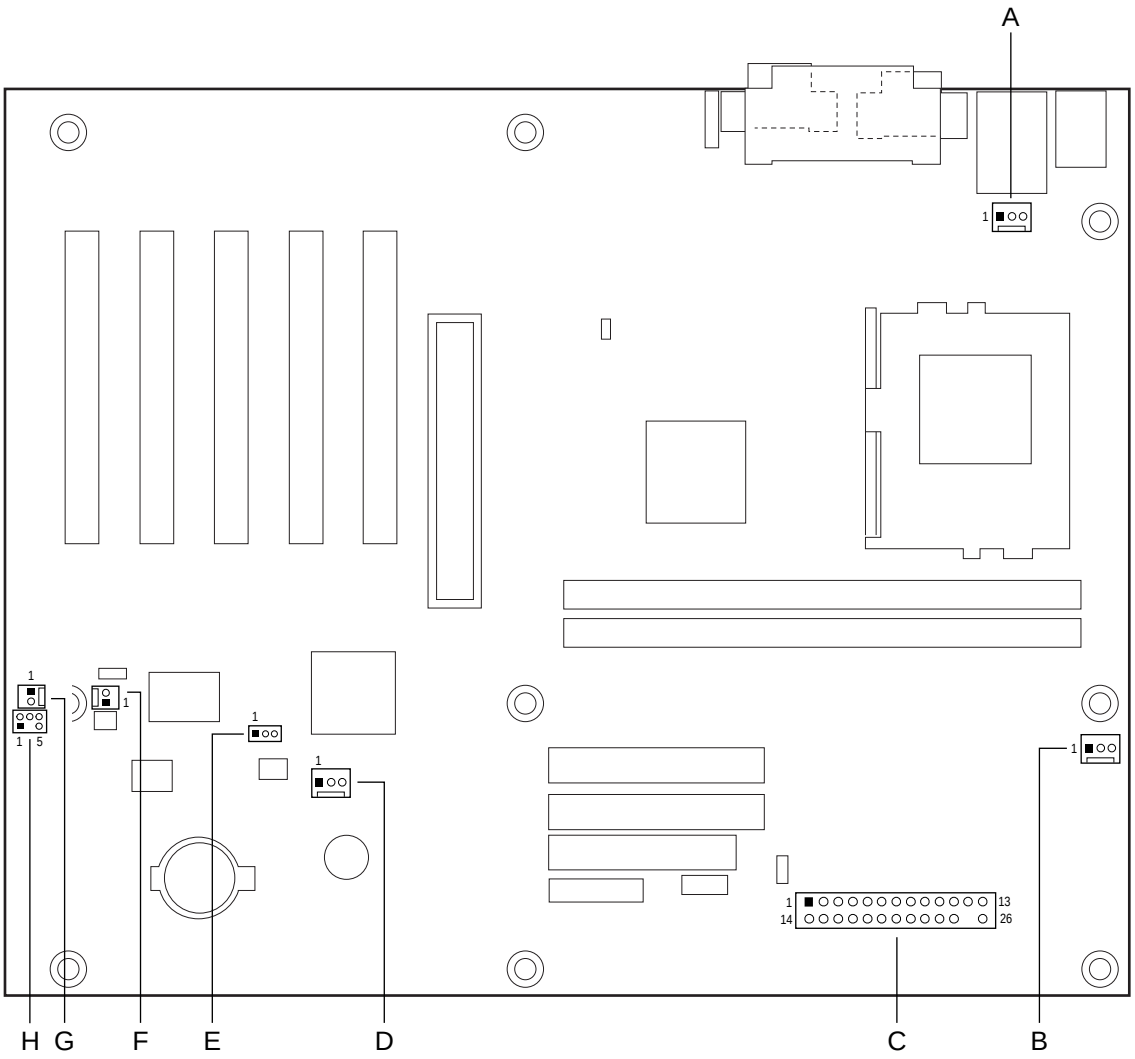
Note: Signal names in brackets ([ ]) are for the secondary IDE connector.

Table 25. SCSI LED Connector (J7B3)

Pin	Signal Name
1	SCSI activity
2	No connect

2.8.3 Hardware Control and Power

Figure 8 shows the location of the hardware control and power connectors.



Item	Description	Reference Designator
A	Chassis fan (see Table 26)	J2L1
B	Processor fan (see Table 27)	J7M1
C	Power (see Table 28)	J9K1
D	Chassis fan (see Table 29)	J8D1
E	Wake on LAN technology (see Table 30)	J7C1
F	Wake on Ring (see Table 31)	J7B2
G	Chassis intrusion (see Table 32)	J7A1
H	PC / PCI (see Table 33)	J7A2

Figure 8. Hardware Control and Power Connectors

For information about	Refer to
The power connector	Section 1.9.2.1, page 34
The functions of the fan connectors	Section 1.9.2.2, page 34
Wake on LAN technology	Section 1.9.2.3, page 35
Wake on Ring technology	Section 1.9.2.5, page 37

Table 26. Chassis Fan Connector (J2L1)

Pin	Signal Name
1	Fan Control (Note)
2	+12 V
3	Fan Tachometer (Note)

Note: As a manufacturing option, the fan is not monitored and is always powered on when the computer is powered on. With this option, the connector signals are the same as those in Table 29.

Table 27. Processor Fan Connector (J7M1)

Pin	Signal Name
1	Fan Control (Note)
2	+12 V
3	Fan Tachometer (Note)

Note: As a manufacturing option, the fan is not monitored and is always powered on when the computer is powered on. With this option, the connector signals are the same as those in Table 29.

Table 28. Power Connector (J9K1)

Pin	Signal Name	Pin	Signal Name
1	+3.3 V	11	+3.3 V
2	+3.3 V	12	-12 V
3	Ground	13	Ground
4	+5 V	14	PS-ON# (power supply remote on/off)
5	Ground	15	Ground
6	+5 V	16	Ground
7	Ground	17	Ground
8	PWRGD (Power Good)	18	-5 V
9	+5 V (Standby)	19	+5 V
10	+12 V	20	+5 V

Table 29. Chassis Fan Connector (J8D1)

Pin	Signal Name
1	Ground
2	+12 V
3	Ground

Table 30. Wake on LAN Technology Connector (J7C1)

Pin	Signal Name
1	+5 VSB
2	Ground
3	WOL

Table 31. Wake on Ring Connector (J7B2)

Pin	Signal Name
1	Ground
2	RINGA#

Table 32. Chassis Intrusion Connector (J7A1)

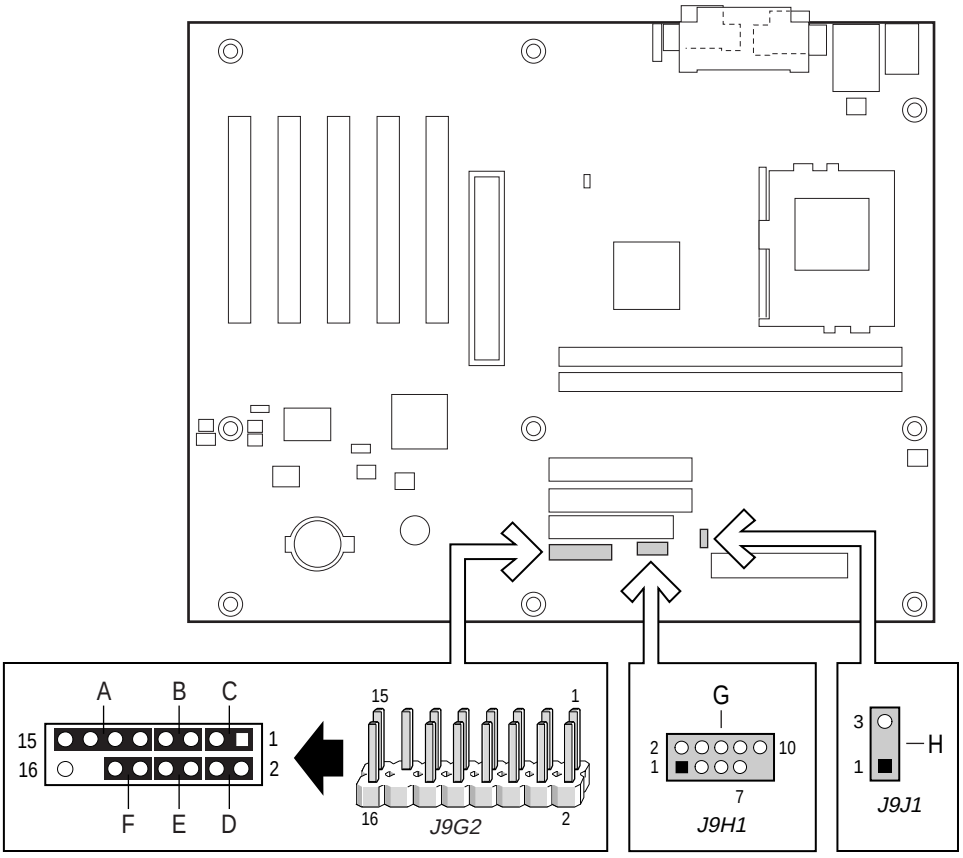
Pin	Signal Name
1	INTRUDER#
2	Ground

Table 33. PC/PCI Connector (J7A2)

Pin	Signal Name
1	P_PCIGNTA In
2	Ground
3	No connection
4	P_PCIREQA Out
5	Ground
6	SER_IRQ Out

2.8.4 Front Panel Connectors

Figure 9 shows the location of the front panel connectors.



	Item	Pins	Description
Front panel connector (see Table 34)	A	9, 11, 13, and 15	Infrared port
	B	5 and 7	Reset switch
	C	1 and 3	Hard drive activity LED
	D	2 and 4	Power / Sleep / Message Waiting LED
	E	6 and 8	Power switch
	F	10 and 12	No connect
Front USB connector (see Table 37)	G	1-7, 9-10	USB port 1 (dependent on setting of the USB routing jumper; see Table 41)
Auxiliary front panel power LED connector (see Table 38)	H	1 and 3	Auxiliary power LED connector

Figure 9. Front Panel Connectors

2.8.4.1 Front Panel Connector

The front panel connector is a central connecting point for five connectors, all of which can be attached at the same time. The front panel connector supports the following functions:

- Infrared port
- Reset switch
- Hard drive activity LED
- Power / Sleep / Message Waiting LED
- Power switch

Table 34 lists the signal names of the front panel connector. The paragraphs that follow describe the functions supported by the connector.

Table 34. Front Panel Connector (J9G2)

Pin	Signal	In/Out	Description	Pin	Signal	In/Out	Description
1	HD_PWR	Out	Hard disk LED pullup (330 Ω) to +5 V	2	HDR_BLNK_ GRN	Out	Front panel green LED
3	HDA#	Out	Hard disk active LED	4	HDR_BLNK_ YEL	Out	Front panel yellow LED
5	GND		Ground	6	SW_ON#	In	Power switch
7	FP_RESET#	In	Reset switch	8	GND		Ground
9	+5 V	Out	IR Power	10	N/C		
11	IRRX	In	IrDA serial input	12	GND		Ground
13	GND		Ground	14	(pin removed)		No connect
15	IRTX	Out	IrDA serial output	16	+5 V	Out	Power

2.8.4.1.1 Infrared Port Connector

Serial port B can be configured to support an IrDA module connected to pins 9, 11, 13, and 15.

For information about	Refer to
Infrared support	Section 1.7.2, page 27
Configuring serial port B for infrared applications	Section 4.4.3, page 92

2.8.4.1.2 Reset Switch Connector

Pins 5 and 7 can be connected to a momentary SPST type switch that is normally open. When the switch is closed, the D820LP board resets and runs POST.

2.8.4.1.3 Hard Drive Activity LED Connector

Pins 1 and 3 can be connected to an LED to provide a visual indicator that data is being read from or written to a hard drive. For the LED to function properly, an IDE drive must be connected to the onboard IDE interface. The LED will also show activity for devices connected to the SCSI hard drive activity LED connector.

For information about	Refer to
The SCSI hard drive activity LED connector	Section 1.6.3.2, page 25

2.8.4.1.4 Power / Sleep / Message Waiting LED Connector

Pins 2 and 4 can be connected to a single- or dual-colored LED. Table 35 shows the possible states for a single-colored LED.

Table 36 shows the possible states for a dual-colored LED.

Table 35. States for a Single-colored Power LED

LED State	Description
Off	Power off/sleeping
Steady Green	Running
Blinking Green	Running/message waiting

Table 36. States for a Dual-colored Power LED

LED State	Description
Off	Power off
Steady Green	Running
Blinking Green	Running/message waiting
Steady Yellow	Sleeping
Blinking Yellow	Sleeping/message waiting

NOTE

To use the message waiting function, ACPI must be enabled in the operating system and a message-capturing application must be invoked.

2.8.4.1.5 Power Switch Connector

Pins 6 and 8 can be connected to a front panel momentary-contact power switch. The switch must pull pin 6 to ground for at least 50 ms to signal the power supply to switch on or off. (The time requirement is due to internal debounce circuitry on the D820LP board.) At least two seconds must pass before the power supply will recognize another on/off signal.

2.8.4.2 Front USB Connector (Optional)

This connector is used if the chassis has a front panel USB connector. The onboard jumper block at J8C1 can be set to route USB port 1 signals to the onboard front USB connector. This connector can then be cabled to the chassis' front panel connector.

Table 37. Front USB Connector (J9H1)

Pin	Signal Name
1	USB_FNT_PWR
2	USB_FNT_PWR
3	USBP1#
4	No connect
5	USBP1
6	No connect
7	Ground
8	Ground
9	No connect
10	USB_FNT_OC#

For information about	Refer to
The location of the USB port 1 routing jumper block	Figure 10, page 61
Setting the USB port 1 routing jumper block	Table 41, page 63

2.8.4.3 Auxiliary Front Panel Power LED Connector

This connector duplicates the signals on pins 2 and 4 of the front panel connector.

Table 38. Auxiliary Front Panel Power LED Connector (J9J1)

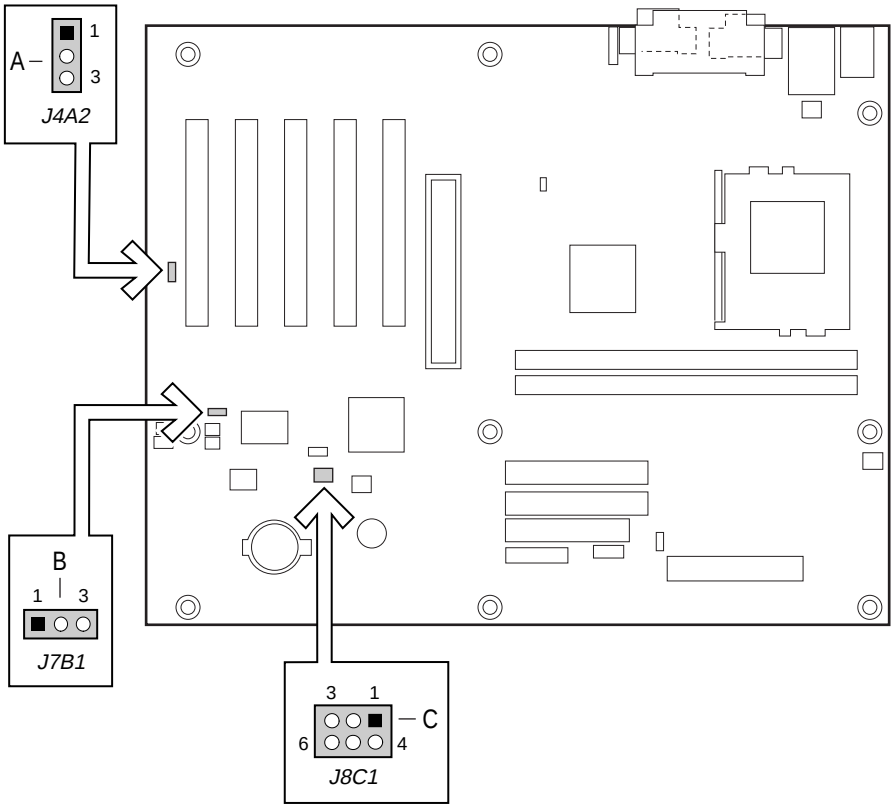
Pin	Signal Name	In/Out	Description
1	HDR_BLNK_GRN	Out	Front panel green LED
2	No connect		
3	HDR_BLNK_YEL	Out	Front panel yellow LED

2.9 Jumper Blocks

CAUTION

Do not move any jumper with the power ON. Always turn the power off and unplug the power cord from the computer before changing a jumper setting. Otherwise, damage to the D820LP board could occur.

The D820LP board has the jumper blocks shown in Figure 10.



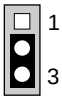
Item	Description	Reference Designator
A	S5 remote control jumper block	J4A2
B	BIOS Setup configuration jumper block	J7B1
C	USB port 1 routing jumper block (optional)	J8C1

Figure 10. Location of the Jumper Blocks

2.9.1 S5 Remote Control Jumper Block

Table 39 describes jumper block J4A2 that provides user-control over system wake events. If the jumper is set to connect pins 1-2 (default), the system resumes from an S5 state when a PME# or Wake on LAN technology event is asserted. If the jumper is set to connect pins 2-3, the system will no longer resume from an S5 state. This feature is useful if, for example, the user does not wish their dial-up modem to wake their previously powered-off computer whenever the telephone rings. The jumper setting does not affect S3 resume events.

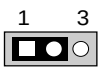
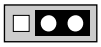
Table 39. S5 Remote Control Jumper Settings (J4A2)

Function/Mode	Jumper Setting		Configuration
Enable S5 Wake Events	1-2	 1 3 (default)	System will resume from an S5 state when a PME# or Wake on LAN technology event is asserted.
Disable S5 Wake Events	2-3	 1 3	System will NOT resume from an S5 state when a PME# or Wake on LAN technology event is asserted.

2.9.2 BIOS Setup Configuration Jumper Block

Table 40 describes the jumper settings for the three BIOS setup configuration modes: normal, configure, and recovery. This 3-pin jumper block determines the BIOS Setup program's mode.

Table 40. BIOS Setup Configuration Jumper Settings (J7B1)

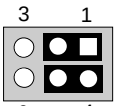
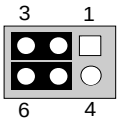
Function/Mode	Jumper Setting		Configuration
Normal	1-2	 1 3	The BIOS uses current configuration information and passwords for booting.
Configure	2-3	 1 3	After the POST runs, Setup runs automatically. The Maintenance menu is displayed.
Recovery	None	 1 3	The BIOS attempts to recover the BIOS configuration. A recovery diskette is required.

For information about	Refer to
How to access the BIOS Setup program	Section 4.1, page 85
The Maintenance menu of the BIOS Setup program	Section 4.2, page 86
BIOS recovery	Section 3.6, page 80

2.9.3 USB Port 1 Routing Jumper Block (Optional)

Table 41 describes the settings of optional jumper block J8C1. This jumper block routes the USB port 1 signals to either the bottom back-panel USB connector or to connector J9H1 near the front of the board. If the chassis has a front panel USB connector, it can then be cabled to the onboard connector at J9H1.

Table 41. Settings for the Optional USB Port 1 Routing Jumper Block (J8C1)

Function/Mode	Jumper Setting		Configuration
Back Panel USB Port 1	1-2 4-5	 (default)	Routes USB port 1 to the top back-panel USB connector.
Front USB Port 1	2-3 5-6		Routes USB port 1 to connector J9H1 near the front of the board. If the chassis has a front panel USB connector, it can then be cabled to the onboard connector at J9H1.

For information about	Refer to
The location of the onboard front USB connector	Figure 9, page 57
The signal names of the onboard front USB connector	Table 37, page 60

2.10 Mechanical Considerations

2.10.1 Form Factor

The D820LP board is designed to fit into an ATX-form-factor chassis. Figure 11 illustrates the mechanical form factor for the D820LP board. Dimensions are given in inches [millimeters]. The outer dimensions are 9.60 inches by 12.00 inches. Location of the I/O connectors and mounting holes are in compliance with the ATX specification (see Section 1.3).

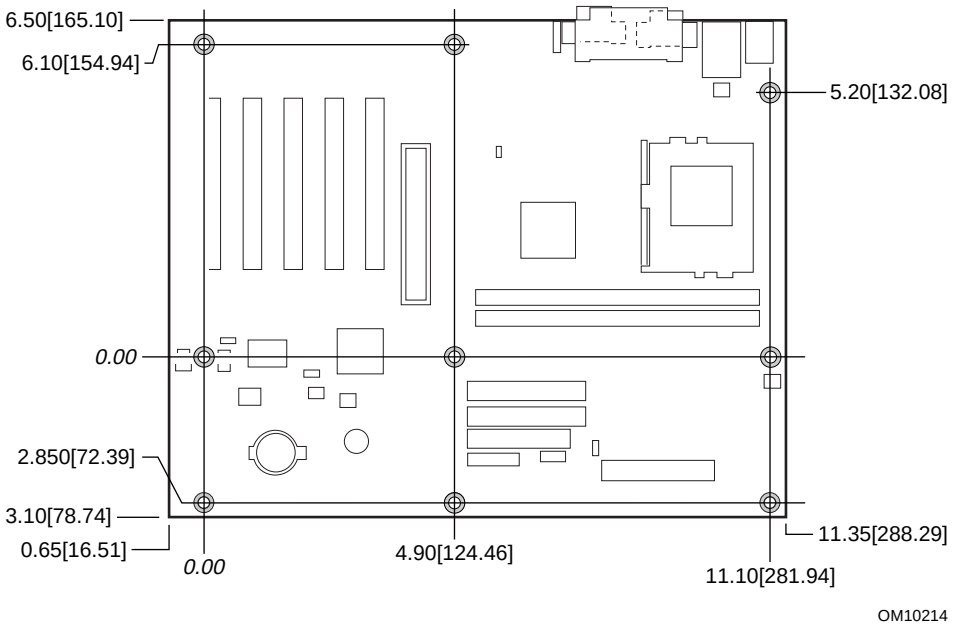


Figure 11. D820LP Board Dimensions

2.10.2 I/O Shield

The back panel I/O shield for the D820LP board must meet specific dimension and material requirements. Systems based on this D820LP board need the back panel I/O shield to pass certification testing. Figure 12 shows the critical dimensions of the I/O shield. Dimensions are given in inches. For dimensions given to two decimal places, the tolerance is ±0.02 inches unless otherwise noted. The figure also indicates the position of each cutout. Additional design considerations for I/O shields relative to chassis requirements are described in the ATX specification. See Section 1.3 for information about the ATX specification.

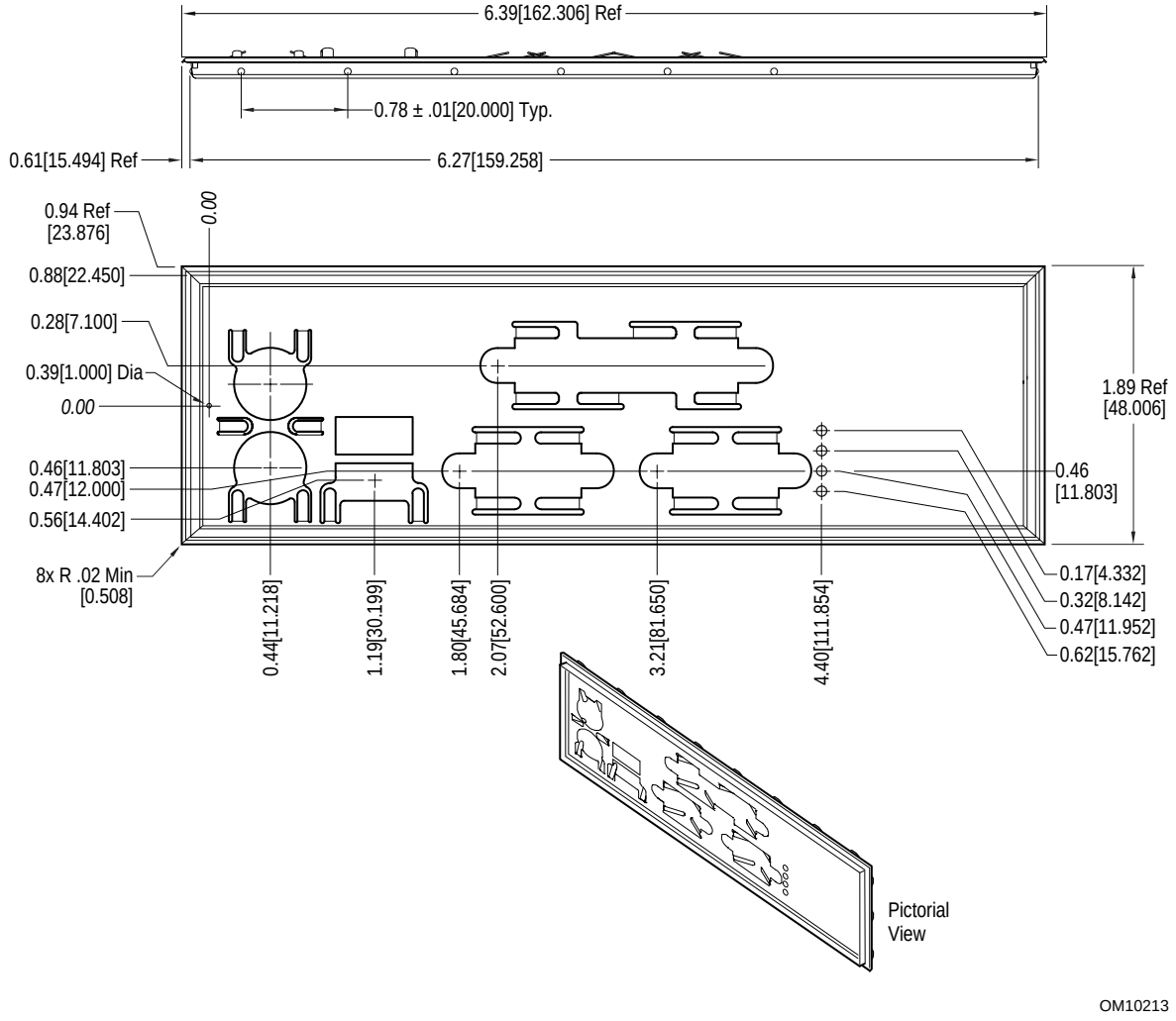


Figure 12. I/O Shield Dimensions

2.11 Electrical Considerations

2.11.1 Power Consumption

Table 42 lists typical power usage measurements for a desktop computer that contains the D820LP board and the following:

- 677 MHz Intel Pentium III processor with a 256 KB cache
- 192 MB PC800 RDRAM
- 3.5-inch diskette drive
- 1.2 GB IDE hard disk drive
- 34X IDE CD-ROM drive

This information is provided only as a guide for calculating approximate power usage with additional resources added.

Values for the Windows 98 SE desktop mode are measured at 1024 x 768 x 32bpp colors and 75 Hz refresh rate. AC watts are measured with a typical 145 W power supply meeting ATX version 2.01 specifications, nominal input voltage and frequency, and using a true RMS wattmeter at the line input.

NOTE

Actual system power consumption depends upon system configuration. The power supply should comply with the recommendations found in the ATX Form Factor Specification document (see Table 3 on page 16 for specification information).

Table 42. Typical Power Usage

Using Windows 98 SE and Power Management Mode	APM Full On (Idle)	APM Suspend	ACPI S0 Idle	ACPI S1	ACPI S3	ACPI S5
AC Watts	30.30 W	25.80 W	29.65 W	26.30 W	2.58 W	2.32 W

All measurements were made at nominal input voltage and frequency with a true RMS wattmeter connected to the power supply's line input.

Table 43 lists the maximum current required for each power supply voltage. Although not seen continuously, these peak values may occur during normal operation. Power supplies chosen for the D820LP board should be able to meet the maximum power supply current requirements, plus any additional system and add-in board requirements.

Table 43. Maximum Power Supply Current Requirements

DC Voltage	+3.3 V	+5 V	+12 V	-12 V	+5 VSB
Maximum Current	8.51 A	11.2 A	1.4 A	0.05 A	See Table 45, page 68

2.11.2 Add-in Board Considerations

The D820LP board has six slots for add-in boards: five PCI slots and one AGP slot. The maximum power used by any PCI slot (from all voltage sources) should not exceed 25 W. The total current load for all slots should not exceed 14 A. Table 44 lists the maximum current load for PCI add-boards from all voltage sources.

Table 44. Maximum PCI Add-in Board Current Load

Power Rail	+3.3 V	+5 V	+12 V	-12 V
Maximum Current	7.6 A	5.0 A	500 mA	100 mA

2.11.3 Standby Current Requirements

⚠ CAUTION

If the standby current necessary to support multiple wake events from the PCI and/or USB buses exceeds power supply capacity, the D820LP board may lose register settings stored in memory, etc. Calculate the standby current requirements using the steps described below.

To support the Instantly Available (ACPI S3 sleep state) configuration listed in Table 45, power supplies used with the D820LP desktop board must provide enough standby current.

Approximate values can be determined by specifications such as PCI 2.2. Actual measured values may vary.

To estimate the total amount of standby current required for a particular system configuration, add together the standby current requirements of all installed components. Refer to Table 45 and follow these steps:

1. Note the total D820LP desktop board standby current requirement.
2. Add to that the total PS/2 port standby current requirement if a wake enabled device is attached to the bottom PS/2 connector.
3. Add, from the PCI 2.2 slots (wake enabled) row, the total number of wake enabled devices installed (PCI and AGP) and multiply by the standby current requirement.
4. Add, from the PCI 2.2 slots (non-wake enabled) row, the total number of non-wake enabled devices installed (PCI and AGP) and multiply by the standby current requirement.
5. Add all additional wake enabled devices' and non-wake enabled devices' standby current requirements as applicable.
6. Add all the required current totals from steps 1 through 5 to determine the total estimated standby current power supply requirement.

Table 45. Standby Current Requirements

Instantly Available Current Support	Description	Standby Current Requirements (mA)
Estimate for integrated board components	Total for the D820LP board	200
Estimate for add-on components (Add to integrated board components shown above)	PS/2 ports (Note)	345
	PCI 2.2 slots (wake enabled)	375
	PCI 2.2 slots (non-wake enabled)	20
	WOL header	225
	USB ports (Note)	507.5 (maximum for both ports)

Note: Dependent upon system configuration

NOTE

The standby current requirements listed in Table 45 were derived from the following:

IBM PS/2 Port Specification (Sept 1991) states

- *275 mA for keyboard*
- *70 mA for the mouse (not wake-enable device)*

PCI/AGP requirements are calculated by totaling the following:

- *One wake enabled device @ 375 mA*
- *Non-wake enabled devices @ 20 mA each*

USB requirements are calculated as:

- *One USB wake enabled device @ 500 mA*
- *Three USB non-wake enabled devices @ 2.5 mA each*

NOTE

Both USB ports are capable of providing up to 500 mA during normal G0/S0 operation. Only one USB port will support up to 500 mA of stand-by current (wake enabled device) during G1/S3 suspended operation. The other port may provide up to 7.5 mA (three non-wake enabled devices only) during G1/S3 suspended operation.

2.11.4 Fan Current Requirements

The D820LP Desktop Board is capable of supplying 250 mA per fan connector (maximum).

2.11.5 Power Supply Considerations

⚠ CAUTION

The 5 V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to do so can damage the power supply. The total amount of standby current required depends on the wake devices supported. Refer to Section 2.11.3 on page 67 for additional information.

System integrators should refer to the power usage values listed in Table 42 and Table 43 when selecting a power supply for use with this D820LP board.

Measurements account only for current sourced by the D820LP board while running in idle modes of the started operating systems.

Additional power required will depend on configurations chosen by the integrator.

The power supply must comply with the following recommendations found in the indicated sections of the ATX form factor specification.

- The potential relation between 3.3 VDC and +5 VDC power rails (Section 4.2)
- The current capability of the +5 VSB line (Section 4.2.1.2)
- All timing parameters (Section 4.2.1.3)
- All voltage tolerances (Section 4.2.2)

For information about	Refer to
The ATX form factor specification	Section 1.3, page 16

2.12 Thermal Considerations

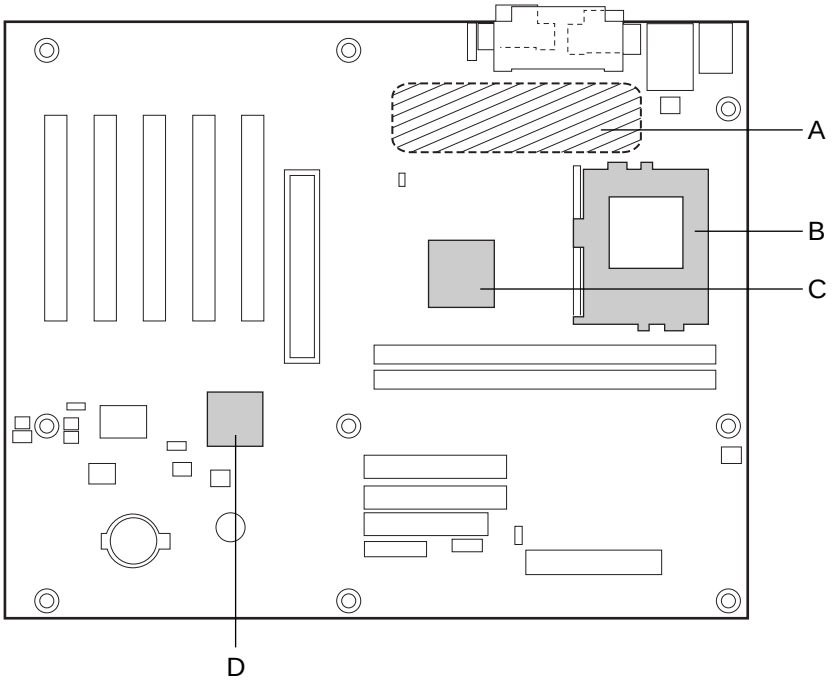
CAUTION

An ambient temperature that exceeds the D820LP board's maximum operating temperature by 5 °C to 10 °C could cause components to exceed their maximum case temperature and malfunction. For information about the maximum operating temperature, see the environmental specifications in Section 2.14.

CAUTION

System integrators should ensure that proper airflow is maintained in the voltage regulator circuit. The voltage regulator area can reach a temperature of up to 85 °C in an open chassis (item A in Figure 13). Failure to do so may result in damage to the voltage regulator circuit.

Figure 13 shows the locations of the board's high temperature zones.



A	Processor voltage regulator area
B	Processor
C	Intel 82820 MCH
D	Intel 82801AA ICH

Figure 13. High Temperature Zones

Table 46 provides maximum case temperatures for D820LP board components that are sensitive to thermal changes. Case temperatures could be affected by the operating temperature, current load, or operating frequency. Maximum case temperatures are important when considering proper airflow to cool the D820LP board.

Table 46. Thermal Considerations for Components

Component Type	Maximum Component Temperature
Intel 82820 MCH	110 °C
Intel 82801AA ICH	100 °C
Pentium III processor	Refer to the processor data sheet and specification updates at this Intel Web site: http://www.intel.com/design/litcentr

2.13 Reliability

The mean time between failures (MTBF) prediction is calculated using component and subassembly random failure rates. The calculation is based on the Bellcore Reliability Prediction Procedure, TR-NWT-000332, Issue 4, September 1991. The MTBF prediction is used to estimate repair rates and spare parts requirements.

The Mean Time Between Failures (MTBF) data is calculated from predicted data at 55 ºC.

D820LP board MTBF: 126,563.69 hours

2.14 Environmental

Table 47 lists the environmental specifications for the D820LP board.

Table 47. D820LP Board Environmental Specifications

Parameter	Specification		
Temperature			
Non-operating	-40 °C to +70 °C		
Operating	0 °C to +55 °C		
Shock			
Unpackaged	30 g trapezoidal waveform		
	Velocity change of 170 inches/second		
Packaged	Half sine 2 millisecond		
	Product Weight (pounds)	Free Fall (inches)	Velocity Change (inches/sec)
	<20	36	167
	21-40	30	152
	41-80	24	136
	81-100	18	118
Vibration			
Unpackaged	5 Hz to 20 Hz : 0.01 g^2 Hz sloping up to 0.02 g^2 Hz		
	20 Hz to 500 Hz : 0.02 g^2 Hz (flat)		
Packaged	10 Hz to 40 Hz : 0.015 g^2 Hz (flat)		
	40 Hz to 500 Hz : 0.015 g^2 Hz sloping down to 0.00015 g^2 Hz		

2.15 Regulatory Compliance

This section describes the D820LP board's compliance with safety and EMC regulations.

2.15.1 Safety Regulations

Table 48 lists the safety regulations with which the D820LP board complies when it is correctly installed in a compatible host system.

Table 48. Safety Regulations

Regulation	Title
UL 1950/CSA950, 3rd edition, Dated 07-28-95	Bi-National Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (USA and Canada)
EN 60950, 2nd Edition, 1992 (with Amendments 1, 2, 3, and 4)	The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (European Community)
IEC 950, 2nd edition, 1991 (with Amendments 1, 2, 3, and 4)	The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (International)
EMKO-TSE (74-SEC) 207/94	Summary of Nordic deviations to EN 60950. (Norway, Sweden, Denmark, and Finland)

2.15.2 EMC Regulations

Table 49 lists the EMC regulations with which D820LP board complies with when it is correctly installed in a compatible host system.

Table 49. EMC Regulations

Regulation	Title
FCC Class B	Title 47 of the Code of Federal Regulations, Parts 2 and 15, Subpart B, pertaining to unintentional radiators. (USA)
CISPR 22, 2nd Edition, 1993 (Class B)	Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (International)
VCCI Class B (ITE)	Implementation Regulations for Voluntary Control of Radio Interference by Data Processing Equipment and Electronic Office Machines. (Japan)
EN55022 (1994) (Class B)	Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (Europe)
EN50082-1 (1992)	Generic Immunity Standard; Currently compliance is determined via testing to IEC 801-2, -3, and -4. (Europe)
ICES-003 (1997)	Interference-Causing Equipment Standard, Digital Apparatus, Class B (Including CRC c.1374). (Canada)
AS/NZ 3548	Australian Communications Authority (ACA), Standard for Electromagnetic Compatibility.

2.15.3 Certification Markings

This printed circuit assembly has the following markings related to product certification:

- UL Joint Recognition Mark: Consists of small c followed by a stylized backward UR and followed by a small US (Component side)
- Manufacturer's recognition mark: Consists of a unique UL recognized manufacturer's logo, along with a flammability rating (94V-0) (Solder side)
- UL File Number for D820LP boards: E139761 (Component side)
- PB Part Number: Intel bare circuit board part number (Solder side) A06300-001
- Battery "+ Side Up" marking: located on the component side of the D820LP board in close proximity to the battery holder
- FCC Logo/Declaration: (Solder side)
- ACA (C-Tick) mark: Consists of a unique letter C, with a tick mark; followed by N-232. Located on the component side of the D820LP board and on the shipping container
- CE Mark: (Component side) The CE mark should also be on the shipping container

3 Overview of BIOS Features

What This Chapter Contains

3.1 Introduction

The D820LP board uses an Intel/AMI BIOS, which is stored in flash memory and can be upgraded using a disk-based program. In addition to the BIOS, the flash memory contains the BIOS Setup program, POST, APM, the PCI auto-configuration utility, and Plug and Play support.

This D820LP board supports system BIOS shadowing, allowing the BIOS to execute from 64-bit onboard write-protected DRAM.

The BIOS displays a message during POST identifying the type of BIOS and a revision code. On the D820LP board, this identifier is VC82010A.86A because the board uses the same BIOS as the Intel® Desktop Board VC820. The two boards can be differentiated by reading the Desktop Management Interface (DMI) entry. On the D820LP board, the DMI entry reports the board as D820LP.

For information about	Refer to
The D820LP board's compliance level with APM and Plug and Play	Section 1.3, page 16

3.2 BIOS Flash Memory Organization

The Intel 82802AB Firmware Hub (FWH) includes a 4 Mbit (512 KB) symmetrical flash memory device. Internally, the device is grouped into eight 64-KB blocks that are individually erasable, lockable, and unlockable. Figure 14 shows the organization of the flash memory.

The last two 8 KB blocks of the fault tolerance area are the parameter blocks. These blocks contain data such as BIOS updates, vital product data (VPD), logo, System Management BIOS (SMBIOS) interface, and extended system configuration data (ESCD) information. The backup block contains a copy of the fault tolerance block.

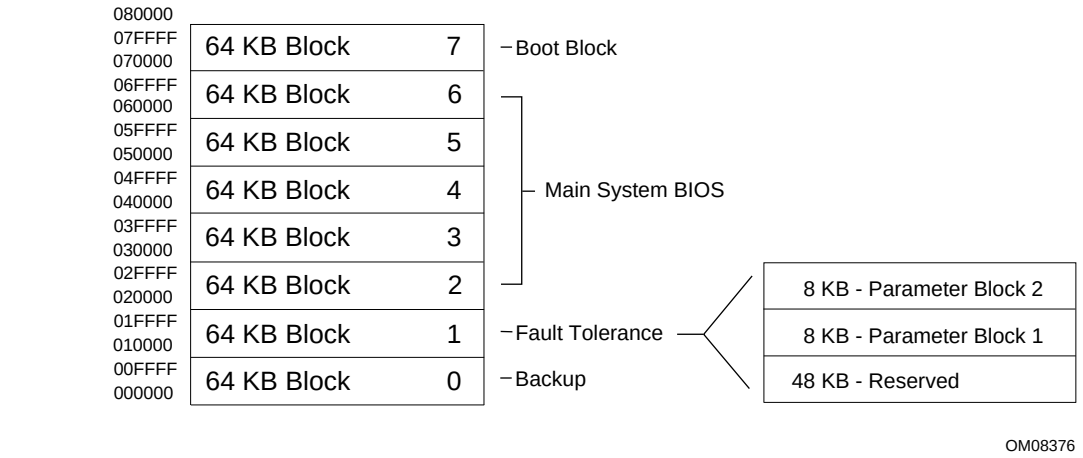


Figure 14. Memory Map of the Flash Memory Device

3.3 Resource Configuration

3.3.1 PCI Autoconfiguration

The BIOS can automatically configure PCI devices. PCI devices may be onboard or add-in boards. Autoconfiguration lets a user insert or remove PCI boards without having to configure the system. When a user turns on the system after adding a PCI board, the BIOS automatically configures interrupts, the I/O space, and other system resources. Any interrupts set to Available in Setup are considered to be available for use by the add-in board.

PCI interrupts are distributed to available ISA interrupts that have not been assigned to system resources. The assignment of PCI interrupts to ISA IRQs is non-deterministic. PCI devices can share an interrupt, but an ISA device cannot share an interrupt allocated to PCI or to another ISA device. Autoconfiguration information is stored in ESCD format.

For information about the versions of PCI and Plug and Play supported by the BIOS, see Section 1.3.

3.3.2 PCI IDE Support

If you select Auto in the BIOS Setup program, the BIOS automatically sets up the two PCI IDE connectors with independent I/O channel support. The IDE interface supports hard drives up to Ultra ATA/66 and recognizes any ATAPI devices, including CD-ROM drives, tape drives, and Ultra DMA drives (see Section 1.3 for the supported version of ATAPI). The BIOS determines the capabilities of each drive and configures them to optimize capacity and performance.

To take advantage of the high capacities typically available today, hard drives are automatically configured for Logical Block Addressing (LBA) and to PIO Mode 3 or 4, depending on the capability of the drive. You can override the auto-configuration options by specifying manual configuration in the BIOS Setup program.

NOTE

Do not connect an ATA device as a slave on the same IDE cable as an ATAPI master device. For example, do not connect an ATA hard drive as a slave to an ATAPI CD-ROM drive.

The D820LP board uses Host Detect to sense Ultra ATA/66 cables and hard drives. Additionally, this feature needs to be enabled in the operating system. (In Windows 98, for example, enable DMA in the Device Manager.)

To use Ultra ATA/66 features the following items are required:

- An Ultra ATA/66 peripheral device
- An Ultra ATA/66 compatible cable
- Operating system support for Ultra ATA/66
- Device driver support for Ultra ATA/66

NOTES

Ultra ATA-66 compatible cables are backward compatible with drives using slower IDE transfer protocols.

Some Ultra ATA/66 drivers do not support unique DMA speed settings for two hard drives connected to the same IDE interface (on the same cable). In this case, hard drives should be connected to different IDE interfaces through two separate cables to ensure the Ultra ATA/66 hard drives achieve maximum performance.

3.4 System Management BIOS (SMBIOS)

SMBIOS is a DMI-compliant method for managing computers in a managed network.

The main component of SMBIOS is the management information format (MIF) database, which contains information about the computing system and its components. Using SMBIOS, a system administrator can obtain the system types, capabilities, operational status, and installation dates for system components. The MIF database defines the data and provides the method for accessing this information. The BIOS enables applications such as Intel® LANDesk® Client Manager to use SMBIOS. The BIOS stores and reports the following SMBIOS information:

- BIOS data, such as the BIOS revision level
- Fixed-system data, such as peripherals, serial numbers, and asset tags
- Resource data, such as memory size, cache size, and processor frequency
- Dynamic data, such as event detection and error logging

Non-Plug and Play operating systems, such as Windows NT†, require an additional interface for obtaining the SMBIOS information. The BIOS supports an SMBIOS table interface for such operating systems. Using this support, an SMBIOS service-level application running on a non-Plug and Play operating system can obtain the SMBIOS information.

For information about	Refer to
The D820LP board's compliance level with SMBIOS	Section 1.3, page 16

3.5 BIOS Upgrades

A new version of the BIOS can be upgraded from a diskette using the Intel® Flash Memory Update utility that is available from Intel. This utility supports the following BIOS maintenance functions:

- Update the flash BIOS from a file on a diskette
- Verify that the upgrade BIOS matches the target system to prevent accidentally installing an incompatible BIOS
- BIOS boot block update

BIOS upgrades and the Intel Flash Memory Update utility are available from Intel through the Intel World Wide Web site.

NOTE

Please review the instructions distributed with the upgrade utility before attempting a BIOS upgrade.

For information about	Refer to
The Intel World Wide Web site	Section 1.2, page 16

3.5.1 Language Support

The BIOS program and help messages are supported in five languages: U.S. English, German, Italian, French, and Spanish. The default language is U.S. English unless another language is selected in the BIOS Setup program.

3.5.2 Custom Splash Screen

During POST, an Intel splash screen is displayed by default. This splash screen can be replaced with a custom splash screen. A utility is available from Intel to assist with creating a custom splash screen. The custom splash screen can be programmed into the flash memory using the BIOS upgrade utility. Information about this capability is available on the Intel Support World Wide Web site.

For information about	Refer to
The Intel World Wide Web site	Section 1.2, page 16

3.6 Recovering BIOS Data

Some types of failure can destroy the BIOS. For example, the data can be lost if a power outage occurs while the BIOS is being updated in flash memory. The BIOS can be recovered from a diskette using the BIOS recovery mode. When recovering the BIOS, be aware of the following:

- Because of the small amount of code available in the boot block area, there is no video support. You can only monitor this procedure by listening to the speaker or looking at the diskette drive LED.
- The recovery process may take several minutes; larger BIOS flash memory devices require more time.
- One beep indicates the beginning of the BIOS recovery process.
- Two beeps and the end of activity in the diskette drive indicate successful BIOS recovery.
- A series of continuous beeps indicates a failed BIOS recovery.

To create a BIOS recovery diskette, a bootable diskette must be created and the BIOS update files copied to it. BIOS upgrades and the Intel Flash Memory Update utility are available from Intel Customer Support through the Intel World Wide Web site.

NOTE

When recovering the BIOS using an LS-120 drive, the BIOS recovery diskette must be a standard 1.44 MB diskette not a 120 MB diskette.

For information about	Refer to
The BIOS recovery mode jumper settings	Table 41, page 63
The Boot menu in the BIOS Setup program	Section 4.7, page 101
Contacting Intel customer support	Section 1.2, page 16

3.7 Boot Options

In the BIOS Setup program, the user can choose to boot from a diskette drive, hard drive, CD-ROM, or the network. Table 50 lists the default boot order.

Table 50. Default Boot Order

Boot Order	Boot Device
First	Diskette drive
Second	IDE hard drive
Third	ATAPI CD-ROM
Fourth	Other bootable device detected by the BIOS

3.7.1 CD-ROM and Network Boot

Booting from CD-ROM is supported in compliance to the El Torito bootable CD-ROM format specification. Boot devices are defined in priority order. If the CD-ROM is selected as the boot device, it must be the first device with bootable media.

The network can be selected as a boot device. This selection allows booting from a network add-in board with a remote boot ROM installed.

For information about	Refer to
The El Torito specification	Section 1.3, page 16

3.7.2 Booting Without Attached Devices

For use in embedded applications, the BIOS has been designed so that after passing the POST, the operating system loader is invoked even if the following devices are not present:

- Video adapter (the BIOS will notify the user with one long and two short beeps)
- Keyboard
- Mouse

3.8 USB Legacy Support

USB legacy support enables USB devices such as keyboards, mice, and hubs to be used even when no operating system USB drivers are in place. USB legacy support is used in accessing the BIOS Setup program and installing an operating system that supports USB. By default, USB legacy support is set to Enabled. This setting enables USB legacy support if a supported USB device is connected to the USB port.

This sequence describes how USB legacy support operates in the disabled mode.

1. When you power up the computer, USB legacy support is disabled.
2. POST begins.
3. USB legacy support is temporarily enabled by the BIOS. This allows you to use a USB keyboard to enter the BIOS Setup program or the Maintenance mode.
4. POST completes and disables USB legacy support.
5. The operating system loads. While the operating system is loading, USB keyboards and mice are not recognized. After the operating system loads the USB drivers, the USB devices are recognized by the operating system.

To install an operating system that supports USB, enable USB legacy support in the BIOS Setup program and follow the operating system's installation instructions. Once the operating system is installed and the USB drivers have been configured, USB legacy support is no longer used. USB legacy support can be left enabled in the BIOS Setup program if needed.

Notes on using USB legacy support:

- Do not use USB devices with an operating system that does not support USB. USB legacy is not intended to support the use of USB devices in a non-USB aware operating system.
- USB legacy support is for keyboards, mice, and hubs only. Other USB devices are not supported.

3.9 BIOS Security Features

The BIOS includes security features that restrict access to the BIOS Setup program and who can boot the computer. A supervisor password and a user password can be set for the BIOS Setup program and for booting the computer, with the following restrictions:

- The supervisor password gives unrestricted access to view and change all the Setup options in the BIOS Setup program. This is the supervisor mode.
- The user password gives restricted access to view and change Setup options in the BIOS Setup program. The user's access privileges are determined in the supervisor mode.
- If only the supervisor password is set, pressing the <Enter> key at the password prompt of the BIOS Setup program allows the user restricted access to Setup.
- If both the supervisor and user passwords are set, users can enter either the supervisor password or the user password to access Setup. Users have access to Setup respective to which password is entered. The user's access privileges are determined in the supervisor mode.
- Setting the user password restricts who can boot the computer. The password prompt will be displayed before the computer is booted. If only the supervisor password is set, the computer boots without asking for a password. If both passwords are set, the user can enter either password to boot the computer.

Table 51 shows the effects of setting the supervisor password and user password. This table is for reference only and is not displayed on the screen.

Table 51. Supervisor and User Password Functions

Password Set	Supervisor Mode	User Mode	Setup Options	Password to Enter Setup	Password During Boot
Neither	Can change all options (Note)	Can change all options (Note)	None	None	None
Supervisor only	Can change all options	Can change a limited number of options with the access level determined by supervisor.	Supervisor Password	Supervisor	None
User only	N/A	Can change all options	• Enter Password • Clear User Password	User	User
Supervisor and user set	Can change all options	Can change a limited number of options with the access level determined by supervisor.	• Supervisor Password • Enter Password	Supervisor or user	Supervisor or user

Note: If no password is set, any user can change all Setup options.

For information about	Refer to
Setting user and supervisor passwords	Section 4.5, page 99

4 BIOS Setup Program

What This Chapter Contains

4.1 Introduction

The BIOS Setup program can be used to view and change the BIOS settings for the computer. The BIOS Setup program is accessed by pressing the <F2> key after the Power-On Self-Test (POST) memory test begins and before the operating system boot begins. The menu bar is shown below.

Maintenance	Main	Advanced	Security	Power	Boot	Exit

Table 52 lists the BIOS Setup program menu functions.

Table 52. BIOS Setup Program Menu Bar

Maintenance	Main	Advanced	Security	Power	Boot	Exit
Clears passwords and Boot Integrity Service (Note) credentials, and configures extended configuration settings	Allocates resources for hardware components	Configures advanced features available through the chipset	Sets passwords and security features	Configures power management features	Selects boot options and power supply controls	Saves or discards changes to Setup program options

Note: For information about the Boot Integrity Service, refer to the Intel Web site at:

http://developer.intel.com/design/security/index1.htm

NOTE

In this chapter, all examples of the BIOS Setup Program menu bar include the Maintenance menu; however, the Maintenance menu is displayed only when the board is in configuration mode. Section 2.9 on page 61 tells how to put the board in configuration mode.

Table 53 lists the function keys available for menu screens.

Table 53. BIOS Setup Program Function Keys

BIOS Setup Program Function Key	Description
<←> or <→>	Selects a different menu screen by moving the cursor left or right
<↑> or <↓>	Selects an item by moving the cursor up or down
<Enter>	Executes command or selects the submenu
<F9>	Loads the default configuration values for the current menu
<F10>	Saves the current values and exits the BIOS Setup program
<Esc>	Exits the menu

4.2 Maintenance Menu

Maintenance	Main	Advanced	Security	Power	Boot	Exit

The menu shown in Table 54 is for clearing Setup passwords and enabling extended configuration mode. Setup only displays this menu in configuration mode. See Section 2.9 on page 61 for configuration mode setting information.

Table 54. Maintenance Menu

Feature	Options	Description
Clear All Passwords	No options	Clears the user and supervisor passwords.
Clear BIS (Note) Credentials	No options	Clears the Wired for Management Boot Integrity Service (BIS) credentials.
Extended Configuration	• **Default (default)** • User-Defined	*User Defined* allows system control and video memory cache mode to be set. If *User Defined* is selected, the Advanced Menu will display: "Extended Menu: *Used*."
CPU Information:		
CPU Stepping Signature	No options	Displays the CPU stepping signature.
CPU Microcode Update Revision	No options	Displays the CPU microcode update revision.

Note: For information about the BIS, refer to the Intel Web site at:

http://developer.intel.com/design/security/index1.htm

4.2.1 Extended Configuration Submenu

Maintenance	Main	Advanced	Security	Power	Boot	Exit
Extended Configuration						

The submenu represented by Table 55 is for setting system control and video memory cache mode. This submenu becomes available when User Defined is selected under Extended Configuration.

Table 55. Extended Configuration Submenu

Feature	Options	Description
System Control: Video Memory Cache Mode	• USWC	Selects Uncacheable Speculative Write-Combining (USWC) video memory cache mode. Full 32 byte contents of the Write Combining buffer are written to memory as required. Cache lookups are not performed. Both the video driver and the application must support Write Combining.
	• **UC (default)**	Selects Uncacheable (UC) video memory cache mode. This setting identifies the video memory range as uncacheable by the processor. Memory writes are performed in program order. Cache lookups are not performed. Well suited for applications not supporting Write Combining.

4.3 Main Menu

Maintenance	**Main**	Advanced	Security	Power	Boot	Exit

Table 56 describes the Main Menu. This menu reports processor and memory information and is for configuring the system date and system time.

Table 56. Main Menu

Feature	Options	Description
BIOS Version	No options	Displays the version of the BIOS.
Processor Type	No options	Displays processor type.
Processor Speed	No options	Displays processor operating frequency.
System Bus Frequency	No options	Displays the system bus frequency.
Cache RAM	No options	Displays the size of second-level cache and whether it is ECC-capable.
Total Memory	No options	Displays the total amount of RAM.
Memory Bank 0 Memory Bank 1	No options	Displays type of RIMM installed in each memory bank.
Language	• **English (US) (default)** • Espanol • Deutsche • Italian • Francais	Selects the default language used by the BIOS.
Processor Serial Number	• **Disabled (default)** • Enabled	Enables and disables the processor serial number. (Not supported by all processor speeds.)
Memory Configuration	• **Non-ECC (default)** • ECC	Allows selection of ECC-mode memory operation if ECC memory is installed.
System Time	Hour, minute, and second	Specifies the current time.
System Date	Day of the week, month, day, and year	Specifies the current date.

4.4 Advanced Menu

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

Table 57 describes the Advanced Menu. This menu is used for setting advanced features that are available through the chipset.

Table 57. Advanced Menu

Feature	Options	Description
Extended Configuration	• Used • **Not Used (default)**	If *Used* is highlighted, *User-Defined* has been selected in Extended Configuration under the Maintenance Menu.
PCI Configuration	No options	Configures individual PCI slot's IRQ priority. When selected, displays the PCI Configuration submenu.
Boot Configuration	No options	Configures Plug and Play and the Numlock key, and resets configuration data. When selected, displays the Boot Configuration submenu.
Peripheral Configuration	No options	Configures peripheral ports and devices. When selected, displays the Peripheral Configuration submenu.
IDE Configuration	No options	Specifies type of connected IDE device.
Diskette Configuration	No options	When selected, displays the Floppy Options submenu.
Event Log Configuration	No options	Configures Event Logging. When selected, displays the Event Log Configuration submenu.
Video Configuration	No options	Configures video features. When selected, displays the Video Configuration submenu.

4.4.1 PCI Configuration Submenu

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

The submenu represented by Table 58 is for configuring the IRQ priority of PCI slots individually.

Table 58. PCI Configuration Submenu

Feature	Options (Note)	Description
PCI Slot 1 IRQ Priority	• **Auto (default)** • 9 • 10 • 11	Allows selection of IRQ priority.
PCI Slot 2 IRQ Priority	• **Auto (default)** • 9 • 10 • 11	Allows selection of IRQ priority.
PCI Slot 3 IRQ Priority	• **Auto (default)** • 9 • 10 • 11	Allows selection of IRQ priority. IRQ Priority selections for PCI slots 3 and 5 are linked. Selections made to PCI Slot 3 IRQ Priority are repeated in PCI Slot 5 IRQ Priority.
PCI Slot 4 IRQ Priority	• **Auto (default)** • 9 • 10 • 11	Allows selection of IRQ priority.
PCI Slot 5 IRQ Priority	Whatever is selected in slot 3	No selections can be made to PCI Slot 5 IRQ Priority. Selections made to PCI Slot 3 repeat in PCI Slot 5.

Note: If IRQs 3, 4, 5, and 7 are not used by onboard devices, they will appear here as options also.

4.4.2 Boot Configuration Submenu

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

The submenu represented by Table 59 is for setting Plug and Play options, resetting configuration data, and the power-on state of the Numlock key.

Table 59. Boot Configuration Submenu

Feature	Options	Description
Plug & Play O/S	• **No (default)** • Yes	Specifies if a Plug and Play operating system is being used. *No* lets the BIOS configure all devices. Use this setting for non-Plug and Play operating systems. *Yes* lets the BIOS configure only those devices needed to boot the system.
Reset Config Data	• **No (default)** • Yes	Clears the BIOS configuration data on the next boot.
Numlock	• Off • **On (default)**	Specifies the power-on state of the Numlock feature on the numeric keypad of the keyboard.

4.4.3 Peripheral Configuration Submenu

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

The submenu represented in Table 60 is used for enabling the onboard LAN devices and USB legacy support.

Table 60. Peripheral Configuration Submenu

Feature	Options	Description
Serial Port A	• Disabled • Enabled • **Auto (default)**	Configures serial port A. *Auto* assigns the first free COM port, normally COM1, the address 3F8h, and the interrupt IRQ4. An * (asterisk) displayed next to an address indicates a conflict with another device.
Base I/O address (This feature is displayed only if Serial Port A is set to *Enabled*.)	• **3F8 (default)** • 2F8 • 3E8 • 2E8	Specifies the base I/O address for serial port A, if Serial Port A is set to *Enabled*.
Interrupt (This feature is displayed only if Serial Port A is set to *Enabled*.)	• IRQ 3 • **IRQ 4 (default)**	Specifies the interrupt for serial port A, if Serial Port A is set to *Enabled*.
Serial Port B	• Disabled • Enabled • **Auto (default)**	Configures serial port B. *Auto* assigns the first free COM port, normally COM2, the address 2F8h, and the interrupt IRQ3. An * (asterisk) displayed next to an address indicates a conflict with another device. If either serial port address is set, that address will not appear in the list of options for the other serial port.
Mode	• **Normal (default)** • IrDA SIR-A • ASK_IR	Specifies the mode for serial port B for normal (COM 2) or infrared applications. This option is not available if serial port B has been disabled.

continued

Table 60. Peripheral Configuration Submenu (continued)

Feature	Options	Description
Base I/O address (This feature is displayed only if Serial Port B is set to *Enabled*.)	• **2F8 (default)** • 3E8 • 2E8	Specifies the base I/O address for serial port B.
Interrupt (This feature is displayed only if Serial Port B is set to *Enabled*.)	• **IRQ 3 (default)** • IRQ 4	Specifies the interrupt for serial port B.
Parallel port	• Disabled • Enabled • **Auto (default)**	Configures the parallel port. *Auto* assigns LPT1 the address 378h and the interrupt IRQ7. An * (asterisk) displayed next to an address indicates a conflict with another device.
Mode	• Output Only • **Bi-directional (default)** • EPP • ECP	Selects the mode for the parallel port. Not available if the parallel port is disabled. *Output Only* operates in AT†-compatible mode. *Bi-directional* operates in PS/2-compatible mode. *EPP* is Extended Parallel Port mode, a high-speed bi-directional mode. *ECP* is Enhanced Capabilities Port mode, a high-speed bi-directional mode.
Base I/O address (This feature is displayed only if Parallel Port is set to *Enabled*.)	• **378 (default)** • 278	Specifies the base I/O address for the parallel port.
Interrupt (This feature is displayed only if Parallel Port is set to *Enabled*.)	• IRQ 5 • **IRQ 7(default)**	Specifies the interrupt for the parallel port.
Legacy USB Support	• Disabled • **Enabled (default)**	Enables or disables USB legacy support. (See Section 3.8 on page 82 for more information.)

4.4.4 IDE Configuration Submenu

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

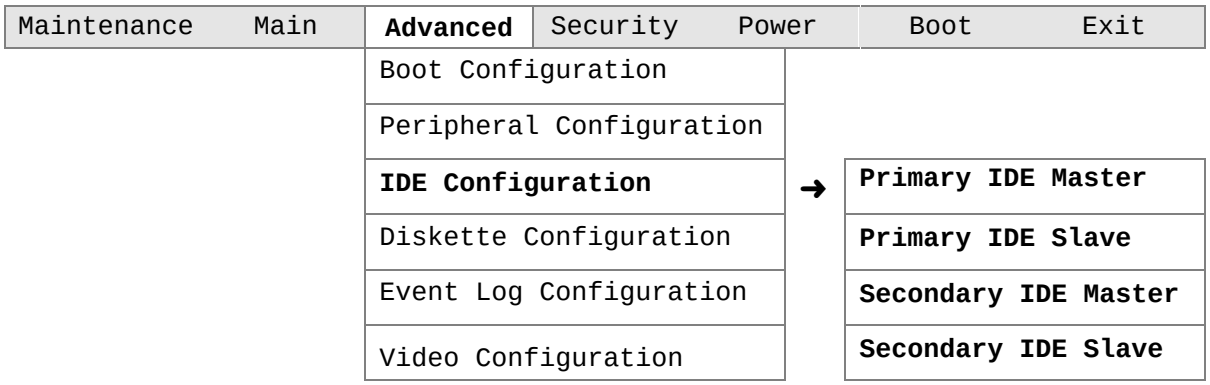
PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

The submenu represented in Table 61 is used to configure IDE device options.

Table 61. IDE Configuration Submenu

Feature	Options	Description
IDE Controller	• Disabled • Primary • Secondary • **Both (default)**	Specifies the integrated IDE controller. *Primary* enables only the primary IDE controller. *Secondary* enables only the secondary IDE controller. *Both* enables both IDE controllers.
Hard Disk Pre-Delay	• **Disabled (default)** • 3 Seconds • 6 Seconds • 9 Seconds • 12 Seconds • 15 Seconds • 21 Seconds • 30 Seconds	Specifies the hard disk drive pre-delay.
Primary IDE Master	No options	Reports type of connected IDE device. When selected, displays the Primary IDE Master submenu.
Primary IDE Slave	No options	Reports type of connected IDE device. When selected, displays the Primary IDE Slave submenu.
Secondary IDE Master	No options	Reports type of connected IDE device. When selected, displays the Secondary IDE Master submenu.
Secondary IDE Slave	No options	Reports type of connected IDE device. When selected, displays the Secondary IDE Slave submenu.

4.4.4.1 IDE Configuration Sub-Submenus



The submenus represented in Table 62 are used to configure IDE devices.

Table 62. IDE Configuration Sub-Submenus

Feature	Options	Description
Type	• None • User • **Auto (default)** • CD-ROM • ATAPI Removable • Other ATAPI • IDE Removable	Specifies the IDE configuration mode for IDE devices. *User* allows the LBA Mode Control, Multi-sector Transfers, PIO Mode, and Ultra DMA features to be changed. *Auto* automatically selects the values for the LBA Mode Control, Multi-sector Transfers, PIO Mode, and Ultra DMA features.
LBA Mode Control (Note)	• Disabled • **Enabled (default)**	Enables or disables LBA Mode Control.
Multi-sector Transfers (Note)	• Disabled • 2 Sectors • 4 Sectors • 8 Sectors • **16 Sectors (default)**	Specifies number of sectors per block for transfers from the hard disk drive to memory. Check the hard disk drive's specifications for optimum setting.
PIO Mode (Note)	• **Auto (default)** • 0 • 1 • 2 • 3 • 4	Specifies the transfer mode.
Ultra DMA (Note)	• **Disabled (default)** • Mode 0 • Mode 1 • Mode 2 • Mode 3 • Mode 4	Specifies the Ultra DMA mode for the drive. Note that when *Auto* is selected in PIO Mode, the BIOS sets Ultra DMA to the fastest speed supported. If the drive doesn't support Ultra DMA, the BIOS sets Ultra DMA to *Disabled* and the fastest supported PIO mode is used instead.

Note: The setting of *Type* determines whether these features display.

4.4.5 Diskette Configuration Submenu

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

The submenu represented by Table 63 is used for configuring the diskette drive.

Table 63. Diskette Configuration Submenu

Feature	Options	Description
Diskette Controller	• Disabled • **Enabled (default)**	Disables or enables the integrated diskette controller.
Floppy A	• Not Installed • 360 KB 5¼ inches • 1.2 MB 5¼ inches • 720 KB 3½ inches • **1.44/1.25 MB 3½ inches (default)** • 2.88 MB 3½ inches	Specifies the capacity and physical size of diskette drive A.
Diskette Write Protect	• **Disabled (default)** • Enabled	Disables or enables write-protect for the diskette drive.

4.4.6 Event Log Configuration Submenu

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

The submenu represented by Table 64 is used to configure the event logging features.

Table 64. Event Log Configuration Submenu

Feature	Options	Description
Event Log	No options	Indicates if there is space available in the event log.
Event Log Validity	No options	Indicates if the contents of the event log are valid.
View Event Log	[Enter]	Displays the event log.
Clear All Event Logs	• **No (default)** • Yes	Clears the event log after rebooting.
Event Logging	• Disabled • **Enabled (default)**	Enables logging of events.
ECC Event Logging	• Disabled • **Enabled (default)**	Enables logging of ECC events.
Mark Events as Read	[Enter]	Marks all events as read.

4.4.7 Video Configuration Submenu

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

The submenu represented in Table 65 is for configuring the video features.

Table 65. Video Configuration Submenu

Feature	Options	Description
AGP Aperture Size	• **64 MB (default)** • 256 MB	Specifies the aperture size for the AGP video controller.
Primary Video Adapter	• **AGP (default)** • PCI	Selects primary video adapter to be used during boot.

4.5 Security Menu

Maintenance	Main	Advanced	**Security**	Power	Boot	Exit

The menu represented by Table 66 is for setting passwords and security features.

Table 66. Security Menu

If no password is set these features appear:		
Feature	**Options**	**Description**
Supervisor Password Is	No options	Reports if there is a supervisor password set.
User Password Is	No options	Reports if there is a user password set.
Set Supervisor Password	Password can be up to seven alphanumeric characters.	Specifies the supervisor password.
Set User Password	Password can be up to seven alphanumeric characters.	Specifies the user password.
Clear User Password (Note 1)	• Yes • No	Allows removal of a previously entered password.
User Access Level (Note 2)	• Limited • No access • View Only • **Full (default)**	Specifies the amount of user access to the Setup program. *Limited* allows only limited fields to be changed. *No Access* prevents user access. *View Only* allows the user to view but not change the fields in the Setup program. *Full* allows any field to be changed except the supervisor password.
Unattended Start (Note 1)	• Enabled • **Disabled (default)**	When enabled, the computer boots, but the keyboard is locked. The user must enter a password to unlock the computer or boot from a diskette.

Notes:

1. This feature appears only if a user password has been set.
2. This feature appears only if a supervisor password has been set.

4.6 Power Menu

Maintenance	Main	Advanced	Security	**Power**	Boot	Exit

The menu represented in Table 67 is for setting the power management features.

Table 67. Power Menu

Feature	Options	Description
Power Management	• Disabled • **Enabled (default)**	Enables or disables the BIOS power management feature.
Inactivity Timer	• Off • 1 Minute • 5 Minutes • 10 Minutes • **20 Minutes (default)** • 30 Minutes • 60 Minutes • 120 Minutes	Specifies the amount of time before the computer enters standby mode.
Hard Drive	• Disabled • **Enabled (default)**	Enables power management for hard disks during standby modes.
Video Power-Down	• Disabled • Standby • **Suspend (default)** • Sleep	Specifies power management for video during standby modes.
ACPI Suspend State	• **S1 State (default)** • S3 State	Specifies the ACPI suspend state.

NOTE

When an ACPI-capable operating system is configured for ACPI, only the ACPI Suspend State option affects power management. The ACPI Suspend State is not supported if the system is configured for APM.

4.7 Boot Menu

Maintenance	Main	Advanced	Security	Power	**Boot**	Exit

The menu represented in Table 68 is used to set the boot features and the boot sequence.

Table 68. Boot Menu

Feature	Options	Description
Quiet Boot	• Disabled • **Enabled (default)**	*Disabled* displays normal POST messages. *Enabled* displays OEM graphic instead of POST messages.
Quick Boot	• Disabled • **Enabled (default)**	Enables the computer to boot without running certain POST tests.
Scan User Flash Area	• **Disabled (default)** • Enabled	Enables the BIOS to scan the flash memory for user binary files that are executed at boot time.
After Power Failure	• Stays Off • **Last State (default)** • Power On	*Stays Off* keeps the power off until the power button is pressed. *Last State* restores the previous power state before power loss occurred. Specifies the mode of operation if an AC/Power loss occurs. *Power On* restores power to the computer.
On Modem Ring	• **Stay Off (default)** • Power On	Specifies how the computer responds to an incoming call on an installed modem when the power is off. This soft-off mode applies to Wake on Ring technology. This feature applies only to systems configured in APM mode.
1st Boot Device 2nd Boot Device 3rd Boot Device 4th Boot Device (This list varies in length with the number of devices attached up to 8.)	• Floppy • ARMD-FDD (Note 1) • ARMD-HDD (Note 2) • IDE-HDD (Note 3) • ATAPI CD-ROM • Disabled • (Note 4)	Specifies the boot sequence from the available devices. To specify boot sequence: 1. Select the boot device with <↑> or <↓>. 2. Press <Enter> to set the selection as the intended boot device. The operating system assigns a drive letter to each boot device in the order listed. Changing the order of the devices changes the drive lettering. Not all of the devices in this list are available as second, third, and fourth boot devices. The default settings for the first through fourth boot devices are, respectively: • Floppy • 1st IDE-HDD (set in the next feature entitled IDE Drive Configuration) • ATAPI CD-ROM • Other bootable device detected by the BIOS
IDE Drive Configuration	[Enter]	Configures IDE drives. When selected, displays the IDE Drive Configuration submenu.

Notes:

1. ARMD-FDD = ATAPI removable device - floppy disk drive
2. ARMD-HDD = ATAPI removable device - hard disk drive
3. HDD = Hard disk drive
4. Other bootable devices detected by the BIOS, such as LAN and SCSI add-in boards, will appear in this list.

4.7.1 IDE Drive Configuration Submenu

Maintenance	Main	Advanced	Security	Power	**Boot**	Exit
					IDE Drive Configuration	

The submenu represented in Table 69 is used to select the IDE drive to boot from.

Table 69. IDE Drive Configuration Submenu

Feature	Options	Description
Primary Master IDE Primary Slave IDE Secondary Master IDE Secondary Slave IDE	• **1st IDE (default)** • 2nd IDE • 3rd IDE • 4th IDE	*1st IDE* specifies the IDE hard disk drive to boot from. To specify the drive to boot from: 1. Use <↑> or <↓> to select the channel, and master or slave mode of the drive to boot from. 2. Use <↑> or <↓> to select 1st IDE. Press <Enter> to set the selection.

4.8 Exit Menu

Maintenance	Main	Advanced	Security	Power	Boot	**Exit**

The menu represented in Table 70 is for exiting the BIOS Setup program, saving changes, and loading and saving defaults.

Table 70. Exit Menu

Feature	Description
Exit Saving Changes	Exits and saves the changes in CMOS SRAM.
Exit Discarding Changes	Exits without saving any changes made in the BIOS Setup program.
Load Setup Defaults	Loads the factory default values for all the Setup options.
Load Custom Defaults	Loads the custom defaults for Setup options.
Save Custom Defaults	Saves the current values as custom defaults. Normally, the BIOS reads the Setup values from flash memory. If this memory is corrupted, the BIOS reads the custom defaults. If no custom defaults are set, the BIOS reads the factory defaults.
Discard Changes	Discards changes without exiting Setup. The option values present when the computer was turned on are used.

5 Error Messages and Beep Codes

What This Chapter Contains

5.1 BIOS Error Messages

Table 71 lists the error messages and provides a brief description of each.

Table 71. BIOS Error Messages

Error Message	Explanation
GA20 Error	An error occurred with Gate A20 when switching to protected mode during the memory test.
Pri Master HDD Error Pri Slave HDD Error Sec Master HDD Error Sec Slave HDD Error	Could not read sector from corresponding drive.
Pri Master Drive - ATAPI Incompatible Pri Slave Drive - ATAPI Incompatible Sec Master Drive - ATAPI Incompatible Sec Slave Drive - ATAPI Incompatible	Corresponding drive in not an ATAPI device. Run Setup to make sure device is selected correctly.
A: Drive Error	No response from diskette drive.
Cache Memory Bad	An error occurred when testing L2 cache. Cache memory may be bad.
CMOS Battery Low	The battery may be losing power. Replace the battery soon.
CMOS Display Type Wrong	The display type is different than what has been stored in CMOS. Check Setup to make sure type is correct.
CMOS Checksum Bad	The CMOS checksum is incorrect. CMOS memory may have been corrupted. Run Setup to reset values.
CMOS Settings Wrong	CMOS values are not the same as the last boot. These values have either been corrupted or the battery has failed.
CMOS Date/Time Not Set	The time and/or date values stored in CMOS are invalid. Run Setup to set correct values.
DMA Error	Error during read/write test of DMA controller.
FDC Failure	Error occurred trying to access diskette drive controller.
HDC Failure	Error occurred trying to access hard disk controller.

continued

Table 71. BIOS Error Messages (continued)

Error Message	Explanation
Checking NVRAM.....	NVRAM is being checked to see if it is valid.
Update OK!	NVRAM was invalid and has been updated.
Updated Failed	NVRAM was invalid but was unable to be updated.
Keyboard Is Locked	The system keyboard lock is engaged. The system must be unlocked to continue to boot.
Keyboard Error	Error in the keyboard connection. Make sure keyboard is connected properly.
KB/Interface Error	Keyboard interface test failed.
Memory Size Decreased	Memory size has decreased since the last boot. If no memory was removed then memory may be bad.
Memory Size Increased	Memory size has increased since the last boot. If no memory was added there may be a problem with the system.
Memory Size Changed	Memory size has changed since the last boot. If no memory was added or removed then memory may be bad.
No Boot Device Available	System did not find a device to boot.
Off Board Parity Error	A parity error occurred on an off-board card. This error is followed by an address.
On Board Parity Error	A parity error occurred in onboard memory. This error is followed by an address.
Parity Error	A parity error occurred in onboard memory at an unknown address.
<CTRL_N> Pressed	CMOS is ignored and NVRAM is cleared. User must enter Setup.

5.2 Port 80h POST Codes

During the POST the BIOS generates diagnostic progress codes (POST-codes) to I/O port 80h. If the POST fails, execution stops and the last POST code generated is left at port 80h. This code is useful for determining the point where an error occurred.

Displaying the POST-codes requires an add-in board (often called a POST card). The POST card can decode the port and display the contents on a medium such as a seven-segment display.

The tables below offer descriptions of the POST codes generated by the BIOS. Table 72 defines the Uncompressed INIT Code Checkpoints, Table 73 describes the Boot Block Recovery Code Checkpoints, and Table 74 lists the Runtime Code Uncompressed in F000 Shadow RAM. Some codes are repeated in the tables because that code applies to more than one operation.

Table 72. Uncompressed INIT Code Checkpoints

Code	Description of POST Operation
D0	NMI is Disabled. Onboard KBC, RTC enabled (if present). Init code Checksum verification starting.
D1	Keyboard controller BAT test, CPU ID saved, and going to 4 GB flat mode.
D3	Perform necessary chipset initialization, start memory refresh, perform Memory sizing.
D4	Verify base memory.
D5	Init code to be copied to segment 0 and control to be transferred to segment 0.
D6	Control is in segment 0. To check recovery mode and verify main BIOS checksum. If either it is recovery mode or main BIOS checksum is bad, go to check point E0 for recovery else go to check point D7 for giving control to main BIOS.
D7	Find Main BIOS module in ROM image.
D8	Uncompress the main BIOS module.
D9	Copy main BIOS image to F000 shadow RAM and give control to main BIOS in F000 shadow RAM.

Table 73. Boot Block Recovery Code Checkpoints

Code	Description of POST Operation
E0	Onboard Floppy Controller (if any) is initialized. Compressed recovery code is uncompressed in F000:0000 in Shadow RAM and give control to recovery code in F000 Shadow RAM. Initialize interrupt vector tables, initialize system timer, initialize DMA controller and interrupt controller.
E8	Initialize extra (Intel Recovery) Module.
E9	Initialize floppy drive.
EA	Try to boot from floppy. If reading of boot sector is successful, give control to boot sector code.
EB	Booting from floppy failed, look for ATAPI (LS-120, Zip) devices.
EC	Try to boot from ATAPI. If reading of boot sector is successful, give control to boot sector code.
EF	Booting from floppy and ATAPI device failed. Give two beeps. Retry the booting procedure again (go to check point E9).

Table 74. Runtime Code Uncompressed in F000 Shadow RAM

Code	Description of POST Operation
03	NMI is disabled. To check soft reset/power-on.
05	BIOS stack set. Going to disable cache if any.
06	POST code to be uncompressed.
07	CPU init and CPU data area init to be done.
08	CMOS checksum calculation to be done next.
0B	Any initialization before keyboard BAT to be done next.
0C	KB controller I/B free. To issue the BAT command to keyboard controller.
0E	Any initialization after KB controller BAT to be done next.
0F	Keyboard command byte to be written.
10	Going to issue Pin 23,24 blocking/unblocking command.
11	Going to check pressing of <INS>, <END> key during power-on.
12	To init CMOS if "Init CMOS in every boot" is set or <END> key is pressed. Going to disable DMA and Interrupt controllers.
13	Video display is disabled and port B is initialized. Chipset init about to begin.
14	8254 timer test about to start.
19	About to start memory refresh test.
1A	Memory Refresh line is toggling. Going to check 15 µs ON/OFF time.
23	To read 8042 input port and disable Megakey GreenPC feature. Make BIOS code segment writeable.
24	To do any setup before Int vector init.
25	Interrupt vector initialization to begin. To clear password if necessary.
27	Any initialization before setting video mode to be done.
28	Going for monochrome mode and color mode setting.
2A	Different buses init (system, static, and output devices) to start if present. (See Section 5.3 for details of different buses.)
2B	To give control for any setup required before optional video ROM check.
2C	To look for optional video ROM and give control.
2D	To give control to do any processing after video ROM returns control.
2E	If EGA/VGA not found then do display memory R/W test.
2F	EGA/VGA not found. Display memory R/W test about to begin.
30	Display memory R/W test passed. About to look for the retrace checking.
31	Display memory R/W test or retrace checking failed. To do alternate Display memory R/W test.
32	Alternate Display memory R/W test passed. To look for the alternate display retrace checking.
34	Video display checking over. Display mode to be set next.
37	Display mode set. Going to display the power-on message.
38	Different buses init (input, IPL, general devices) to start if present. (See Section 5.3 for details of different buses.)
39	Display different buses initialization error messages. (See Section 5.3 for details of different buses.)
3A	New cursor position read and saved. To display the Hit <DEL> message.

continued

Table 74. Runtime Code Uncompressed in F000 Shadow RAM (continued)

Code	Description of POST Operation
40	To prepare the descriptor tables.
42	To enter in virtual mode for memory test.
43	To enable interrupts for diagnostics mode.
44	To initialize data to check memory wrap around at 0:0.
45	Data initialized. Going to check for memory wrap around at 0:0 and finding the total system memory size.
46	Memory wrap around test done. Memory size calculation over. About to go for writing patterns to test memory.
47	Pattern to be tested written in extended memory. Going to write patterns in base 640k memory.
48	Patterns written in base memory. Going to find out amount of memory below 1M memory.
49	Amount of memory below 1M found and verified. Going to find out amount of memory above 1M memory.
4B	Amount of memory above 1M found and verified. Check for soft reset and going to clear memory below 1M for soft reset. (If power on, go to check point # 4Eh).
4C	Memory below 1M cleared. (SOFT RESET) Going to clear memory above 1M.
4D	Memory above 1M cleared. (SOFT RESET) Going to save the memory size. (Go to check point # 52h).
4E	Memory test started. (NOT SOFT RESET) About to display the first 64k memory size.
4F	Memory size display started. This will be updated during memory test. Going for sequential and random memory test.
50	Memory testing/initialization below 1M complete. Going to adjust displayed memory size for relocation/ shadow.
51	Memory size display adjusted due to relocation/ shadow. Memory test above 1M to follow.
52	Memory testing/initialization above 1M complete. Going to save memory size information.
53	Memory size information is saved. CPU registers are saved. Going to enter in real mode.
54	Shutdown successful, CPU in real mode. Going to disable gate A20 line and disable parity/NMI.
57	A20 address line, parity/NMI disable successful. Going to adjust memory size depending on relocation/shadow.
58	Memory size adjusted for relocation/shadow. Going to clear Hit <DEL> message.
59	Hit <DEL> message cleared. <WAIT...> message displayed. About to start DMA and interrupt controller test.
60	DMA page register test passed. To do DMA#1 base register test.
62	DMA#1 base register test passed. To do DMA#2 base register test.
65	DMA#2 base register test passed. To program DMA unit 1 and 2.
66	DMA unit 1 and 2 programming over. To initialize 8259 interrupt controller.
7F	Extended NMI sources enabling is in progress.
80	Keyboard test started. Clearing output buffer, checking for stuck key, to issue keyboard reset command.
81	Keyboard reset error/stuck key found. To issue keyboard controller interface test command.
82	Keyboard controller interface test over. To write command byte and init circular buffer.
83	Command byte written, global data init done. To check for lock-key.

continued

Table 74. Runtime Code Uncompressed in F000 Shadow RAM (continued)

Code	Description of POST Operation
84	Lock-key checking over. To check for memory size mismatch with CMOS.
85	Memory size check done. To display soft error and check for password or bypass setup.
86	Password checked. About to do programming before setup.
87	Programming before setup complete. To uncompress SETUP code and execute CMOS setup.
88	Returned from CMOS setup program and screen is cleared. About to do programming after setup.
89	Programming after setup complete. Going to display power-on screen message.
8B	First screen message displayed. <WAIT...> message displayed. PS/2 Mouse check and extended BIOS data area allocation to be done.
8C	Setup options programming after CMOS setup about to start.
8D	Going for hard disk controller reset.
8F	Hard disk controller reset done. Floppy setup to be done next.
91	Floppy setup complete. Hard disk setup to be done next.
95	Init of different buses optional ROMs from C800 to start. (See Section 5.3 for details of different buses.)
96	Going to do any init before C800 optional ROM control.
97	Any init before C800 optional ROM control is over. Optional ROM check and control will be done next.
98	Optional ROM control is done. About to give control to do any required processing after optional ROM returns control and enable external cache.
99	Any initialization required after optional ROM test over. Going to setup timer data area and printer base address.
9A	Return after setting timer and printer base address. Going to set the RS-232 base address.
9B	Returned after RS-232 base address. Going to do any initialization before Coprocessor test.
9C	Required initialization before Coprocessor is over. Going to initialize the Coprocessor next.
9D	Coprocessor initialized. Going to do any initialization after Coprocessor test.
9E	Initialization after Coprocessor test is complete. Going to check extended keyboard, keyboard ID and Numlock.
A2	Going to display any soft errors.
A3	Soft error display complete. Going to set keyboard typematic rate.
A4	Keyboard typematic rate set. To program memory wait states.
A5	Going to enable parity/NMI.
A7	NMI and parity enabled. Going to do any initialization required before giving control to optional ROM at E000.
A8	Initialization before E000 ROM control over. E000 ROM to get control next.
A9	Returned from E000 ROM control. Going to do any initialization required after E000 optional ROM control.
AA	Initialization after E000 optional ROM control is over. Going to display the system configuration.
AB	Put INT13 module runtime image to shadow.
AC	Generate MP for multiprocessor support (if present).
AD	Put CGA INT10 module (if present) in Shadow.

continued

Table 74. Runtime Code Uncompressed in F000 Shadow RAM (continued)

Code	Description of POST Operation
AE	Uncompress SMBIOS module and init SMBIOS code and form the runtime SMBIOS image in shadow.
B1	Going to copy any code to specific area.
00	Copying of code to specific area done. Going to give control to INT-19 boot loader.

5.3 Bus Initialization Checkpoints

The system BIOS gives control to the different buses at several checkpoints to do various tasks. Table 75 describes the bus initialization checkpoints.

Table 75. Bus Initialization Checkpoints

Checkpoint	Description
2A	Different buses init (system, static, and output devices) to start if present.
38	Different buses init (input, IPL, and general devices) to start if present.
39	Display different buses initialization error messages.
95	Init of different buses optional ROMs from C800 to start.

While control is inside the different bus routines, additional checkpoints are output to port 80h as WORD to identify the routines under execution. In these WORD checkpoints, the low byte of the checkpoint is the system BIOS checkpoint from which the control is passed to the different bus routines. The high byte of the checkpoint is the indication of which routine is being executed in the different buses. Table 76 describes the upper nibble of the high byte and indicates the function that is being executed.

Table 76. Upper Nibble High Byte Functions

Value	Description
0	func#0, disable all devices on the bus concerned.
1	func#1, static devices init on the bus concerned.
2	func#2, output device init on the bus concerned.
3	func#3, input device init on the bus concerned.
4	func#4, IPL device init on the bus concerned.
5	func#5, general device init on the bus concerned.
6	func#6, error reporting for the bus concerned.
7	func#7, add-on ROM init for all buses.

Table 77 describes the lower nibble of the high byte and indicates the bus on which the routines are being executed.

Table 77. Lower Nibble High Byte Functions

Value	Description
0	Generic DIM (Device Initialization Manager)
1	On-board System devices
2	ISA devices
3	EISA devices
4	ISA PnP devices
5	PCI devices

5.4 Speaker

A 47 Ω inductive speaker is mounted on the D820LP board. The speaker provides audible error code (beep code) information during POST.

For information about	Refer to
The location of the onboard speaker	Figure 1, page 14

5.5 BIOS Beep Codes

Whenever a recoverable error occurs during POST, the BIOS displays an error message describing the problem (see Table 78). The BIOS also issues a beep code (one long tone followed by two short tones) during POST if the video configuration fails (a faulty video board or no board installed) or if an external ROM module does not properly checksum to zero.

An external ROM module (for example, a video BIOS) can also issue audible errors, usually consisting of one long tone followed by a series of short tones. For more information on the beep codes issued, check the documentation for that external device.

There are several POST routines that issue a POST terminal error and shut down the system if they fail. Before shutting down the system, the terminal error handler issues a beep code signifying the test point error, writes the error to I/O port 80h, attempts to initialize the video and writes the error in the upper left corner of the screen (using both monochrome and color adapters).

If POST completes normally, the BIOS issues one short beep before passing control to the operating system.

Table 78. Beep Codes

Beep	Description
1	Refresh failure
2	Parity cannot be reset
3	Memory failure
4	Timer not operational
5	Not used
6	8042 GateA20 cannot be toggled
7	Exception interrupt error
8	Display memory R/W error
9	Not used
10	CMOS Shutdown register test error
11	Invalid BIOS (e.g. POST module not found, etc.)

5.6 Enhanced Diagnostics

The enhanced diagnostics feature consists of a hardware decoder and four LEDs located next to the serial port B connector. This feature requires no modifications to the chassis (other than I/O back panel shield) or cabling.

Figure 15 shows the location of the diagnostic LEDs. Table 79 lists the diagnostic codes displayed by the LEDs.

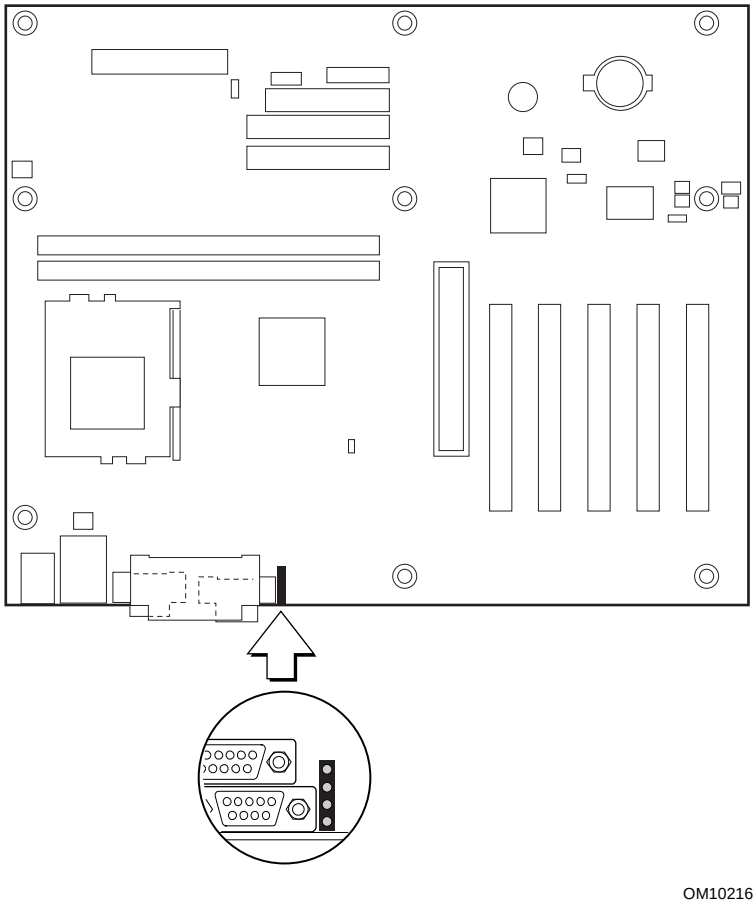
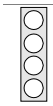
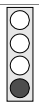
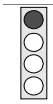
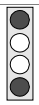
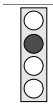
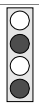
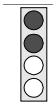
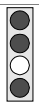
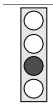
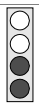
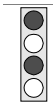
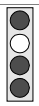
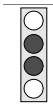
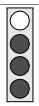
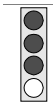
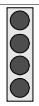


Figure 15. Enhanced Diagnostic LEDs

Table 79. Diagnostic LED Codes

Display		BIOS Operation	Display		BIOS Operation
	Amber Amber Amber Amber	Power on, starting BIOS		Amber Amber Amber Green	Reserved
	Green Amber Amber Amber	Recovery mode		Green Amber Amber Green	Reserved
	Amber Green Amber Amber	Processor, cache, etc.		Amber Green Amber Green	Reserved
	Green Green Amber Amber	Memory, auto-size, shadow, etc.		Green Green Amber Green	Reserved
	Amber Amber Green Amber	PCI bus initialization		Amber Amber Green Green	Reserved
	Green Amber Green Amber	Video		Green Amber Green Green	Reserved
	Amber Green Green Amber	IDE bus initialization		Amber Green Green Green	Reserved
	Green Green Green Amber	USB initialization		Green Green Green Green	Booting operating system