Classic E Expandable Desktop

Jumper Settings / Connectors

(* denotes default setting)

FLASH BOOT BLOCK (J3)

1-2 Boot from Boot Block (recovery mode) 2-3* Boot from standard BIOS

SUPER I/O PC87311AVF (J4)

1-2* Enable 2-3 Disable

CPU SPEED SELECT (J5, J6)

	J5	*J6*
16 MHz	1-2	1-2
20 MHz	2-3	1-2
25 MHz	1-2	2-3
33 MHz	2-3	2-3

CPU Speed Select Jumper Settings.

PASSWORD JUMPER (J7)

1-2 Clear Password 2-3* Enable Password function

PARALLEL PORT DIRECTION VIA HARDWARE (J9)

1-2* Parallel port is output 2-3 Parallel port is input

PARALLEL PORT DIRECTION HARDWARE/SOFTWARE (J11)

1-2 Software select for redirection 2-3* Hardware select for redirection

BATTERY TYPE SELECT (J17)

1-2 6 volt 2-3* 3.6 volt or 4.5 volt

FAN POWER (J29)

1-2 No connect 2-3 Connect secondary 12V DC fan*

FLASH WRITE (J30)

1-2* Enable +12V to FLASH (erasable) 2-3 Disable +12V to FLASH

LOCAL BUS READY MODE (J31)

1-2* Delayed Local Bus Ready 2-3 Direct Local Bus Ready

UPGRADE SOCKET CPU TYPE (J32, J33)

Upgrade Socket (U58) CPU Type	*J32*		*J33*	
i486DX	1-2	5-6	3-5	4-6
i487SX	1-2	5-6	1-3	2-4
i486DX2	1-2	5-6	3-5	4-6
OverDrive processor (ODP)	1-2	5-6	1-3	2-4
i486SX	3-4		4-6	
None	Don't Care		1-3	2-4

Upgrade Socket CPU Type Jumper Settings.

CACHE SIZE (J34)

Cache Size	*Jumpers*			*SRAM Required*
0 KB	Don't Care			None
64 KB	Out			8K x 8 (both banks)
128 KB	1-2	5-6		32K x 8 (bank 0)
256 KB	1-2	3-4	7-8	32K x 8 (both banks)

Cache Size Jumper Selections.

CMOS CLEAR (J25)

1	3	5	7	9	11	13	15	17*
2	4	6	8	10	12	14	16	18*

No jumper Clear CMOS on boot-up

17-18* Use saved CMOS settings on boot-up

* Note: The CMOS clear jumper shares the same connector header with the speaker, reset, hard drive LED and power LED circuitry. The J25:17-18 connection is located on the side closest to the cache SRAM sockets.

Connectors

SERIAL PORTS COM1 & COM2 (J16 & J18)

J16 & J18	*DB9 Pin*	*Name*	*Description*
1	**1**	DCD	Data Carrier Detected
3	**2**	RXD	Receive Data
5	**3**	TXD	Transmit Data
7	**4**	DTR	Data Terminal Ready
9	**5**	GND	Ground
2	**6**	DSR	Data Set Ready
4	**7**	RTS	Request to Send
6	**8**	CTS	Clear to Send
8	**9**	RIA	Ring Indication Active

Serial Ports Pin-Out

PARALLEL PORT (J19)

J19 Pin	*DB25 Pin*	*Name*	*J19 Pin*	*DB25 Pin*	*Name*
1	**1**	STROBE*	**2**	**14**	AUTOFD*
3	**2**	D0	**4**	**15**	ERROR*
5	**3**	D1	**6**	**16**	INIT*
7	**4**	D2	**8**	**17**	SLCTIN*
9	**5**	D3	**10**	**18**	GND
11	**6**	D4	**12**	**19**	GND
13	**7**	D5	**14**	**20**	GND
15	**8**	D6	**16**	**21**	GND
17	**9**	D7	**18**	**22**	GND
19	**10**	ACK*	**20**	**23**	GND
21	**11**	BUSY	**22**	**24**	GND
23	**12**	PE	**24**	**25**	GND
25	**13**	SLCT			

Parallel Port Connector Pin-Out

FLOPPY CONNECTOR (J13)

Pin	*Name*	*Function*
1	(NC)	Docking drive only, usually GND
2	HD_In	High Density In
3	(NC)	Docking drive only, usually GND
4	(NC)	Docking drive only, usually GND
5	(Keyed)	
6	ED_In	Extended Density In
7	+5V	Docking drive only, usually GND
8	INDEX*	L = Beginning of track
9	+5V	Docking drive only, usually GND
10	MOTENA*	Motor A select
11	+5V	Docking drive only, usually GND
12	DRVSELB*	Drive B select
13	GND	
14	DRVSELA*	Drive A Select
15	GND	
16	MOTENB*	Motor B Select
17	GND	

Pin	*Name*	*Function*
18	DIR*	Head Move to Center
19	GND	
20	STEP*	Step (Supplies step pulses)
21	GND	
22	WRDATA*	Write Data
23	GND	
24	FLPYWE*	Enable Head to Write
25	GND	
26	TRACK0*	Indicates Head on Track 0
27	GND	
28	WP*	Write Protected
29	ED_Out	Extended Density Out
30	RDDATA*	Read Data
31	GND	
32	HDSEL*	Head Select side 1
33	HD_Out	High Density Out
34	DSKCHNG*	Disk Changed

IDE CONNECTOR (J14)

1	IDERST	Reset signal from CPU
2	GND	Ground
3	ID7	Data bit 7
4	ID8	Data bit 8
5	ID6	Data bit 6
6	ID9	Data bit 9
7	ID5	Data bit 5
8	ID10	Data bit 10
9	ID4	Data bit 4
10	ID11	Data bit 11
11	ID3	Data bit 3
12	ID12	Data bit 12
13	ID2	Data bit 2
14	ID13	Data bit 13
15	ID1	Data bit 1
16	ID14	Data bit 14
17	ID0	Data bit 0
18	ID15	Data bit 15
19	GND	Ground
20	KEY	No connection

21	IDEDRQ - CHRDY	I/O Channel Ready
22	GND	Ground
23	IDEIOW*	I/O write
24	GND	Ground
25	IDEIOR*	I/O read
26	GND	Ground
27	CHRDY	I/O channel ready
28	IDEBALE	Address latch enable
29	IDEDAK*	
30	GND	Ground
31	IDEIRQ14	IRQ 14
32	CS16	
33	IDESA1	Address bit 1
34	PDIAG*	
35	IDESA0	Address bit 0
36	IDESA2	Address bit 2
37	IDECS0*	Chip select 0
38	IDECS1*	Chip select 1
39	IDEHDACT*/ DR1PRES*	Disk activity light
40	GND	Ground

POWER CONNECTOR

J1

Pin	*Name*	*Function*
1	PWRGD	Power Good
2	+5 V	+ 5 volts
3	+12 V	+ 12 volts
4	-12 V	- 12 volts
5	GND	Ground
6	GND	Ground

Power Connector Pin-Out J1

J2

Pin	*Name*	*Function*
1	GND	Ground
2	GND	Ground
3	-5 V	- 5 volts
4	+5 V	+ 5 volts
5	+5 V	+ 5 volts
6	+5 V	+ 5 volts

Power Connector Pin-Out J2

TITLE:	Classic E Expandable Desktop Jumper Settings / Connectors
INTEL REF:	E_TPS4F.doc
PRODUCT:	Classic E Expandable Desktop
DATE/VER:	4/1/93, Ver. 1.0
RELATED:	Board Level Features, System Level Features, User-Installable Upgrades, Memory Map/Interrupts/Specs
KEYWORDS:	Jumpers, Connectors