BI440ZX Motherboard
Technical Product Specification

November 1998

Order Number 726089-001

The BI440ZX motherboard may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in the BI440ZX Motherboard Specification Update.

Revision History

Revision	Revision History	Date
001	First Release of the BI440ZX Motherboard Technical Product Specification	November 1998

This product specification applies only to standard BI440ZX motherboards with BIOS identifier 4B4IZ0XA.86A.

Changes to this specification will be published in the BI440ZX Motherboard Specification Update before being incorporated into a revision of this document.

Preface

This Technical Product Specification (TPS) specifies the board layout, components, connectors, power and environmental requirements, and the BIOS for the BI440ZX motherboard. It describes the standard motherboard product and available manufacturing options.

Intended Audience

The TPS is intended to provide detailed, technical information about the motherboard and its components to the vendors, system integrators, and other engineers and technicians who need this level of information. It is specifically *not* intended for general audiences.

What This Document Contains

Chapter	Description
1	A description of the hardware used on this board
2	A map of the resources of the board
3	The features supported by the BIOS Setup program
4	The contents of the BIOS Setup program's menus and submenus
5	A description of the BIOS error messages, beep codes, and POST codes
6	A list of where to find information about specifications supported by the motherboard

Typographical Conventions

This section contains information about the conventions used in this specification. Not all of these symbols and abbreviations appear in all specifications of this type.

Notes, Cautions, and Warnings

NOTE

Notes call attention to important information.

CAUTION

Cautions are included to help you avoid damaging hardware or losing data.

WARNING

Warnings indicate conditions which, if not observed, can cause personal injury.

Other Common Notation

#	Used after a signal name to identify an active-low signal (such as USBP0#)
(NxnX)	When used in the description of a component, N indicates component type, xn are the relative coordinates of its location on the motherboard, and X is the instance of the particular part at that general location. For example, J5J1 is a connector, located at 5J. It is the first connector in the 5J area.
KB	Kilobyte (1024 bytes)
Kbit	Kilobit (1024 bits)
MB	Megabyte (1,048,576 bytes)
Mbit	Megabit (1,048,576 bits)
GB	Gigabyte (1,073,741,824 bytes)
xxh	An address or data value ending with a lowercase h indicates a hexadecimal value.
x.x V	Volts. Voltages are DC unless otherwise specified.
†	This symbol is used to indicate third-party brands and names that are the property of their respective owners.

Contents

1 Motherboard Description

What This Chapter Contains

1.1 Overview

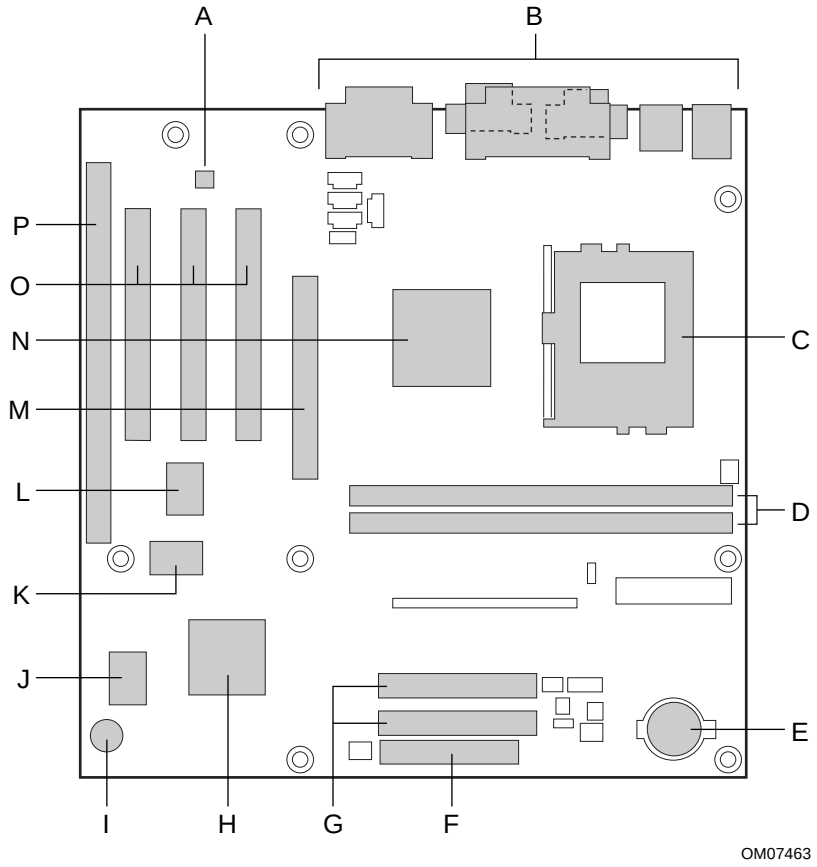
The BI440ZX motherboard's features are summarized below:

Form Factor	microATX (9.6 inches by 9.6 inches)
Processor	Support for an Intel® Celeron™ processor in a PPGA package
Memory	• Two 168-pin dual inline memory module (DIMM) sockets • Supports up to 256 MB of 66 MHz synchronous DRAM (SDRAM)
Chipset	Intel® 82440ZX AGPset, consisting of: • Intel® 82443ZX PCI/AGP controller (PAC) • Intel® 82371EB PCI ISA IDE Xcelerator (PIIX4E)
I/O Control	SMSC FDC37M807 I/O controller
Peripheral Interfaces	• Two serial ports • Two Universal Serial Bus (USB) ports • One parallel port • Two IDE interfaces with Ultra DMA support • One diskette drive interface
Expansion capabilities	Four add-in card expansion slots: • One Accelerated Graphics Port (AGP) connector • One shared expansion slot for either a PCI bus or an ISA bus add-in card • Two dedicated PCI bus add-in card connectors
BIOS	• Intel/AMI BIOS • Intel® E28F200B5 2 Mbit flash memory • Support for Advanced Power Management (APM), Advanced Configuration and Power Interface (ACPI), Plug and Play, and SMBIOS

For information about	Refer to
Manufacturing options	Section 1.1.2, page 14
The board's compliance level with APM, ACPI, Plug and Play, and SMBIOS	Section 6.2, page 99

1.1.1 Motherboard Layout

Figure 1 shows the location of the major components on the motherboard.



A	CS4297 audio codec (optional)	J	SMSC FDC37M807 I/O controller
B	Back panel connectors	K	Flash memory
C	Processor socket	L	Creative Sound Blaster† AudioPCI 64V AC '97 digital controller (optional)
D	DIMM sockets		
E	Battery	M	AGP connector
F	Diskette drive connector	N	Intel 82443ZX PAC
G	IDE connectors	O	PCI bus add-in card connectors
H	Intel 82371EB PIIX4E	P	ISA bus add-in card connector
I	Speaker		

Figure 1. Motherboard Components

1.1.2 Manufacturing Options

The following are manufacturing options. Not all manufacturing options are available in all marketing channels. Please contact your Intel representative to determine what manufacturing options are available to you.

- Audio subsystem
  - AC ’97 Crystal CS4297 audio codec
  - Creative Sound Blaster AudioPCI 64V AC ’97 Digital Controller
  - CD-ROM (legacy-style 2 mm) connector
  - Video source line in connector
  - Auxiliary line in connector
  - Telephony connector
  - ATAPI CD-ROM connector
- Power supply fan control connector
- SCSI hard drive LED
- System fan connector
- USB front panel connector
- USB port 0 routing jumper
- Wake on Ring connector

1.2 Processor

The motherboard supports an Intel Celeron processor in a PPGA package at the speeds listed in Table 1. The processor speed is automatically selected. All supported onboard memory can be cached.

Table 1. Processor Speeds Supported by the Motherboard

Processor Speed	Host Bus Frequency	Cache Size
300A MHz	66 MHz	128 KB
333 MHz	66 MHz	128 KB

For information about	Refer to
Processor support for the BI440ZX motherboard	http://support.intel.com/support/motherboards/desktop

1.3 Memory

The motherboard has two DIMM sockets. Using the serial presence detect (SPD) data structure, programmed into an E^2PROM on the DIMM, the BIOS can determine the SDRAM's size and speed. Minimum memory size is 16 MB; maximum memory size is 256 MB. Memory can be installed in one or both sockets. Memory size can vary between sockets.

The motherboard supports the following memory features:

- 168-pin SPD or non-SPD DIMMs with gold-plated contacts
- 66 MHz or 100 MHz unbuffered SDRAM
- 64-bit (non-ECC) memory
- 3.3 V memory only
- Single- or double-sided DIMMs in the sizes listed in Table 2

Table 2. Supported Memory Sizes and Configurations

DIMM Size	Configuration
16 MB	2 Mbit x 64
32 MB	4 Mbit x 64
64 MB	8 Mbit x 64
128 MB	16 Mbit x 64

All memory components and DIMMs used with this motherboard must comply with the following PC SDRAM specifications:

- *PC SDRAM Specification* (memory component specific)
- *PC Unbuffered SDRAM Specifications*
- *PC Serial Presence Detect Specification*

For information about	Refer to
Obtaining copies of PC SDRAM specifications	http:// www.intel.com/design/pcisets/memory

NOTE

The board is compatible with both 66 MHz and 100 MHz DIMMs, but installing faster speed memory will not increase system performance, because of the 66 MHz host bus frequency.

CAUTION

To be fully compliant with all applicable Intel SDRAM specifications, use DIMMs that support the SPD data structure. If your memory modules do not support SPD, you will see a notification to this effect on the screen at power up. The BIOS will attempt to configure the memory controller for normal operation, however, non-SPD DIMMs might not function at the determined frequency. Refer to the PC Serial Presence Detect Specification *for more information.*

1.4 Chipset

The Intel 82440ZX AGPset consists of the Intel 82443ZX PAC and the Intel 82371EB PIIX4E bridge chip. The PAC provides an optimized DRAM controller and an Accelerated Graphics Port (AGP) interface. The I/O subsystem of the 82440ZX is based on the PIIX4E, which is a highly integrated PCI ISA IDE Xcelerator Bridge.

1.4.1 Intel® 82443ZX PAC

The Intel 82443ZX PAC provides bus-control signals, address paths, and data paths for transfers between the processor's host bus, the PCI bus, the AGP, and main memory. The PAC features:

- Processor interface control
  - — Support for processor host bus frequency of 66 MHz
  - — 32-bit addressing
  - — Desktop optimized GTL+ compliant host bus interface
- Integrated DRAM controller, with support for
  - — +3.3 V only DIMM DRAM configurations
  - — Up to two double-sided DIMMs
  - — 100-MHz or 66-MHz SDRAM
  - — DIMM serial presence detect via SMBus interface
  - — 16- and 64-Mbit devices with 2 KB, 4 KB, and 8 KB page sizes
  - — x 4, x 8, x 16, and x 32 DRAM widths
  - — Symmetrical and asymmetrical DRAM addressing
- AGP interface
  - — Complies with the AGP specification (see Section 6.2 for specification information)
  - — Support for AGP 2X device
  - — Synchronous coupling to the host bus frequency
- PCI bus interface
  - — Complies with the PCI specification Rev. 2.1, +5 V 33-MHz interface (see Section 6.2 for specification information)
  - — Asynchronous coupling to the host-bus frequency
  - — PCI parity generation support
  - — Data streaming support from PCI-to-DRAM
  - — Support for four PCI bus masters in addition to the host and PCI-to-ISA I/O bridge
  - — Support for concurrent host, AGP, and PCI transactions to main memory
- Data buffering
  - — DRAM write buffer with read-around-write capability
  - — Dedicated host-to-DRAM, PCI0-to-DRAM, and PCI1/AGP-to-DRAM read buffers
  - — AGP dedicated inbound/outbound FIFOs, used for temporary data storage
- Power management functions
  - — Support for system suspend/resume
  - — Compliant with ACPI power management
- SMBus support for desktop management functions
- Support for system management mode (SMM)

1.4.2 Intel® 82371EB (PIIX4E)

The PIIX4E is a multifunctional PCI device implementing the PCI-to-ISA bridge, PCI IDE functionality, USB host/hub functionality, and enhanced power management. The PIIX4E features:

- Multifunctional PCI-to-ISA bridge
  - Support for the PCI bus at 33 MHz
  - PCI specification-compliant (see Section 6.2 for specification information)
  - Full ISA bus support
- USB controller
  - Two USB ports (see Section 6.2 for specification information)
  - Support for legacy keyboard and mouse
  - Support for Universal Host Controller Interface (UHCI) Design Guide (see Section 6.2 for specification information)
- Integrated dual-channel enhanced IDE interface
  - Support for up to four IDE devices
  - PIO Mode 4 transfers at up to 16 MB/sec
  - Support for Ultra DMA/33 synchronous DMA mode transfers at up to 33 MB/sec
  - Bus master mode with an 8 x 32-bit buffer for bus master PCI IDE burst transfers
- Enhanced DMA controller
  - Two 8237-based DMA controllers
  - Support for PCI DMA with three PC/PCI channels and distributed DMA protocols
  - Fast type-F DMA for reduced PCI bus usage
- Interrupt controller based on 82C59
  - Support for 15 interrupts
  - Programmable for edge/level sensitivity
- Power management logic
  - Sleep/resume logic
  - Support for Wake on Ring and Wake on LAN† technology
  - Support for APM and ACPI (see Section 6.2 for specification information)
- Real-Time Clock
  - 256-byte battery-backed CMOS SRAM
  - Date alarm
- 16-bit counters/timers based on 82C54

1.4.3 AGP

AGP is a high-performance bus for graphics-intensive applications, such as 3D applications. AGP, while based on the *PCI Local Bus Specification*, Rev. 2.1, is independent of the PCI bus and is intended for exclusive use with graphical display devices. AGP overcomes certain limitations of the PCI bus related to handling large amount of graphics data with the following features:

- Pipelined memory read and write operations that hide memory access latency
- Demultiplexing of address and data on the bus for nearly 100 percent bus efficiency

For information about	Refer to
The location of the AGP connector	Figure 7, page 41
The signal names of the AGP connector	Table 29, page 45
Obtaining the *Accelerated Graphics Port Interface Specification*	Section 6.2, page 99

1.4.4 USB

The motherboard has two USB ports; one USB peripheral can be connected to each port. For more than two USB devices, an external hub can be connected to either port. The two USB ports are implemented with stacked back panel connectors. The motherboard fully supports UHCI and uses UHCI-compatible software drivers. USB features include:

- Self-identifying peripherals that can be plugged in while the computer is running
- Automatic mapping of function to driver and configuration
- Support for isochronous and asynchronous transfer types over the same set of wires
- Support for up to 127 physical devices
- Guaranteed bandwidth and low latencies appropriate for telephony, audio, and other applications
- Error-handling and fault-recovery mechanisms built into the protocol

With an optional jumper, USB port 0 on the back panel can be disabled or rerouted to an optional front panel USB connector.

NOTE

Computer systems that have an unshielded cable attached to a USB port may not meet FCC Class B requirements, even if no device or a low-speed USB device is attached to the cable. Use shielded cable that meets the requirements for full-speed devices.

For information about	Refer to
The location of the USB connectors on the back panel	Figure 3, page 29
The signal names of the USB connectors	Table 5, page 30
The jumper settings for USB port 0	Section 1.14.1, page 51
The USB and UHCI specifications	Section 6.2, page 99

1.4.5 IDE Support

The motherboard has two independent bus-mastering IDE interfaces. These interfaces support:

- ATAPI devices (such as CD-ROM drives)
- ATA devices using the transfer modes listed in Table 60 on page 84

The BIOS supports logical block addressing (LBA) and extended cylinder head sector (ECHS) translation modes. The drive reports the transfer rate and translation mode to the BIOS.

The motherboard supports laser servo (LS-120) diskette technology through its IDE interfaces. LS-120 diskette technology enables users to store 120 MB of data on a single, 3.5-inch removable diskette. LS-120 technology is backward-compatible (both read and write) with 1.44 MB and 720 KB DOS-formatted diskettes and is supported by the Windows† 95, Windows 98, and Windows NT† operating systems. The LS-120 drive can be configured as a boot device, if selected in the BIOS Setup program.

For information about	Refer to
The location of the IDE connectors	Figure 5, page 36
The signal names of the IDE connectors	Table 17, page 37

1.4.6 Real-Time Clock, CMOS SRAM, and Battery

The real-time clock is compatible with DS1287 and MC146818 components. The clock provides a time-of-day clock and a multicentury calendar with alarm features and century rollover. The real-time clock supports 256 bytes of battery-backed CMOS SRAM in two banks that are reserved for BIOS use.

A coin-cell battery powers the real-time clock and CMOS memory. When the computer is not plugged into a wall socket, the battery has an estimated life of three years. When the computer is plugged in, the 3.3 V standby current from the power supply extends the life of the battery. The clock is accurate to ± 13 minutes/year at 25 ºC with 3.3 VSB applied.

The time, date, and CMOS values can be specified in the BIOS Setup program. The CMOS values can be returned to their defaults by using the BIOS Setup program.

NOTE

The recommended method of accessing the date in systems with Intel® motherboards is indirectly from the Real Time Clock (RTC) via the BIOS. The BIOS on Intel motherboards and baseboards contains a century checking and maintenance feature. This feature checks the two least significant digits of the year stored in the RTC during each BIOS request (INT 1Ah) to read the date and, if less than 80 (i.e., 1980 is the first year supported by the PC), updates the century byte to 20. This feature enables operating systems and applications using the BIOS date/time services to reliably manipulate the year as a four-digit value.

For information about	Refer to
Proper date access in systems with Intel motherboards	http://support.intel.com/support/year2000/

1.5 I/O Controller

The FDC37M807 I/O controller from SMSC is an ISA Plug and Play-compatible, multifunctional I/O device that provides the following features (see Section 6.2 for Plug and Play information):

- Two serial ports
- Interface for one 1.2 MB, 1.44 MB, or 2.88 MB diskette drive
- Three-mode diskette drive support (driver required)
- FIFO support on both serial and diskette drive interfaces
- One parallel port with Extended Capabilities Port (ECP) and Enhanced Parallel Port (EPP) support
- PS/2†-style mouse and keyboard interfaces
- Support for serial IRQ packet protocol
- Intelligent power management, including:
  - — Shadowed write-only registers for ACPI compliance
  - — Programmable wake up event interface

The BIOS Setup program provides configuration options for the I/O controller.

1.5.1 Serial Ports

The motherboard has two 9-pin D-Sub serial port connectors located on the back panel. The serial ports' NS16C550-compatible UARTs support data transfers at speeds up to 115.2 Kbits/sec with BIOS support. The serial ports can be assigned as COM1 (3F8), COM2 (2F8), COM3 (3E8), or COM4 (2E8).

For information about	Refer to
The location of the serial port connectors	Figure 3, page 29
The signal names of the serial port connectors	Table 6, page 30

1.5.2 Parallel Port

The connector for the multimode bidirectional parallel port is a 25-pin D-Sub connector located on the back panel. In the BIOS Setup program, the parallel port can be configured for the following:

- Output only (AT†-compatible mode)
- Bi-directional (PS/2 compatible)
- EPP
- ECP

For information about	Refer to
The location of the parallel port connector	Figure 3, page 29
The signal names of the parallel port connector	Table 7, page 31

1.5.3 Diskette Drive Controller

The I/O controller supports a single diskette drive that is compatible with the 82077 diskette drive controller and supports both PC-AT† and PS/2 modes.

NOTE

The I/O controller supports 1.2 MB, 3.5-inch diskette drives, but a special driver is required is for this type of drive.

For information about	Refer to
The location of the diskette drive connector	Figure 5, page 36
The signal names of the diskette drive connector	Table 18, page 38
The supported diskette drive capacities and sizes	Table 61, page 85

1.5.4 Keyboard and Mouse Interface

PS/2 keyboard and mouse connectors are located on the back panel. The +5 V lines to these connectors are protected with a PolySwitch† circuit that, like a self-healing fuse, reestablishes the connection after an overcurrent condition is removed.

NOTE

The keyboard and mouse can be plugged into either of the PS/2 connectors. Power to the computer should be turned off before a keyboard or mouse is connected or disconnected.

The keyboard controller contains the Phoenix keyboard and mouse controller code, provides the keyboard and mouse control functions, and supports password protection for power on/reset. A power on/reset password can be specified in the BIOS Setup program.

The keyboard controller also supports the hot-key sequence <Ctrl><Alt><Del> for a software reset. This key sequence resets the computer's software by jumping to the beginning of the BIOS code and running the Power-On Self Test (POST).

For information about	Refer to
The location of the keyboard and mouse connectors	Figure 3, page 29
The signal names of the keyboard and mouse connectors	Table 4, page 30

1.6 Audio Subsystem (Optional)

The optional Audio Codec ’97 (AC’97) compatible audio subsystem includes these features:

- Split digital/analog architecture for improved S/N (signal-to-noise) ratio: ≥ 85dB – measured at line out, from any analog input, including line in, CD-ROM, and auxiliary line in
- 3-D stereo enhancement
- Power management support for APM 1.2 and ACPI 1.0
- Audio inputs:
  - Four analog line-level stereo inputs for connection from line in, CD, video source line in, and aux
  - Two analog line-level inputs for speakerphone input and PC beep
  - One mono microphone input
- Audio outputs:
  - Stereo line-level output
  - Mono output for speakerphone

The audio subsystem consists of the following:

- Creative Sound Blaster AudioPCI 64V AC ’97 digital controller
- Crystal Semiconductor CS4297 stereo audio codec
- Audio connectors (described in Section 1.6.3, beginning on page 23)

1.6.1 Creative Sound Blaster AudioPCI 64V AC ’97 V1.03 Digital Controller

- PCI 2.1 compliant
- PCI bus master for PCI audio
- 64 voice wavetable synthesizer
- Aureal A3D† API, Sound Blaster Pro†, Roland MPU 401 MIDI, joystick compatible
- Ensoniq 3D positional audio and Microsoft DirectSound† 3D support

1.6.2 Crystal Semiconductor CS4297 Stereo Audio Codec

- High performance 18-bit stereo full-duplex audio codec with up to 48 kHz sampling rate
- Connects to the Sound Blaster AudioPCI 64V using a five-wire digital interface

1.6.3 Audio Connectors

The audio connectors include the following:

- CD-ROM (legacy-style 2 mm connector)
- ATAPI-style connectors:
  - Video source line in
  - Auxiliary line in
  - Telephony
  - CD-ROM
- Back panel audio connectors:
  - Line out
  - Line in
  - Mic in
  - MIDI/Game Port

For information about	Refer to
The back panel audio connectors	Section 1.13.1, page 29

NOTE

Some of the audio connectors are optional and are not installed on all versions of the board.

1.6.3.1 CD-ROM (Legacy-style 2 mm) Connector

A 1 x 4-pin legacy-style 2 mm connector connects an internal CD-ROM drive to the audio mixer.

For information about	Refer to
The location of the legacy-style 2 mm connector	Figure 4, page 34
The signal names of the legacy-style 2 mm connector	Table 12, page 35

1.6.3.2 Video Source Line In Connector

A 1 x 4-pin ATAPI-style connector connects the left and right audio channel signals of an internal video device to the audio subsystem. An audio-in signal interface of this type is necessary for applications such as TV tuners.

For information about	Refer to
The location of the video source line in connector	Figure 4, page 34
The signal names of the video source line in connector	Table 13, page 35

1.6.3.3 Auxiliary Line In Connector

A 1 x 4-pin ATAPI-style connector connects the left and right channel signals of an internal audio device to the audio subsystem.

For information about	Refer to
The location of the auxiliary line in connector	Figure 4, page 34
The signal names of the auxiliary line in connector	Table 14, page 35

1.6.3.4 Telephony Connector

A 1 x 4-pin ATAPI-style connector connects the monoaural audio signals of an internal telephony device to the audio subsystem. A monaural audio-in and audio-out signal interface is necessary for telephony applications such as speakerphones, fax/modems, and answering machines.

For information about	Refer to
The location of the telephony connector	Figure 4, page 34
The signal names of the telephony connector	Table 15, page 35

1.6.3.5 ATAPI CD-ROM Audio Connector

A 1 x 4-pin ATAPI-style connector connects an internal ATAPI CD-ROM drive to the audio mixer.

For information about	Refer to
The location of the ATAPI CD-ROM connector	Figure 4, page 34
The signal names of the ATAPI CD-ROM connector	Table 16, page 35

1.6.4 Audio Drivers and Utilities

Audio software and utilities are available from Intel's World Wide Web site:

http://support.intel.com/support/motherboards/desktop

1.7 SCSI Hard Drive LED Connector (Optional)

The optional SCSI hard drive LED connector is a 1 x 2-pin connector that allows add-in SCSI controller applications to use the same LED as the IDE controller. This connector can be connected to the LED output of the add-in controller card. The LED will indicate when data is being read or written using the add-in controller.

For information about	Refer to
The location of the SCSI hard drive LED connector	Figure 5, page 36
The signal names of the SCSI hard drive LED connector	Table 19, page 38

1.8 Wake on LAN Technology

Wake on LAN technology enables remote wakeup of the computer through a network. Wake on LAN technology requires a PCI add-in network interface card (NIC) with remote wakeup capabilities. The remote wakeup connector on the NIC must be connected to the onboard Wake on LAN technology connector. The NIC monitors network traffic at the MII interface; upon detecting a Magic Packet†, the NIC asserts a wakeup signal that powers up the computer. To access this feature use the Wake on LAN technology connector.

⚠ CAUTION

For Wake on LAN technology, the 5-V standby line for the power supply must be capable of delivering +5 V ± 5 % at 720 mA. Failure to provide adequate standby current when implementing Wake on LAN technology, can damage the power supply.

For information about	Refer to
The location of the Wake on LAN technology connector	Figure 6, page 39
The signal names of the Wake on LAN technology connector	Table 25, page 40

1.9 Wake on Ring / Resume on Ring Technologies

This section describes two technologies that enable telephony devices to access the computer when it is in a power-managed state. The method used depends on the type of telephony device (external or internal) and the power management mode being used (APM or ACPI).

NOTE

Wake on ring and resume on ring technologies require the support of an operating system that provides full ACPI functionality.

For information about	Refer to
APM	Section 3.5.1, page 70
ACPI	Section 3.5.2, page 70

1.9.1 Wake on Ring Technology

The operation of Wake on Ring can be summarized as follows:

- Powers up the computer from either the APM soft-off mode or the ACPI S5 state
- Requires two calls to access the computer:
  - First call powers up the computer
  - Second call enables access (when the appropriate software is loaded)
- Detects incoming call differently for external as opposed to internal modems:
  - For external modems, motherboard hardware monitors the ring indicate (RI) input of serial port A (serial port B does not support this feature)
  - For internal modems, a cable must be routed from the modem to the Wake on Ring connector

The Wake on Ring connector is a manufacturing option.

For information about	Refer to
The location of the Wake on Ring connector	Figure 6, page 39
The signal names of the Wake on Ring connector	Table 23, page 40

1.9.2 Resume on Ring Technology

The operation of Resume on Ring can be summarized as follows:

- Resumes operation from either the APM sleep mode or the ACPI S1 state
- Requires only one call to access the computer
- Detects incoming call similarly for external and internal modems; does not use the Wake on Ring connector
- Requires modem interrupt be unmasked for correct operation

1.10 Power Connector

When used with an ATX-compliant power supply that supports remote power on/off, the motherboard can turn off the system power through software control. To enable soft-off control in software, advanced power management must be enabled in the BIOS Setup program and in the operating system. When the system BIOS receives the correct APM command from the operating system, the BIOS turns off power to the computer.

With soft-off enabled, if power to the computer is interrupted by a power outage or a disconnected power cord, when power resumes, the computer returns to the power state it was in before power was interrupted (on or off).

For information about	Refer to
The location of the power connector	Figure 6, page 39
The signal names of the power connector	Table 22, page 40
The ATX specification	Section 6.2, page 99

1.11 Speaker

A 47 Ω inductive speaker is mounted on the motherboard. The speaker provides audible error code (beep code) information during the power-on self test (POST).

For information about	Refer to
The location of the onboard speaker	Figure 1, page 13

1.12 Fan Connectors

The board has three fan connectors, two of which are manufacturing options. The functions of the these connectors are described in Table 3.

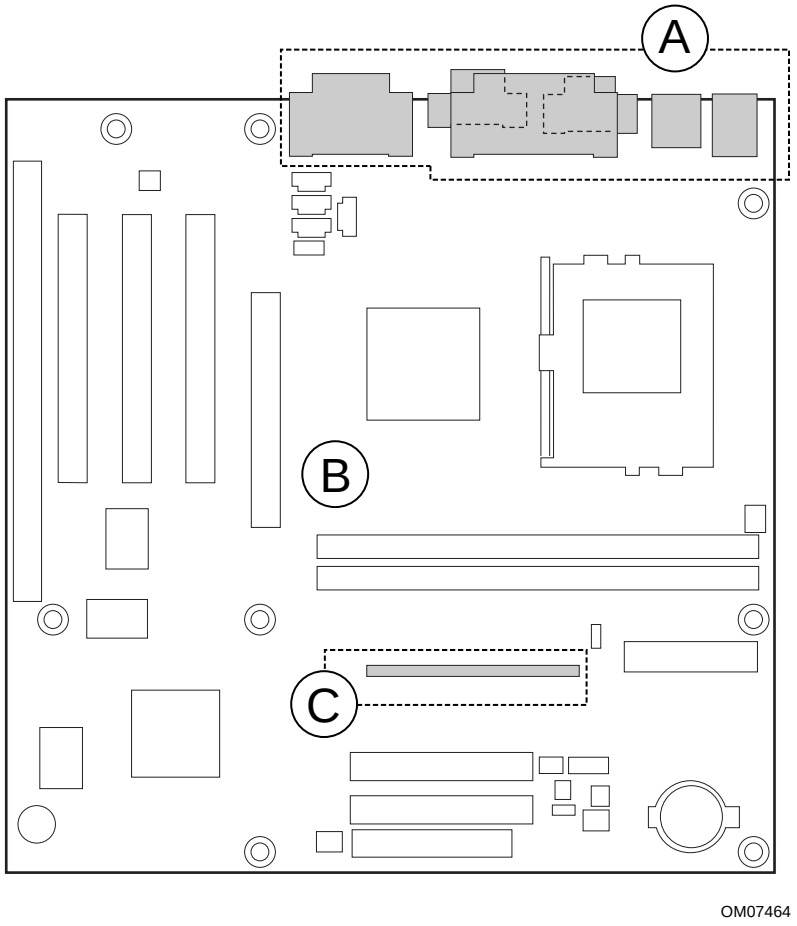
Table 3. Fan Connector Descriptions

Connector	Function
Processor fan	Provides +12 V DC for a processor fan or active fan heatsink
Power supply fan control (optional)	Provides an on/off control signal for a fan located inside of and powered by the system power supply
System fan (optional)	Provides +12 V DC for a system or chassis fan. The fan voltage can be switched on or off, depending on the power management state of the computer.

For information about	Refer to
The location of the fan connectors	Figure 6, page 39
The signal names of the fan connectors	Section 1.13.2.3, page 39

1.13 Connectors

This section describes the motherboard's connectors. The connectors can be divided into three groups, as shown in Figure 2.



A. **Back panel connectors (see page 29)**

B. **Midboard connectors (see page 33)**

C. **Front panel connectors (see page 46)**

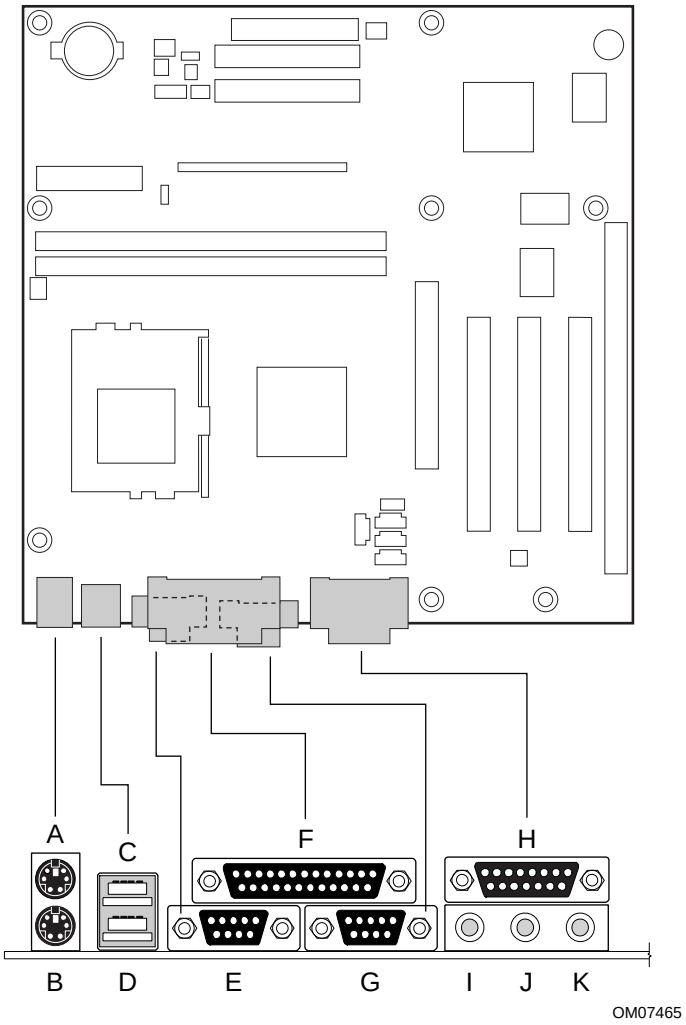
Figure 2. Connector Groups

CAUTION

Only the back panel connectors of this motherboard have overcurrent protection. The internal motherboard connectors are not overcurrent protected, and should connect only to devices inside the computer chassis, such as fans and internal peripherals. Do not use these connectors for powering devices external to the computer chassis. A fault in the load presented by the external devices could cause damage to the computer, the interconnecting cable, and the external devices themselves.

1.13.1 Back Panel Connectors

Figure 3 shows the location of the back panel connectors.



A	PS/2 keyboard or mouse
B	PS/2 keyboard or mouse
C	USB port 0
D	USB port 1
E	Serial port A
F	Parallel port
G	Serial port B
H	MIDI/Game port
I	Audio line out
J	Audio line in
K	Mic in

Figure 3. Back Panel Connectors

NOTE

The back panel audio line out connector is designed to power headphones or amplified speakers only. Poor audio quality may occur if passive (non-amplified) speakers are connected to this output.

Table 4. PS/2 Keyboard/Mouse Connectors

Pin	Signal Name
1	Data
2	Not connected
3	Ground
4	Fused +5 V
5	Clock
6	Not connected

Table 5. USB Connectors

Pin	Signal Name
1	+5 V (fused)
2	USBP0# [USBP1#]
3	USBP0 [USBP1]
4	Ground

Signal names in brackets ([ ]) are for USB port 1.

Table 6. Serial Port Connectors

Pin	Signal Name
1	DCD—Data Carrier Detect
2	SIN #—Serial Data In
3	SOUT #—Serial Data Out
4	DTR—Data Terminal Ready
5	Ground
6	DSR—Data Set Ready
7	RTS—Request to Send
8	CTS—Clear to Send
9	RI—Ring Indicator

Table 7. Parallel Port Connector

Pin	Standard Signal Name	ECP Signal Name	EPP Signal Name	I/O
1	STROBE#	STROBE#	WRITE#	I/O
2	PD0	PD0	PD0	I/O
3	PD1	PD1	PD1	I/O
4	PD2	PD2	PD2	I/O
5	PD3	PD3	PD3	I/O
6	PD4	PD4	PD4	I/O
7	PD5	PD5	PD5	I/O
8	PD6	PD6	PD6	I/O
9	PD7	PD7	PD7	I/O
10	ACK#	ACK#	INTR	I
11	BUSY	BUSY#, PERIPHACK	WAIT#	I
12	PERROR	PE, ACKREVERSE#	PE	I
13	SELECT	SELECT	SELECT	I
14	AUDOFD#	AUDOFD#, HOSTACK	DATASTB#	O
15	FAULT#	FAULT#, PERIPHREQST#	FAULT#	I
16	INIT#	INIT#, REVERSERQST#	RESET#	O
17	SLCTIN#	SLCTIN#	ADDRSTB#	O
18 - 25	GND	GND	GND	-

Table 8. Audio Line In Connector

Pin	Signal Name
Tip	Audio left in
Ring	Audio right in
Sleeve	Ground

Table 9. Audio Line Out Connector

Pin	Signal Name
Tip	Audio left out
Ring	Audio right out
Sleeve	Ground

Table 10. Audio Mic In Connector

Pin	Signal Name
Tip	Mono in
Ring	Mic bias voltage
Sleeve	Ground

Table 11. MIDI/Game Port Connector

Pin	Signal Name	Pin	Signal Name
1	+5 V (fused)	9	+5 V (fused)
2	GP4 (JSBUT0)	10	GP6 (JSBUT2)
3	GP0 (JSX1)	11	GP2 (JSX2)
4	Ground	12	MIDI-OUT
5	Ground	13	GP3 (JSY2)
6	GP1 (JSY1)	14	GP7 (JSBUT3)
7	GP5 (JSBUT1)	15	MIDI-IN
8	+5 V (fused)		

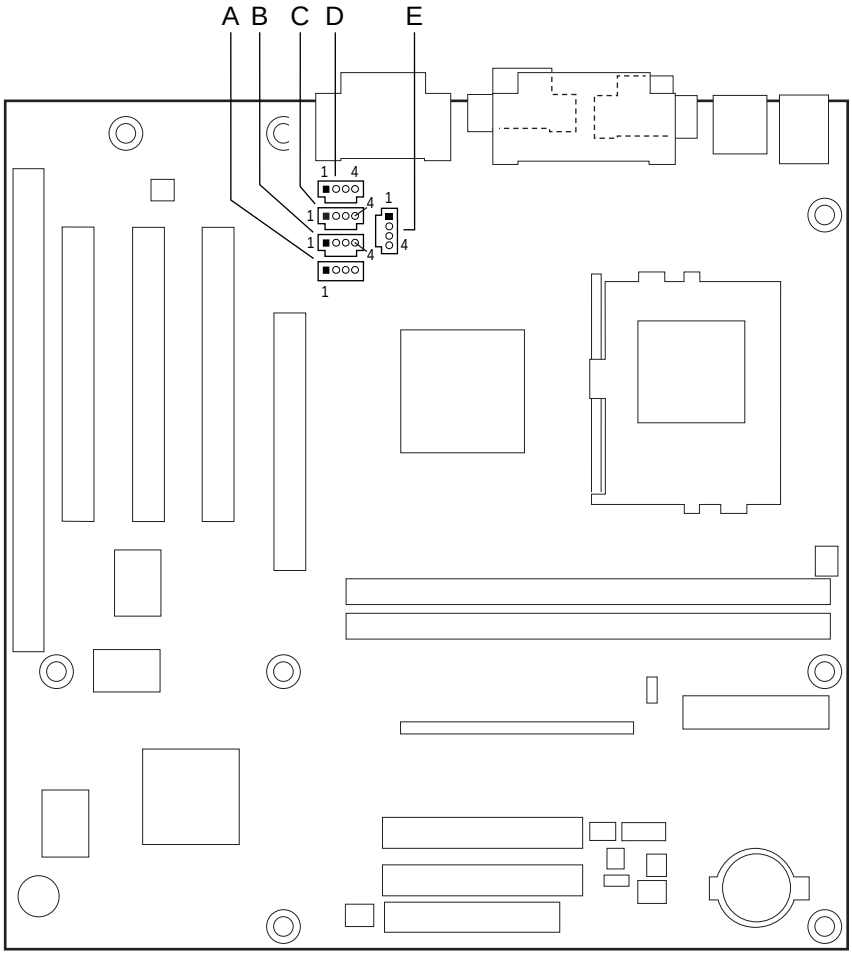
1.13.2 Midboard Connectors

The midboard connectors are divided into the following functional groups:

- Audio (see page 34)
  - CD-ROM (legacy-style 2 mm connector)
  - Video source line in
  - Auxiliary line in
  - Telephony
  - ATAPI CD-ROM
- Peripheral interfaces and indicators (see page 36)
  - USB front panel
  - SCSI LED
  - Diskette drive
  - IDE
- Hardware control (see page 39)
  - Fans
  - Power
  - Wake on Ring
  - Wake on LAN technology
- Add-in boards (see page 41)
  - ISA bus
  - PCI bus
  - AGP

1.13.2.1 Audio

Figure 4 shows the location of the audio connectors.



Item	Description	Color	Style	Reference Designator
A	CD-ROM (optional)	White	Legacy-style, 2 mm	J2D5
B	Video source line in (optional)	Blue	ATAPI	J2D4
C	Auxiliary line in (optional)	Natural	ATAPI	J2D2
D	Telephony (optional)	Green	ATAPI	J2D1
E	ATAPI CD-ROM (optional)	Black	ATAPI	J2E1

Figure 4. Audio Connectors

Table 12. CD-ROM Connector (J2D5)

Pin	Signal Name
1	Ground
2	CD_IN-Left
3	Ground
4	CD_IN-Right

Table 13. Video Source Audio Line In Connector (J2D4)

Pin	Signal Name
1	Left auxiliary line in
2	Ground
3	Ground
4	Right auxiliary line in

Table 14. Auxiliary Line In Connector (J2D2)

Pin	Signal Name
1	Left auxiliary line in
2	Ground
3	Ground
4	Right auxiliary line in

Table 15. Telephony Connector (J2D1)

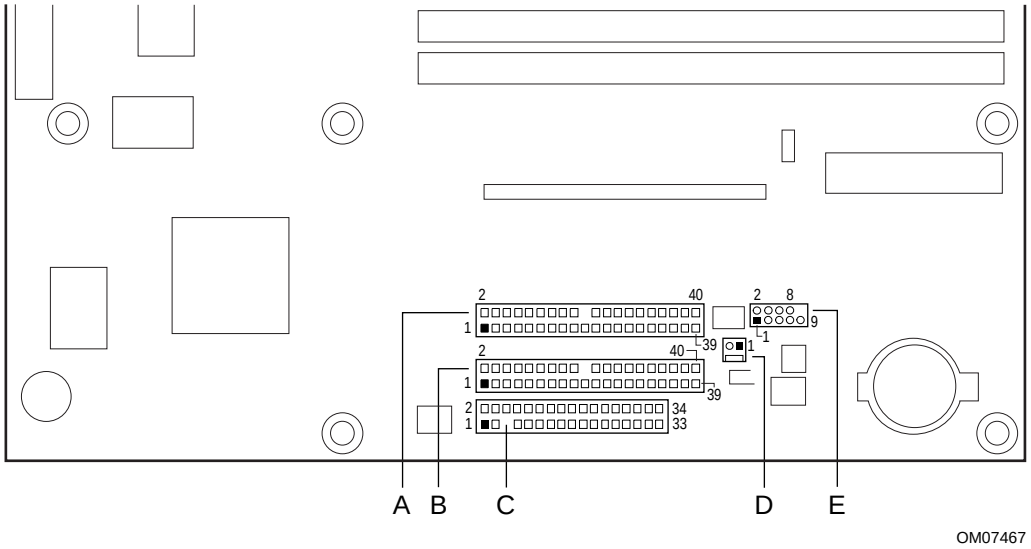
Pin	Signal Name
1	Analog audio mono input
2	Ground
3	Ground
4	Analog audio mono output

Table 16. ATAPI CD-ROM Connector (J2E1)

Pin	Signal Name
1	Left audio input from CD-ROM
2	CD audio differential ground
3	CD audio differential ground
4	Right audio input from CD-ROM

1.13.2.2 Peripheral Interfaces and Indicators

Figure 5 shows the location of the peripheral interface and indicator connectors.



Item	Description	Reference Designator
A	Secondary IDE	J9F1
B	Primary IDE	J9F2
C	Diskette drive	J10F1
D	SCSI LED (optional)	J9G2
E	USB front panel (optional)	J9H1

Figure 5. Peripheral Interface and Indicator Connectors

Table 17. PCI IDE Connectors (J9F2 [J9F1])

Pin	Signal Name	Pin	Signal Name
1	Reset IDE	2	Ground
3	Data 7	4	Data 8
5	Data 6	6	Data 9
7	Data 5	8	Data 10
9	Data 4	10	Data 11
11	Data 3	12	Data 12
13	Data 2	14	Data 13
15	Data 1	16	Data 14
17	Data 0	18	Data 15
19	Ground	20	Key
21	DDRQ0 [DDRQ1]	22	Ground
23	I/O Write#	24	Ground
25	I/O Read#	26	Ground
27	IOCHRDY	28	P_ALE (Cable Select pullup)
29	DDACK0# [DDACK1#]	30	Ground
31	IRQ 14 [IRQ 15]	32	Reserved
33	DAG1 (Address 1)	34	Reserved
35	DAG0 (Address 0)	36	DAG2Address 2
37	Chip Select 1P# [Chip Select 1S#]	38	Chip Select 3P# [Chip Select 3S#]
39	Activity#	40	Ground

Note: Signal names in brackets ([ ]) are for the secondary IDE connector.

Table 18. Diskette Drive Connector (J10F1)

Pin	Signal Name	Pin	Signal Name
1	Ground	2	DENSEL
3	Ground	4	Reserved
5	Key	6	FDEDIN
7	Ground	8	FDINDX# (Index)
9	Ground	10	FDM00# (Motor Enable A)
11	Ground	12	No connect
13	Ground	14	FDDS0# (Drive Select A)
15	Ground	16	No connect
17	No connect	18	FDDIR# (Stepper Motor Direction)
19	Ground	20	FDSTEP# (Step Pulse)
21	Ground	22	FDWD# (Write Data)
23	Ground	24	FDWE# (Write Enable)
25	Ground	26	FDTRK0# (Track 0)
27	No connect	28	FDWPD# (Write Protect)
29	Ground	30	FDRDATA# (Read Data)
31	Ground	32	FDHEAD# (Side 1 Select)
33	Ground	34	DSKCHG# (Diskette Change)

Table 19. SCSI LED Connector (J9G2)

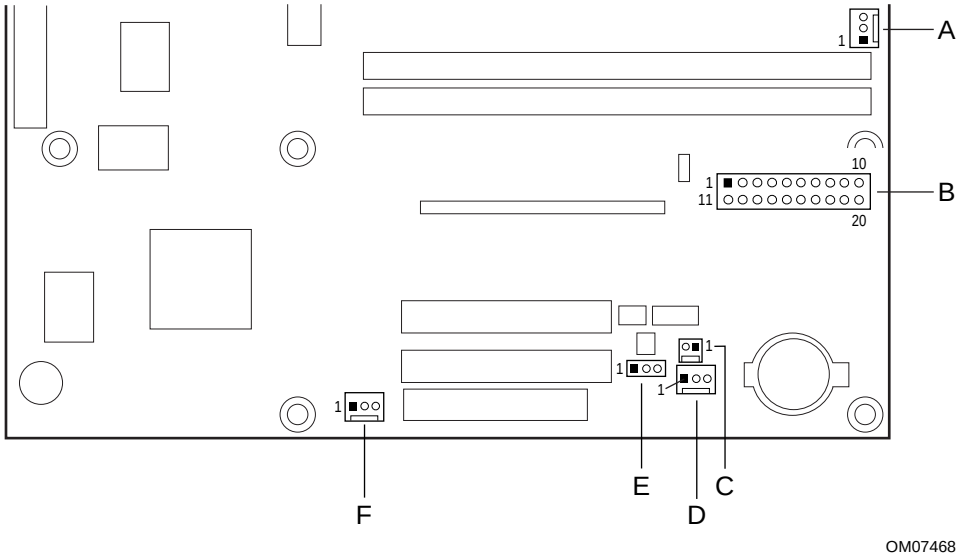
Pin	Signal Name
1	SCSI activity
2	Not connected

Table 20. USB Front Panel Connector (J9H1)

Pin	Signal Name	Pin	Signal Name
1	TP_FPUSB_1	2	VCC
3	Ground	4	TP_FUSB_4
5	TP_FPUSB_5	6	FNT_USBP0
7	Ground	8	FNT_USBP0 #
9	Ground		

1.13.2.3 Hardware Control

Figure 6 shows the location of the hardware control connectors.



Item	Description	Reference Designator
A	Processor fan	J6K1
B	Power	J7J1
C	Wake on Ring (optional)	J9H2
D	Power supply fan control (optional)	J9H3
E	Wake on LAN technology	J9G3
F	System fan (optional)	J10D1

Figure 6. Hardware Control Connectors

For information about	Refer to
Wake on LAN technology	Section 1.8, page 25
Wake on Ring technology	Section 1.9.1, page 26
The power connector	Section 1.10, page 27
The functions of the fan connectors	Section 1.12, page 27

Table 21. Processor Fan Connector (J6K1)

Pin	Signal Name
1	Ground
2	+12 V
3	Ground

Table 22. Power Connector (J7J1)

Pin	Signal Name	Pin	Signal Name
1	+3.3 V	11	+3.3 V
2	+3.3 V	12	-12 V
3	Ground	13	Ground
4	+5 V	14	PS-ON# (power supply remote on/off)
5	Ground	15	Ground
6	+5 V	16	Ground
7	Ground	17	Ground
8	PWRGD (Power Good)	18	-5 V
9	+5 VSB (Standby for real-time clock)	19	+5 V
10	+12 V	20	+5 V

NOTE

The standard SFX 90 W power supply may not be sufficient for the BI440ZX motherboard. For more information, see Section 1.16.3 on page 56.

Table 23. Wake on Ring Connector (J9H2)

Pin	Signal Name
1	Ground
2	RINGA#

Table 24. Power Supply Fan Control Connector (J9H3)

Pin	Signal Name
1	Ground
2	FAN_SUSP1
3	No connect

Table 25. Wake on LAN Technology Connector (J9G3)

Pin	Signal Name
1	+5 VSB
2	Ground
3	WOL

Table 26. System Fan Connector (J10D1)

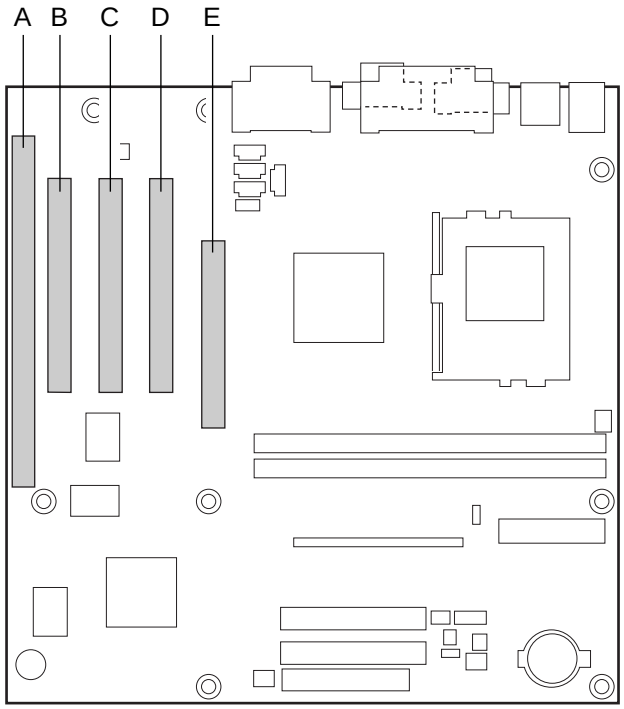
Pin	Signal Name
1	Ground
2	FAN_SUSP2
3	No connect

1.13.2.4 Add-In Boards

There are a maximum of four expansion slots for installing add-in cards, as follows:

- One shared expansion slot for an ISA or a PCI add-in card
- Two dedicated PCI expansion slots
- One AGP expansion slot

All of the PCI bus connectors are bus master capable. Figure 7 shows the location of the add-in board connectors.



Item	Description	Reference Designator
A	ISA bus connector (expansion shot shared with PCI Bus connector 3)	J4A2
B	PCI bus connector 3 (expansion shot shared with ISA bus connector)	J4A1
C	PCI bus connector 2	J4B1
D	PCI bus connector 1	J4C1
E	AGP connector	J4D1

Figure 7. Add-In Board Connectors

Table 27. ISA Bus Connector (J4A2)

Pin	Signal Name (Note 1)	Pin	Signal Name (Note 1)
B1	Ground	A1	IOCHK# (IOCHCK#)
B2	RESET (RESDRV)	A2	SD7
B3	+5 V (Note 2)	A3	SD6
B4	IRQ9	A4	SD5
B5	-5 V	A5	SD4
B6	DRQ2	A6	SD3
B7	-12 V	A7	SD2
B8	SRDY# (NOWS#)	A8	SD1
B9	+12 V	A9	SD0
B10	Ground	A10	IOCHRDY (CHRDY)
B11	SMEMW# (SMWTC#)	A11	AEN
B12	SMEMR# (SMRDC#)	A12	SA19
B13	IOW# (IOWC#)	A13	SA18
B14	IOR# (IORC#)	A14	SA17
B15	DACK3#	A15	SA16
B16	DRQ3	A16	SA15
B17	DACK1#	A17	SA14
B18	DRQ1	A18	SA13
B19	REFRESH#	A19	SA12
B20	BCLK	A20	SA11
B21	IRQ7	A21	SA10
B22	IRQ6	A22	SA9
B23	IRQ5	A23	SA8
B24	IRQ4	A24	SA7
B25	IRQ3	A25	SA6
B26	DACK2#	A26	SA5
B27	TC	A27	SA4
B28	BALE	A28	SA3
B29	+5 V	A29	SA2
B30	OSC	A30	SA1
B31	Ground	A31	SA0
Key		Key	
D1	MEMCS16# (M16#)	C1	SBHE#
D2	IOCS16# (IO16#)	C2	LA23
D3	IRQ10	C3	LA22
D4	IRQ11	C4	LA21
D5	IRQ12	C5	LA20
D6	IRQ15	C6	LA19

continued

Table 27. ISA Bus Connector (continued)

D7	IRQ14	C7	LA18
D8	DACK0#	C8	LA17
D9	DRQ0	C9	MEMR# (MRDC#)
D10	DACK5#	C10	MEMW# (MWTC#)
D11	DRQ5	C11	SD8
D12	DACK6#	C12	SD9
D13	DRQ6	C13	SD10
D14	DACK7#	C14	SD11
D15	DRQ7	C15	SD12
D16	+5 V	C16	SD13
D17	Master16# (MASTER#)	C17	SD14
D18	Ground	C18	SD15

Notes:

1. Items in parentheses are alternate versions of signal names.
2. If an SFX power supply is used with this motherboard, -5 V DC will not be present at pin B5 of ISA bus connector.

Table 28. PCI Bus Connectors (J4C1, J4B1, J4A1)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	Ground (TRST#)*	B1	-12 V	A32	AD16	B32	AD17
A2	+12 V	B2	Ground (TCK)*	A33	+3.3 V	B33	C/BE2#
A3	+5 V (TMS)*	B3	Ground	A34	FRAME#	B34	Ground
A4	+5 V (TDI)*	B4	no connect (TDO)*	A35	Ground	B35	IRDY#
A5	+5 V	B5	+5 V	A36	TRDY#	B36	+3.3 V
A6	INTA#	B6	+5 V	A37	Ground	B37	DEVSEL#
A7	INTC#	B7	INTB#	A38	STOP#	B38	Ground
A8	+5 V	B8	INTD#	A39	+3.3 V	B39	LOCK#
A9	Reserved	B9	no connect (PRSNT1#)*	A40	+5 V (SDONE)*	B40	PERR#
A10	+5 V (I/O)	B10	Reserved	A41	+5 V (SBO#)*	B41	+3.3 V
A11	Reserved	B11	no connect (PRSNT2#)*	A42	Ground	B42	SERR#
A12	Ground	B12	Ground	A43	PAR	B43	+3.3 V
A13	Ground	B13	Ground	A44	AD15	B44	C/BE1#
A14	+3.3 V aux	B14	Reserved	A45	+3.3 V	B45	AD14
A15	RST#	B15	Ground	A46	AD13	B46	Ground
A16	+5 V (I/O)	B16	CLK	A47	AD11	B47	AD12
A17	GNT#	B17	Ground	A48	Ground	B48	AD10
A18	Ground	B18	REQ#	A49	AD09	B49	Ground
A19	PME#	B19	+5 V (I/O)	A50	Key	B50	Key
A20	AD30	B20	AD31	A51	Key	B51	Key
A21	+3.3 V	B21	AD29	A52	C/BE0#	B52	AD08
A22	AD28	B22	Ground	A53	+3.3 V	B53	AD07
A23	AD26	B23	AD27	A54	AD06	B54	+3.3 V
A24	Ground	B24	AD25	A55	AD04	B55	AD05
A25	AD24	B25	+3.3 V	A56	Ground	B56	AD03
A26	IDSEL	B26	C/BE3#	A57	AD02	B57	Ground
A27	+3.3 V	B27	AD23	A58	AD00	B58	AD01
A28	AD22	B28	Ground	A59	+5 V (I/O)	B59	+5 V (I/O)
A29	AD20	B29	AD21	A60	REQ64C#	B60	ACK64C#
A30	Ground	B30	AD19	A61	+5 V	B61	+5 V
A31	AD18	B31	+3.3 V	A62	+5 V	B62	+5 V

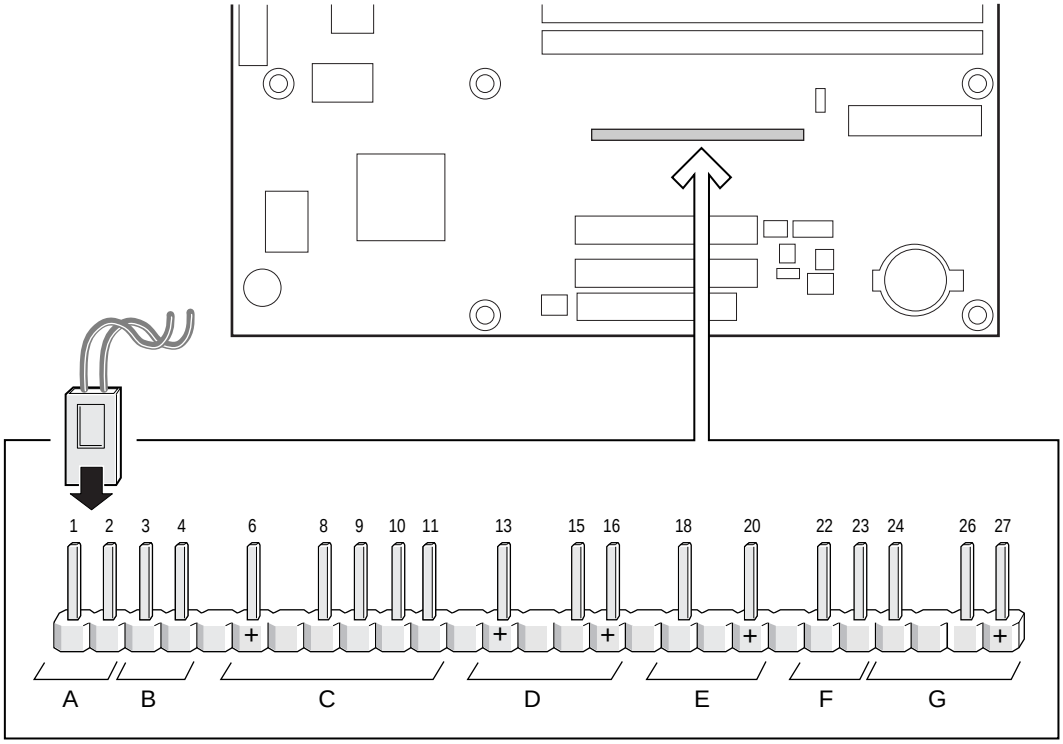
* These signals (in parentheses) are optional in the PCI specification and are not currently implemented.

Table 29. AGP Bus Connector (J4D1)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	+12V	B1	No Connect	A34	Vcc3.3	B34	Vcc3.3
A2	No Connect	B2	Vcc	A35	AD22	B35	AD21
A3	Reserved	B3	Vcc	A36	AD20	B36	AD19
A4	No Connect	B4	No Connect	A37	Ground	B37	Ground
A5	Ground	B5	Ground	A38	AD18	B38	AD17
A6	INTA#	B6	INTB#	A39	AD16	B39	C/BE2#
A7	RST#	B7	CLK	A40	Vcc3.3	B40	Vcc3.3
A8	GNT1#	B8	REQ#	A41	FRAME#	B41	IRDY#
A9	Vcc3.3	B9	Vcc3.3	A42	Reserved	B42	+3.3 V aux
A10	ST1	B10	ST0	A43	Ground	B43	Ground
A11	Reserved	B11	ST2	A44	Reserved	B44	Reserved
A12	PIPE#	B12	RBF#	A45	Vcc3.3	B45	Vcc3.3
A13	Ground	B13	Ground	A46	TRDY#	B46	DEVSEL#
A14	No Connect	B14	No Connect	A47	STOP#	B47	Vcc3.3
A15	SBA1	B15	SBA0	A48	PME#	B48	PERR#
A16	Vcc3.3	B16	Vcc3.3	A49	Ground	B49	Ground
A17	SBA3	B17	SBA2	A50	PAR	B50	SERR#
A18	Reserved	B18	SB_STB	A51	AD15	B51	C/BE1#
A19	Ground	B19	Ground	A52	Vcc3.3	B52	Vcc3.3
A20	SBA5	B20	SBA4	A53	AD13	B53	AD14
A21	SBA7	B21	SBA6	A54	AD11	B54	AD12
A22	Key	B22	Key	A55	Ground	B55	Ground
A23	Key	B23	Key	A56	AD9	B56	AD10
A24	Key	B24	Key	A57	C/BE0#	B57	AD8
A25	Key	B25	Key	A58	Vcc3.3	B58	Vcc3.3
A26	AD30	B26	AD31	A59	Reserved	B59	AD_STB0
A27	AD28	B27	AD29	A60	AD6	B60	AD7
A28	Vcc3.3	B28	Vcc3.3	A61	Ground	B61	Ground
A29	AD26	B29	AD27	A62	AD4	B62	AD5
A30	AD24	B30	AD25	A63	AD2	B63	AD3
A31	Ground	B31	Ground	A64	Vcc3.3	B64	Vcc3.3
A32	Reserved	B32	AD_STB1	A65	AD0	B65	AD1
A33	C/BE3#	B33	AD23	A66	SMB0	B66	SMB1

1.13.3 Front Panel Connector

Figure 8 shows the location of the front panel connector and Table 30 lists the connector signals.



A	Power switch
B	Sleep/Resume switch
C	Infrared port
D	Hard drive activity LED
E	Power LED
F	Reset switch
G	Offboard speaker

Figure 8. Front Panel Connector

Table 30. Front Panel Connector (J8F1)

Group	Function	Pin Number	Signal Name
A	Power Switch (PWR ON)	1	SW_ON#
		2	Ground
B	Sleep/Resume Switch (SLEEP)	3	SLEEP_REQ#
		4	Ground
		5	Key
C	Infrared (IrDA) Port (INFRARED)	6	+5 V
		7	Key
		8	IR_RX
		9	Ground
		10	IR_TX
		11	Open
		12	Key
D	Hard Drive Activity LED (HD LED)	13	HD_PWR +5 V (5 V, 15 mA maximum)
		14	Key
		15	HD Active#
		16	HD_PWR +5 V (5 V, 15 mA maximum)
E	Power LED (PWR LED)	17	Key
		18	PWR_LED0 (yellow)
		19	Key
		20	PWR_LED1 (green)
F	Reset Switch (RESET)	21	Key
		22	Ground
		23	FP_RESET#
G	Offboard Speaker (SPEAKER)	24	SPINNEG
		25	Key
		26	SPINPOS
		27	+5 V

1.13.3.1 Power Switch

These pins can be connected to a front panel power switch. The switch must pull the SW_ON# pin to ground for at least 50 ms to signal the power supply to switch on or off. (The time requirement is due to internal debounce circuitry on the motherboard.) At least two seconds must pass before the power supply will recognize another on/off signal.

1.13.3.2 Sleep/Resume Switch Connector

When APM is enabled in the system BIOS, and the operating system's APM driver is loaded, the system can enter sleep (standby) mode in one of the following ways:

- Optional front panel sleep/resume button
- Prolonged system inactivity using the BIOS inactivity timer feature

The 2-pin connector located on the front panel connector supports a front panel sleep/resume switch, which must be a momentary SPST type that is normally open.

Closing the sleep/resume switch sends a System Management Interrupt (SMI) to the processor, which immediately goes into SMM. While the computer is in sleep mode, it is fully capable of responding to and servicing external interrupts (such as an incoming fax) even though the monitor turns on only if a keyboard or mouse interrupt occurs. To reactivate or resume system operation, the sleep/resume switch must be pressed again, or the keyboard or mouse must be used.

For information about	Refer to
APM	Section 3.5.1, page 70
The BIOS inactivity timer	Table 66, page 87

NOTE

The Sleep/Resume switch feature is supported only by APM; ACPI does not support this feature.

1.13.3.3 Infrared Port Connector

Serial Port B can be configured to support an IrDA module connected to this 5-pin connector. After the IrDA interface is configured, files can be transferred to or from portable devices such as laptops, PDAs, and printers using application software.

1.13.3.4 Hard Drive Activity LED Connector

These pins can be connected to an LED to provide a visual indicator that data is being read from or written to a hard drive. For the LED to function properly, an IDE drive must be connected to the onboard IDE interface. The LED will also show activity for devices connected to the SCSI hard drive LED connector.

For information about	Refer to
The SCSI hard drive LED connector	Section 1.7, page 25

1.13.3.5 Power LED/Sleep/Message Waiting Connector

These pins can be connected to a single- or dual-colored LED. Table 31 shows the possible states for a single-colored LED. Table 32 shows the possible states for a dual-colored LED.

Table 31. States for a Single-colored Power LED

LED State	Description
Off	Power off
Steady Green	Running
Blinking Green	Running/message waiting

Table 32. States for a Dual-colored Power LED

LED State	Description
Off	Power off
Steady Green	Running
Blinking Green	Running/message waiting
Steady Yellow	Sleeping
Blinking Yellow	Sleeping/message waiting

NOTE

To utilize the message waiting function, a message-capturing software application must be invoked.

1.13.3.6 Reset Switch Connector

These pins can be connected to a momentary SPST type switch that is normally open. When the switch is closed, the motherboard resets and runs the POST.

1.13.3.7 Offboard Speaker Connector

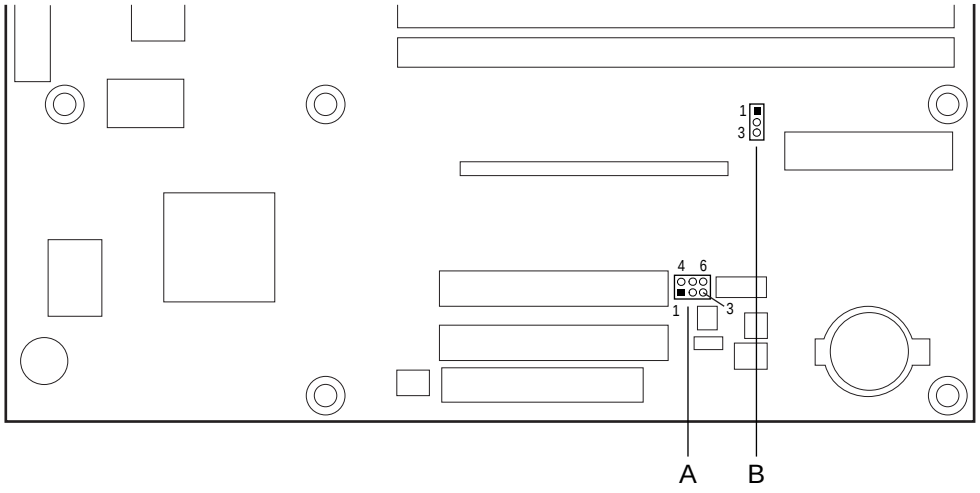
An offboard speaker can be connected to the motherboard at the front panel connector. The speaker (onboard or offboard) provides error beep code information during the POST in the event that the computer cannot use the video interface. The speaker is not connected to the audio subsystem and does not receive output from the audio subsystem.

1.14 Jumper Blocks

The motherboard has two jumper blocks. Figure 9 shows the location of the motherboard's jumper blocks.

CAUTION

Do not move any jumpers with the power on. Always turn off the power and unplug the power cord from the computer before changing a jumper setting. Otherwise, damage to the motherboard could occur.



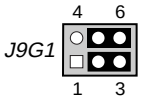
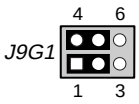
Item	Description	Reference Designator
A	USB port 0 routing jumper block (optional)	J9G1
B	BIOS setup configuration jumper block	J7H1

Figure 9. Location of the Jumper Blocks

1.14.1 USB Port 0 Routing Jumper Block (optional)

This 6-pin jumper block routes the signals of USB port 0. Table 33 describes the jumper settings for USB port 0.

Table 33. USB Port 0 Routing Jumper Settings (J9G1)

Jumper Setting		Configuration
2-3 and 5-6		USB Port 0 signals are routed to the back panel
1-2 and 4-5		USB Port 0 signals are routed for a front panel USB connector

1.14.2 BIOS Setup Configuration Jumper Block

This 3-pin jumper block determines the BIOS Setup program's mode. Table 34 describes the jumper settings for the three modes: normal, configure, and recovery.

Table 34. BIOS Setup Configuration Jumper Settings (J7H1)

Function / Mode	Jumper Setting	Configuration
Normal	1-2 	The BIOS uses current configuration information and passwords for booting.
Configure	2-3 	After the POST runs, Setup runs automatically. The maintenance menu is displayed.
Recovery	none 	The BIOS attempts to recover the BIOS configuration. A recovery diskette is required.

For information about	Refer to
How to access the BIOS Setup program	Section 4.1, page 77
The maintenance menu of the BIOS Setup program	Section 4.2, page 78
BIOS recovery	Section 3.7, page 73

1.15 Mechanical Considerations

1.15.1 microATX Form Factor

The motherboard is designed to fit into a microATX-form-factor chassis. Figure 10 illustrates the mechanical form factor for the motherboard. Dimensions are given in inches. The outer dimensions are 9.6 inches by 9.6 inches. Location of the I/O connectors and mounting holes are in compliance with the microATX specification (see Section 6.2).

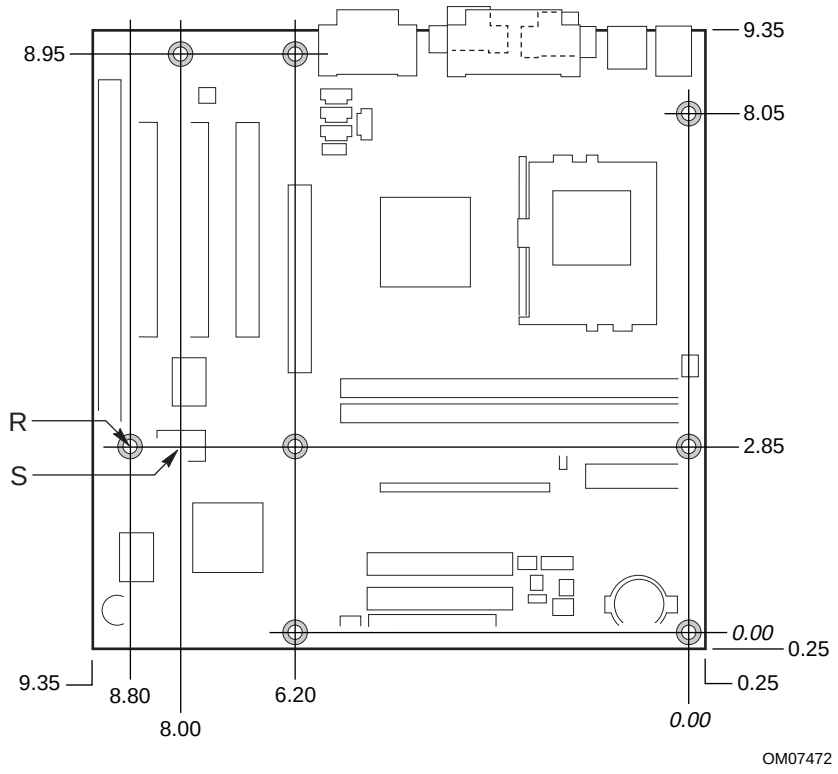


Figure 10. Motherboard Dimensions

⚠ **CAUTION**

As permitted by the microATX specification, the optional hole at location S in Figure 10 was omitted from the BI440ZX. The chassis standoff in this position should not be implemented or should be removable to avoid damage to traces on the motherboard.

1.15.2 I/O Shield

The back panel I/O shield for the motherboard must meet specific dimension and material requirements. Systems based on this motherboard need the back panel I/O shield to pass certification testing. Figure 11 shows the critical dimensions of the chassis-dependent I/O shield. Figure 12 shows the critical dimensions of the chassis-independent I/O shield. Dimensions are given in inches. Both figures indicate the position of each cutout. Additional design considerations for I/O shields relative to chassis requirements are described in the microATX specification. The dimensions of the back panel I/O shield for a microATX form factor are identical to the dimensions for an ATX form factor. See Section 6.2 for information about the microATX specification.

NOTE

An I/O shield specifically designed for the Intel® ATX chassis is available from Intel.

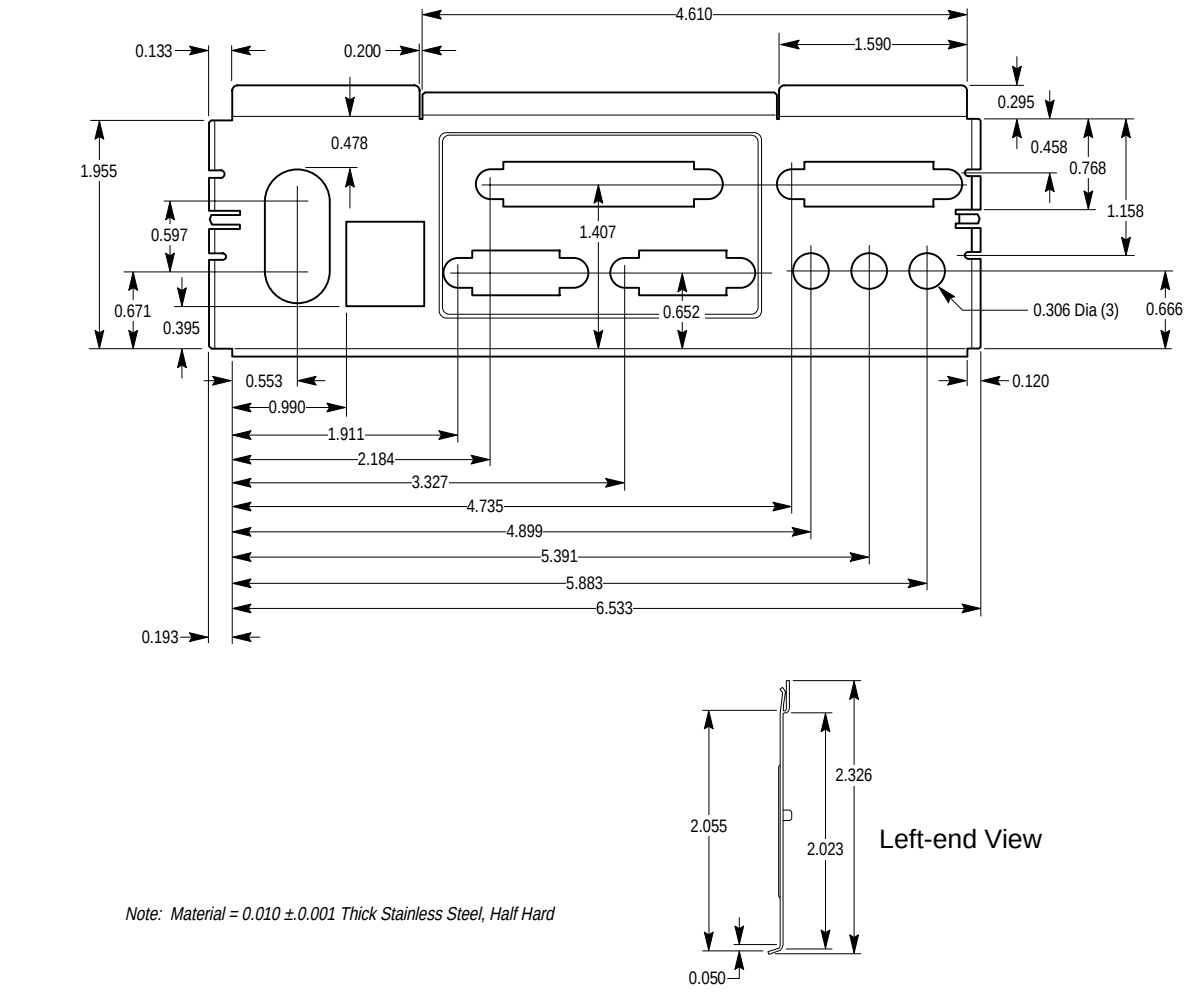


Figure 11. Back Panel I/O Shield Dimensions (Intel® ATX/microATX Chassis)

NOTE

A chassis-independent I/O shield designed to be compliant with the ATX chassis specification 2.01 is available from Intel.

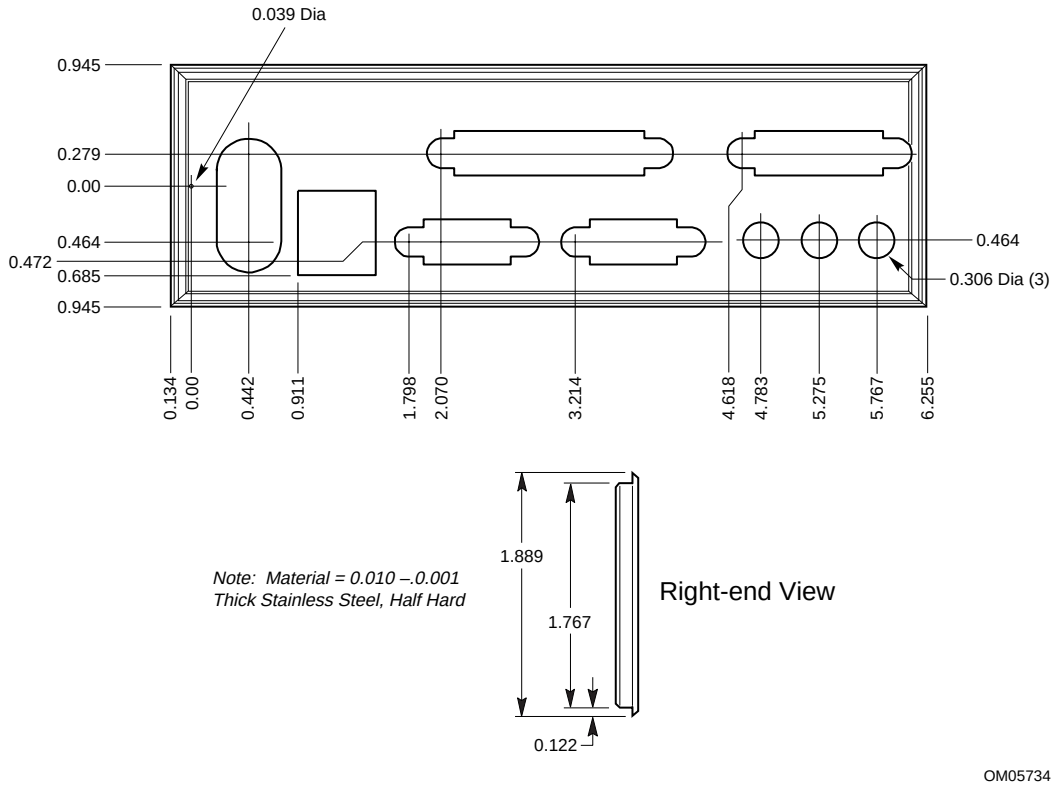


Figure 12. Back Panel I/O Shield Dimensions (ATX/microATX Chassis-Independent)

1.16 Electrical Considerations

1.16.1 Add-in Board Considerations

The motherboard is designed to provide 2 A (average) of +5 V current for each add-in board. The total +5 V current draw for add-in boards in a fully-loaded motherboard (all four expansion slots filled) must not exceed 8 A.

1.16.2 Power Consumption

Table 35 and Table 36 list voltage and current specifications for a computer that contains the motherboard, a 333 MHz Celeron processor with a 128 KB cache, 64 MB SDRAM, a 3.5-inch diskette drive, a 2.16 GB IDE hard disk drive, and an 8X IDE CD-ROM drive. This information is provided only as a guide for calculating approximate power usage with additional resources added.

Values for the Windows 95 desktop mode are measured at 640 x 480 x 256 colors and 60 Hz refresh rate. AC watts are measured with a typical 145 W supply, nominal input voltage and frequency, with true RMS wattmeter at the line input.

Table 35. DC Voltage

Voltage	Acceptable Tolerance	Wattage	Current
+3.3 V	± 5%	46 W	13.94 A
+5 V	± 5%	40 W	8 A
-5 V	± 5%	0 W	0 A
+12 V	± 5%	9 W	750 mA
-12 V	± 5%	3 W	250 mA
5 V SB (Stand By)	± 5%	3.6 W	720 mA

Table 36. Power Usage

Enabled APM Mode	AC Watts	DC Amps at: +3.3 V	+5 V	-5 V	+12 V	-12 V	+5 VSB
Standard (APM disabled)	46 W	1.8 A	2.0 A	0.2 A	0.8 A	0.6 A	0.7 A
Advanced (APM enabled)	46 W	1.7 A	1.8 A	0.2 A	0.8 A	0.4 A	0.7 A
Advanced with video suspend, standby, or sleep	29 W	1.2 A	0.8 A	0.2 A	0.5 A	0.2 A	0.5 A
Advanced with video sleep and IDE drive powered down	27 W	1.2 A	0.7 A	0.2 A	0.4 A	0.2 A	0.5 A

For typical configurations, the motherboard is designed to operate with at least a 200 W power supply. Use a higher wattage supply for heavily loaded configurations.

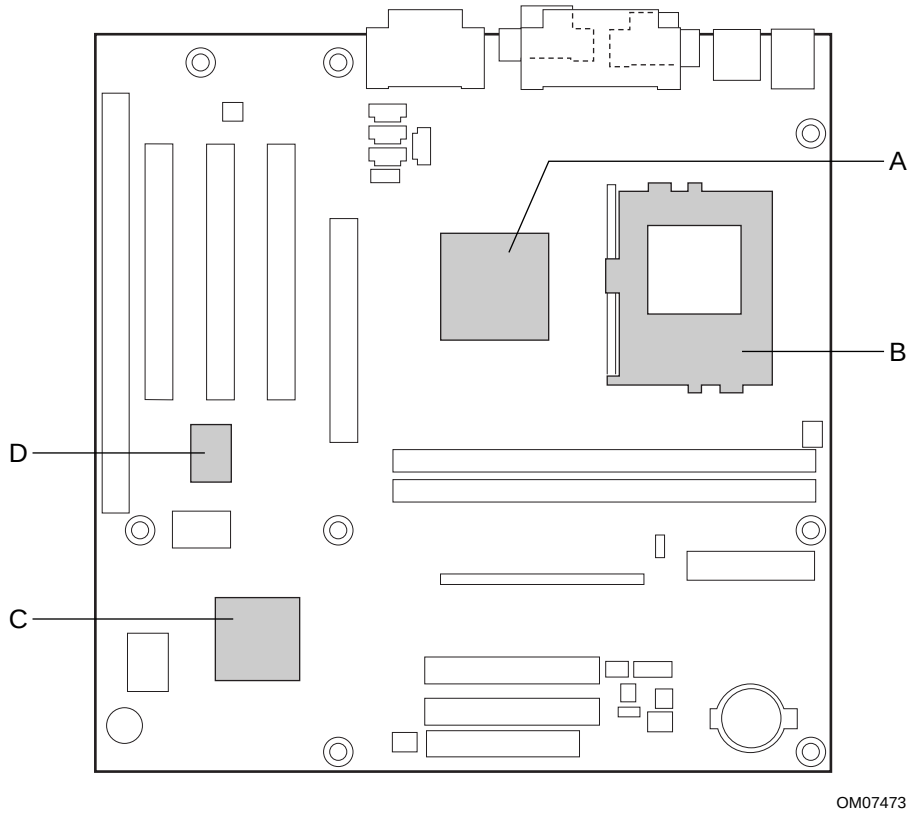
1.16.3 Power Supply Considerations

System integrators should refer to the power usage values listed in Table 35 when selecting a power supply for use with this motherboard. The power supply must comply with the following recommendations found in the indicated sections of the ATX form factor specification (see Section 6.2).

- The potential relation between 3.3 VDC and +5 VDC power rails (Section 4.2)
- The current capability of the +5 VSB line (Section 4.2.1.2)
- All timing parameters (Section 4.2.1.3)
- All voltage tolerances (Section 4.2.2)

1.17 Thermal Considerations

Figure 13 shows the locations of the thermally-sensitive components. Table 37 provides maximum component case temperatures for motherboard components that could be sensitive to thermal changes. Case temperatures could be affected by the operating temperature, current load, or operating frequency. Maximum case temperatures are important when considering proper airflow to cool the motherboard.



A	Intel 82443ZX PAC
B	Processor
C	Intel 82371EB PIIX4E
D	Sound Blaster AudioPCI 64V digital controller

Figure 13. Thermally-sensitive Components

⚠ CAUTION

An ambient temperature that exceeds the board's maximum operating temperature by 5 °C to 10 °C could cause components to exceed their maximum case temperature and malfunction. For information about the maximum operating temperature, see the environmental specifications in Section 1.19.

Table 37. Thermal Considerations for Components

Component	Maximum Case Temperature	
Celeron processor	300A MHz	85 °C
	333 MHz	85 °C
Intel 82443ZX (PAC)	105 °C	
Sound Blaster AudioPCI 64V digital controller	70 °C	
Intel 82371EB (PIIX4E)	85 °C	

1.18 Reliability

The mean time between failures (MTBF) prediction is calculated using component and subassembly random failure rates. The calculation is based on the Bellcore Reliability Prediction Procedure, TR-NWT-000332, Issue 4, September 1991. The MTBF prediction is for estimating repair rates and spare parts requirements.

The Mean Time Between Failures (MTBF) data is calculated from predicted data at 55 ºC.

Motherboard MTBF: 309,047.36 hours

1.19 Environmental

Table 38 lists the environmental specifications for the motherboard.

Table 38. Motherboard Environmental Specifications

Parameter	Specification		
Temperature			
Non-Operating	-40 °C to +70 °C		
Operating	0 °C to +55 °C		
Shock			
Unpackaged	30 g trapezoidal waveform		
	Velocity change of 170 inches/second		
Packaged	Half sine 2 millisecond		
	Product Weight	Free Fall (inches)	Velocity Change (inches/sec)
	<20 lbs.	36	167
	21-40 lbs.	30	152
	41-80 lbs.	24	136
	81-100 lbs.	18	118
Vibration			
Unpackaged	5 Hz to 20 Hz : 0.01 g^2 Hz sloping up to 0.02 g^2 Hz		
	20 Hz to 500 Hz : 0.02 g^2 Hz (flat)		
Packaged	10 Hz to 40 Hz : 0.015 g^2 Hz (flat)		
	40 Hz to 500 Hz : 0.015 g^2 Hz sloping down to 0.00015 g^2 Hz		

1.20 Regulatory Compliance

This motherboard complies with the following safety and EMC regulations when correctly installed in a compatible host system.

Table 39. Safety Regulations

Regulation	Title
UL 1950/CSA950, 3rd edition, Dated 07-28-95	Bi-National Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (USA and Canada)
EN 60950, 2nd Edition, 1992 (with Amendments 1, 2, 3, and 4)	The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (European Community)
IEC 950, 2nd edition, 1991 (with Amendments 1, 2, 3, and 4)	The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (International)
EMKO-TSE (74-SEC) 207/94	Summary of Nordic deviations to EN 60950. (Norway, Sweden, Denmark, and Finland)

Table 40. EMC Regulations

Regulation	Title
FCC Class B	Title 47 of the Code of Federal Regulations, Parts 2 and 15, Subpart B, pertaining to unintentional radiators. (USA)
CISPR 22, 2nd Edition, 1993 (Class B)	Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (International)
VCCI Class B (ITE)	Implementation Regulations for Voluntary Control of Radio Interference by Data Processing Equipment and Electronic Office Machines. (Japan)
EN55022 (1994) (Class B)	Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (Europe)
EN50082-1 (1992)	Generic Immunity Standard; Currently compliance is determined via testing to IEC 801-2, -3, and -4. (Europe)
ICES-003 (1997)	Interference-Causing Equipment Standard, Digital Apparatus, Class B (Including CRC c.1374) (Canada)

This printed circuit assembly has the following product certification markings

- UL Joint Recognition Mark: Consists of small c followed by a stylized backward UR and followed by a small US (Component side)
- Manufacturer's recognition mark: Consists of a unique UL recognized manufacturer's logo, along with a flammability rating (94V-0) (Solder side)
- UL File Number for motherboards: E139761 (Component side)
- PB Part Number: Intel bare circuit board part number (Solder side) 720848-001
- Battery "+ Side Up" marking: located on the component side of the board in close proximity to the battery holder
- FCC Logo/Declaration: (Solder side)
- CE Mark: (Component side) The CE mark should also be on the shipping container

2 Motherboard Resources

What This Chapter Contains

2.1 Memory Map

Table 41. System Memory Map

Address Range (decimal)	Address Range (hex)	Size	Description
1024 K - 262144 K	100000 - FFFFFFF	255 MB	Extended memory
960 K - 1024 K	F0000 - FFFFF	64 KB	Runtime BIOS
896 K - 960 K	E0000 - EFFFF	64 KB	Reserved
800 K - 896 K	C8000 - DFFFF	96 KB	Available high DOS memory (open to ISA and PCI bus)
640 K - 800 K	A0000 - C7FFF	160 KB	Video memory and BIOS
639 K - 640 K	9FC00 - 9FFFF	1 KB	Extended BIOS data (movable by memory manager software)
512 K - 639 K	80000 - 9FBFF	127 KB	Extended conventional memory
0 K - 512 K	00000 - 7FFFF	512 K	Conventional memory

2.2 DMA Channels

Table 42. DMA Channels

DMA Channel Number	Data Width	System Resource
0	8- or 16-bits	Audio
1	8- or 16-bits	Audio / parallel port
2	8- or 16-bits	Diskette Drive
3	8- or 16-bits	Parallel port (for ECP or EPP)/audio
4		Reserved - cascade channel
5	16-bits	Open
6	16-bits	Open
7	16-bits	Open

2.3 I/O Map

Table 43. I/O Map

Address (hex)	Size	Description
0000 - 000F	16 bytes	PIIX4E - DMA 1
0020 - 0021	2 bytes	PIIX4E - interrupt controller 1
0040 - 0043	4 bytes	PIIX4E - counter/timer 1
0048 - 004B	4 bytes	PIIX4E - counter/timer 2
0060	1 byte	Keyboard controller byte - reset IRQ
0061	1 byte	PIIX4E - NMI, speaker control
0064	1 byte	Keyboard controller, CMD/STAT byte
0070, bit 7	1 bit	PIIX4E - enable NMI
0070, bits 6:0	7 bits	PIIX4E - real time clock, address
0071	1 byte	PIIX4E - real time clock, data
0070 -0071	2 bytes	CMOS Bank 0
0072 - 0073	2 bytes	CMOS Bank 1
0080 - 008F	16 bytes	PIIX4E - DMA page registers
00A0 - 00A1	2 bytes	PIIX4E - interrupt controller 2
00B2 - 00B3	2 bytes	APM control
00C0 - 00DE	31 bytes	PIIX4E - DMA 2
00F0	1 byte	Reset numeric error
0170 - 0177	8 bytes	Secondary IDE channel
01F0 - 01F7	8 bytes	Primary IDE channel
0200, or (Note 1) 0208, or 0210, or 0218	(Note 2)	Audio / game port
0220 - 022F	16 bytes	Audio (Sound Blaster Pro compatible)
0240 - 024F	16 bytes	Audio (Sound Blaster Pro compatible)
0278 - 027F	8 bytes	LPT2
0228 - 022F	8 bytes	LPT3
02E8 - 02EF	8 bytes	COM4/video (8514A)
02F8 - 02FF	8 bytes	COM2
0320 - 0327, or (Note 1) 0330 - 0337, or 0340 - 0347, or 0350 - 0357	8 bytes	MPU-401
0376	1 byte	Secondary IDE channel command port
0377	1 byte	Floppy channel 2 command
0377, bit 7	1 bit	Floppy disk change, channel 2

continued

Table 43. I/O Map (continued)

Address (hex)	Size	Description
0377, bits 6:0	7 bits	Secondary IDE channel status port
0378 - 037F	8 bytes	LPT 1
0388- 038B	6 bytes	AdLib† (FM synthesizer)
03B4 - 03B5	2 bytes	Video (VGA)
03BA	1 byte	Video (VGA)
03C0 - 03CA	2 bytes	Video (VGA)
03CC	1 byte	Video (VGA)
03CE - 03CF	2 bytes	Video (VGA)
03D4 - 03D5	2 bytes	Video (VGA)
03DA	1 byte	Video (VGA)
03E8 - 03EF	8 bytes	COM3
03F0 - 03F5	6 bytes	Diskette Channel 1
03F6	1 byte	Primary IDE channel command port
03F7 (Write)	1 byte	Diskette channel 1 command
03F7, bit 7	1 bit	Diskette disk change channel 1
03F7, bits 6:0	7 bits	Primary IDE channel status port
03F8 - 03FF	8 bytes	COM1
04D0 - 04D1	2 bytes	Edge/level triggered PIC
0530 - 0537, or (Note 3) 0E80 - 0E87, or 0F40 - 0F47	8 bytes	Windows Sound System
LPTn + 400h	8 bytes	ECP port, LPTn base address + 400h
0CF8 - 0CFB (Note 4)	4 bytes	PCI configuration address register
0CF9 (Note 5)	1 byte	Turbo and reset control register
0CFC - 0CFF	4 bytes	PCI configuration data register
EF00 - EF3F	64 bytes	Windows Sound System
FFA0 - FFA7	8 bytes	Primary bus master IDE registers
FFA8 - FFAF	8 bytes	Secondary bus master IDE registers
xx00 - xx3F, or (Note 1) xx40 - xx7F, or xx80 - xxBF, or xxC0 - xxFF	64 bytes	Audio controller

Notes:

1. These are the four possible starting addresses for this device
2. The range for this device can vary from 1 byte to 8 bytes
3. These are the three possible starting addresses for this device
4. DWORD access only
5. Byte access only

2.4 PCI Configuration Space Map

Table 44. PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	Description
00	00	00	Intel 82443ZX (PAC)
00	01	00	Intel 82443ZX PCI/AGP bridge
00	07	00	Intel 82371EB (PIIX4E) PCI/ISA bridge
00	07	01	Intel 82371EB (PIIX4E) IDE bus master
00	07	02	Intel 82371EB (PIIX4E) USB
00	07	03	Intel 82371EB (PIIX4E) power management
00	0C	00	PCI audio controller (Sound Blaster AudioPCI 64V)
00	0E	00	PCI bus connector 1 (J4C1)
00	0F	00	PCI bus connector 2 (J4B1)
00	10	00	PCI bus connector 3 (J4A1)
01	00	00	AGP bus connector (J4D1)

2.5 Interrupts

Table 45. Interrupts

IRQ	System Resource
NMI	I/O Channel Check
0	Reserved, Interval Timer
1	Reserved, Keyboard Buffer Full
2	Reserved, Cascade Interrupt From Slave PIC
3	COM2*
4	COM1*
5	LPT2 (Plug and Play option) / Audio / User available
6	Diskette Drive
7	LPT1*
8	Real Time Clock
9	Reserved for PIIX4E system management bus
10	User available
11	Windows Sound System* / User available
12	Onboard Mouse Port (if present, else user available)
13	Reserved, Math Coprocessor
14	Primary IDE (if present, else user available)
15	Secondary IDE (if present, else user available)

* Default, but can be changed to another IRQ

2.6 PCI Interrupt Routing Map

This section describes interrupt sharing and how the interrupt signals are connected between the PCI bus connectors and onboard PCI devices. The PCI specification specifies how interrupts can be shared between devices attached to the PCI bus. In most cases, the small amount of latency added by interrupt sharing does not affect the operation or throughput of the devices. In some special cases where maximum performance is needed from a device, a PCI device should not share an interrupt with other PCI devices. Use the following information to avoid sharing an interrupt with a PCI add-in card.

PCI devices are categorized as follows to specify their interrupt grouping:

- INTA: By default, all add-in cards that require only one interrupt are in this category. For almost all cards that require more than one interrupt, the first interrupt on the card is also classified as INTA.
- INTB: Generally, the second interrupt on add-in cards that require two or more interrupts is classified as INTB. (This is not an absolute requirement.)
- INTC and INTD: Generally, a third interrupt on add-in cards is classified as INTC and a fourth interrupt is classified as INTD.

The PIIX4E PCI-to-ISA bridge has four programmable interrupt request (PIRQ) input signals. Any PCI interrupt source (either onboard or from a PCI add-in card) connects to one of these PIRQ signals. Because there are only four signals, some PCI interrupt sources are mechanically tied together on the motherboard and therefore share the same interrupt. Table 46 lists the PIRQ signals and shows how the signals are connected to the PCI bus connectors and to onboard PCI interrupt sources.

Table 46. PCI Interrupt Routing Map

PIIX4 PIRQ Signal Name	AGP Bus Connector (J4D1)	PCI Bus Connector 1 (J4C1)	PCI Bus Connector 2 (J4B1)	PCI Bus Connector 3 (J4A1)	PCI Audio	USB
PIRQA	INTA	INTD	INTC	INTB		
PIRQB		INTA	INTD	INTC	INTA	
PIRQC	INTB	INTB	INTA	INTD		
PIRQD		INTC	INTB	INTA		INTA

For example, assume an add-in card has one interrupt (group INTA) into PCI bus connector 3. In this PCI bus connector, an interrupt source from group INTA connects to the PIRQD signal, which is already connected to the USB PCI source. The add-in card shares an interrupt with this onboard interrupt source.

NOTE

The PIIX4E can connect each PIRQ line internally to one of the IRQ signals (3, 4, 5, 7, 9, 10, 11, 14, 15). Typically, a device that does not share a PIRQ line will have a unique interrupt. However, in certain interrupt-constrained situations, it is possible for two or more of the PIRQ lines to be connected to the same IRQ signal.

3 Overview of BIOS Features

What This Chapter Contains

3.1 Introduction

The motherboard uses an Intel/AMI BIOS, which is stored in flash memory and can be upgraded using a disk-based program. In addition to the BIOS, the flash memory contains the BIOS Setup program, POST, APM, the PCI auto-configuration utility, and Windows 95-ready Plug and Play. See Section 6.2 for the supported versions of these specifications.

This motherboard supports system BIOS shadowing, allowing the BIOS to execute from 64-bit onboard write-protected DRAM.

The BIOS displays a message during POST identifying the type of BIOS and a revision code. The initial production BIOS is identified as 4B4IZ0XA.86A.

3.2 BIOS Flash Memory Organization

The Intel E28F200B5 2-Mbit flash component is organized as 256 KB x 8 bits and is divided into areas as described in Table 47. The table shows the addresses in the ROM image in normal mode (the addresses change in BIOS Recovery Mode).

Table 47. Flash Memory Organization

Address (Hex)	Size	Description
FFFFC000 - FFFFFFFF	16 KB	Boot Block
FFFFA000 - FFFFBFFF	8 KB	Vital Product Data (VPD) Extended System Configuration Data (ESCD) (SMBIOS configuration data / Plug and Play data)
FFFF9000 - FFFF9FFF	4 KB	Used by BIOS (for activities such as Event Logging)
FFFF8000 - FFFF8FFF	4 KB	OEM logo or Scan Flash Area
FFFC0000 - FFFF7FFF	224 KB	Main BIOS Block

3.3 Resource Configuration

3.3.1 Plug and Play: PCI Autoconfiguration

The BIOS can automatically configure PCI devices and Plug and Play devices. PCI devices may be onboard or add-in cards. Plug and Play devices are ISA devices built to meet the Plug and Play specification. Autoconfiguration lets a user insert or remove PCI or Plug and Play cards without having to configure the system. When a user turns on the system after adding a PCI or Plug and Play card, the BIOS automatically configures interrupts, the I/O space, and other system resources. Any interrupts set to Available in Setup are considered to be available for use by the add-in card.

PCI interrupts are distributed to available ISA interrupts that have not been assigned to an ISA card or to system resources. The assignment of PCI interrupts to ISA IRQs is nondeterministic. PCI devices can share an interrupt, but an ISA device cannot share an interrupt allocated to PCI or to another ISA device. Autoconfiguration information is stored in ESCD format.

For information about the versions of PCI and Plug and Play supported by this BIOS, see Section 6.2.

3.3.2 ISA Plug and Play

If Plug and Play operating system (see Section 4.4.1 on page 80) is selected in the BIOS Setup program, the BIOS autoconfigures only ISA Plug and Play cards that are required for booting (IPL devices). If Plug and Play operating system is not selected in Setup, the BIOS autoconfigures all Plug and Play ISA cards. ISA legacy devices are not autoconfigurable. As a result, the resources for them must be reserved in the BIOS Setup program.

3.3.3 PCI IDE Support

If you select Auto in the BIOS Setup program, the BIOS automatically sets up the two PCI IDE connectors with independent I/O channel support. The IDE interface supports hard drives up to PIO Mode 4 and recognizes any ATAPI devices, including CD-ROM drives, tape drives, and Ultra DMA drives (see Section 6.2 for the supported version of ATAPI). Add-in ISA IDE controllers are not supported. The BIOS determines the capabilities of each drive and configures them to optimize capacity and performance. To take advantage of the high capacities typically available today, hard drives are automatically configured for Logical Block Addressing (LBA) and to PIO Mode 3 or 4, depending on the capability of the drive. You can override the auto-configuration options by specifying manual configuration in the BIOS Setup program.

NOTE

Do not connect an ATA device as a slave on the same IDE cable as an ATAPI master device.

3.4 System Management BIOS (SMBIOS)

SMBIOS is a Desktop Management Interface (DMI) compliant method for managing computers in a managed network.

The main component of SMBIOS is the management information format (MIF) database, which contains information about the computing system and its components. Using SMBIOS, a system administrator can obtain the system types, capabilities, operational status, and installation dates for system components. The MIF database defines the data and provides the method for accessing this information. The BIOS enables applications such as Intel® LANDesk® Client Manager to use SMBIOS. The BIOS stores and reports the following SMBIOS information:

- BIOS data, such as the BIOS revision level
- Fixed-system data, such as peripherals, serial numbers, and asset tags
- Resource data, such as memory size, cache size, and processor speed
- Dynamic data, such as event detection and error logging

OEMs can use a utility available from Intel that programs flash memory so the BIOS can report system and chassis information.

Non-Plug and Play operating systems, such as Windows NT, require an additional interface for obtaining the SMBIOS information. The BIOS supports an SMBIOS table interface for such operating systems. Using this support, an SMBIOS service-level application running on a non-Plug and Play operating system can obtain the SMBIOS information.

For information about	Refer to
The board's compliance level with SMBIOS	Section 6.2, page 99

3.5 Power Management

The BIOS supports both APM and ACPI. If the board is used with an ACPI-aware operating system, the BIOS provides ACPI support. Otherwise, it defaults to APM support.

3.5.1 APM

The energy saving standby mode can be initiated in the following ways:

- Time-out period specified in the BIOS Setup program
- Suspend/resume switch connected to the front panel sleep connector
- From the operating system, such as the Suspend menu item in Windows 95

In standby mode, the motherboard can reduce power consumption by spinning down hard drives, and reducing power to or turning off VESA DPMS-compliant monitors. Power-management mode can be enabled or disabled in the BIOS Setup program.

While in standby mode, the system retains the ability to respond to external interrupts and service requests, such as incoming faxes or network messages. Any keyboard or mouse activity brings the system out of standby mode and immediately restores power to the monitor.

The BIOS enables APM by default; but the operating system must support an APM driver for the power-management features to work. For example, Windows 95 supports the power-management features upon detecting that APM is enabled in the BIOS.

For information about	Refer to
Enabling or disabling power management in the BIOS Setup program	Section 4.6 , page 87
The board's compliance level with APM	Section 6.2, page 99

3.5.2 ACPI

ACPI gives the operating system direct control over the power management and Plug and Play functions of a computer. The use of ACPI with this board requires the support of an operating system that provides full ACPI functionality. ACPI features include:

- Plug and Play (including bus and device enumeration) and APM functionality normally contained in the BIOS
- Power management control of individual devices, add-in boards (some add-in boards may require an ACPI-aware driver), video displays, and hard disk drives
- Methods for achieving less than 30-watt system operation in the Power On Suspend sleeping state, and less than 5-watt system operation in the Suspend to Disk sleeping state
- A Soft-off feature that enables the operating system to power off the computer
- Support for multiple wake up events (see Table 50 on page 72)
- Support for a front panel power and sleep mode switch. Table 48 describes the system states based on how long the power switch is pressed, depending on how ACPI is configured with an ACPI-aware operating system

Table 48. Effects of Pressing the Power Switch

If the system is in this state…	…and the power switch is pressed for	…the system enters this state
Off	Less than four seconds	Power on
On	Less than four seconds	Soft off/Suspend
On	More than four seconds	Fail safe power off
Sleep	Less than four seconds	Wake up

3.5.2.1 System States and Power States

Under ACPI, the operating system directs all system and device power state transitions. The operating system puts devices in and out of low-power states based on user preferences and knowledge of how devices are being used by applications. Devices that are not being used can be turned off. The operating system uses information from applications and user settings to put the system as a whole into a low-power state.

Table 49 lists the power states supported by the motherboard along with the associated system power targets. See the ACPI specification for a complete description of the various system and power states.

Table 49. Power States and Targeted System Power

Global States	Sleeping States	CPU States	Device States	Targeted System Power *
G0 - working state	S0 - working	C0 - working	D0 - working state	Full power > 60 W
G1 - sleeping state	S1 - CPU stopped	C1 - stop grant	D1, D2, D3- device specification specific.	5 W < power < 30 W
G2/S5	S5 - Soft off. Context not saved. Cold boot is required.	No power	D3 - no power except for wake up logic.	Power < 5 W **
G3 - mechanical off. AC power is disconnected from the computer.	No power to the system.	No power	D3 - no power for wake up logic, except when provided by battery or external source.	No power to the system so that service can be performed.

* Total system power is dependent on the system configuration, including add-in boards and peripherals powered by the system chassis' power supply.

** Dependent on the standby power consumption of wake-up devices used in the system.

3.5.2.2 Wake Up Devices and Events

Table 50 describes which devices or specific events can wake the computer from specific states. Sleeping states S4BIOS and S5 are the same for the wake up events.

Table 50. Wake Up Devices and Events

These devices/events can wake up the computer…	…from this state
Power switch	S1, S5
RTC alarm	S1, S5
LAN	S5
Modem	S5

3.5.2.3 Plug and Play

In addition to power management, ACPI provides controls and information so that the operating system can facilitate Plug and Play device enumeration and configuration. ACPI is used only to enumerate and configure motherboard devices that do not have other hardware standards for enumeration and configuration. PCI devices on the motherboard, for example, are not enumerated by ACPI.

3.6 BIOS Upgrades

A new version of the BIOS can be upgraded from a diskette using the Intel® Flash Memory Update utility that is available from Intel. This utility supports the following BIOS maintenance functions:

- Update the flash BIOS from a file on a diskette
- Change the language section of the BIOS
- Verify that the upgrade BIOS matches the target system to prevent accidentally installing an incompatible BIOS

BIOS upgrades and the Intel Flash Memory Update utility are available from Intel through the Intel World Wide Web site. See Section 6.1 for information about this site.

NOTE

Please review the instructions distributed with the upgrade utility before attempting a BIOS upgrade.

3.6.1 Language Support

The BIOS Setup program and help messages can be supported in 32 languages. Five languages are available in the BIOS: American English, German, Italian, French, and Spanish. The default language is American English, which is present unless another language is selected in the BIOS Setup program.

The BIOS includes extensions to support the Kanji character set and other non-ASCII character sets. Translations of other languages may become available at a later date.

3.6.2 OEM Logo or Scan Area

A 4 KB flash-memory user area is available for displaying a custom OEM logo during POST. Information about this capability is available on the Intel Support world wide web site. See Section 6.1 for more information about this site.

3.7 Recovering BIOS Data

Some types of failure can destroy the BIOS. For example, the data can be lost if a power outage occurs while the BIOS is being updated in flash memory. The BIOS can be recovered from a diskette using the BIOS recovery mode. When recovering the BIOS, be aware of the following:

- Because of the small amount of code available in the nonerasable boot block area, there is no video support. The procedure can only be monitored by listening to the speaker and looking at the diskette drive LED.
- The recovery process may take several minutes; larger BIOS flash memory devices require more time.
- A single beep indicates the beginning of the BIOS recovery process.
- Two beeps and the end of activity in the diskette drive indicate successful BIOS recovery.
- A series of continuous beeps indicates a failed BIOS recovery.

To create a BIOS recovery diskette, a bootable diskette must be created and the BIOS update files copied to it. BIOS upgrades and the Intel Flash Memory Upgrade utility are available from Intel Customer Support through the Intel World Wide Web site.

NOTE

BIOS Recovery cannot be accomplished using non-SPD DIMMs. SPD data structure is required for the recovery process.

NOTE

If the computer is configured to boot from an LS-120 diskette (in the Removable Devices submenu), the BIOS recovery diskette must be a standard 1.44 MB diskette not a 120 MB diskette.

For information about	Refer to
The BIOS recovery mode	Section 1.14.2, page 51
The Boot menu in the BIOS Setup program	Section 4.7, page 88
Contacting Intel customer support	Section 6.1, page 99

3.8 Boot Options

In the BIOS Setup program, the user can choose to boot from a diskette drive, hard drives, CD-ROM, or the network. The default setting is for the diskette drive to be the primary boot device and the hard drive to be the secondary boot device. By default, the third and fourth devices are disabled.

3.8.1 CD-ROM and Network Boot

Booting from CD-ROM is supported in compliance to the El Torito bootable CD-ROM format specification. Under the Boot menu in the BIOS Setup program, CD-ROM is listed as a boot device. Boot devices are defined in priority order. If the CD-ROM is selected as the boot device, it must be the first device.

The network can be selected as a boot device. This selection allows booting from a network add-in card with a remote boot ROM installed.

For information about	Refer to
The El Torito specification	Section 6.2, page 99

3.8.2 Booting Without Attached Devices

For use in embedded applications, the BIOS has been designed so that after passing the POST, the operating system loader is invoked even if no video adapter, keyboard, or mouse is attached. During POST, the board will beep six times to indicate that no video adapter was detected, but this is not a fatal error.

With regard to standard settings and custom default settings in the BIOS, if custom defaults have been set, the battery has failed, and AC power has failed, custom defaults will be loaded back into CMOS RAM at power on. If no custom defaults have been set, the standard defaults will be loaded back into CMOS RAM at power on.

3.9 USB Legacy Support

USB legacy support enables USB keyboards and mice to be used even when no operating system USB drivers are in place. By default, USB legacy support is disabled. USB legacy support is only intended to be used in accessing the BIOS Setup program and installing an operating system that supports USB.

This sequence describes how USB legacy support operates in the default (disabled) mode.

1. When you power up the computer, USB legacy support is disabled.
2. POST begins.
3. USB legacy support is temporarily enabled by the BIOS. This allows you to use a USB keyboard to enter the BIOS Setup program or the maintenance mode.
4. POST completes and disables USB legacy support (unless it was set to Enabled while in the BIOS Setup program).
5. The operating system loads. While the operating system is loading, USB keyboards and mice are not recognized. After the operating system loads the USB drivers, the USB devices are recognized.

To install an operating system that supports USB, enable USB Legacy support in the BIOS Setup program and follow the operating system's installation instructions. Once the operating system is installed and the USB drivers configured, USB legacy support is no longer used. USB Legacy support can be left enabled in the BIOS Setup program if needed.

Notes on using USB legacy support:

- If USB legacy support is enabled, don't mix USB and PS/2 keyboards and mice. For example, do not use a PS/2 keyboard with a USB mouse, or a USB keyboard and a PS/2 mouse.
- Do not use USB devices with an operating system that does not support USB. USB legacy is not intended to support the use of USB devices in a non-USB aware operating system.
- USB legacy support is for keyboards and mice only. Hubs and other USB devices are not supported.

3.10 BIOS Security Features

The BIOS includes security features that restrict access to the BIOS Setup program and who can boot the computer. A supervisor password and a user password can be set for the BIOS Setup program and for booting the computer, with the following restrictions:

- The supervisor password gives unrestricted access to view and change all the Setup options in the BIOS Setup program. This is supervisor mode.
- The user password gives restricted access to view and change Setup options in the BIOS Setup program. This is user mode.
- If only the supervisor password is set, pressing the <Enter> key at the password prompt of the BIOS Setup program allows the user restricted access to Setup.
- If both the supervisor and user passwords are set, users can enter either the supervisor password or the user password to access Setup. Users have access to Setup respective to which password is entered.
- Setting the user password restricts who can boot the computer. The password prompt will be displayed before the computer is booted. If only the administrator password is set, the computer boots without asking for a password. If both passwords are set, the user can enter either password to boot the computer.

Table 51 shows the effects of setting the supervisor password and user password. This table is for reference only and is not displayed on the screen.

Table 51. Supervisor and User Password Functions

Password Set	Supervisor Mode	User Mode	Setup Options	Password to Enter Setup	Password During Boot
Neither	Can change all options *	Can change all options *	None	None	None
Supervisor only	Can change all options	Can change a limited number of options	Supervisor Password	Supervisor	None
User only	N/A	Can change all options	Enter Password Clear User Password	User	User
Supervisor and user set	Can change all options	Can change a limited number of options	Supervisor Password Enter Password	Supervisor or user	Supervisor or user

* If no password is set, any user can change all Setup options.

See Section 3.10 for information about setting user and supervisor passwords.

4 BIOS Setup Program

What This Chapter Contains

4.1 Introduction

The BIOS Setup program is for viewing and changing the BIOS settings for a computer. The BIOS Setup program is accessed by pressing the <F2> key after the Power-On Self Test (POST) memory test begins and before the operating system boot begins.

Table 52 shows the menus available from the menu bar at the top of the BIOS Setup program screen.

Table 52. BIOS Setup Program Menu Bar

BISO Setup Program Menu Screen	Description
Maintenance	Used for clearing the BIOS Setup program passwords. This menu is only available in configure mode. Refer to Section 1.14.2 on page 51 for information about configure mode.
Main	Allocates resources for hardware components.
Advanced	Specifies advanced features available through the chipset.
Security	Specifies passwords and security features.
Power	Specifies power management features.
Boot	Specifies boot options and power supply controls.
Exit	Saves or discards changes to the BIOS Setup program options.

Table 53 shows the function keys available for menu screens.

Table 53. BIOS Setup Program Function Keys

BIOS Setup Program Function Key	Description
<←> or <→>	Selects a different menu screen
<↑> or <↓>	Moves cursor up or down
<Enter>	Executes command or selects the submenu
<F9>	Load the default configuration values for the current menu
<F10>	Save the current values and exits the BIOS Setup program
<Esc>	Exits the menu
<F1>	Invokes onscreen help

4.2 Maintenance Menu

This menu is for clearing the Setup passwords. Setup only displays this menu in configure mode. See Section 1.14.2 on page 51 for information about setting configure mode.

Table 54. Maintenance Menu

Feature	Options	Description
Clear All Passwords	No options	Clears the user and administrative passwords

4.3 Main Menu

This menu reports processor and memory information and is for configuring the system date and system time.

Table 55. Main Menu

Feature	Options	Description
BIOS Version	No options	Displays the version of the BIOS.
Processor Type	No options	Displays processor type.
Processor Speed	No options	Displays processor speed.
Cache RAM	No options	Displays the size of second-level cache.
Total Memory	No options	Displays the total amount of RAM on the motherboard.
Bank 0 Bank 1	No options	Displays size and type of DIMM installed in each memory bank.
Language	• **English (US) (default)** • German • French • Italian • Spanish	Selects the default language used by the BIOS.
Cache Bus ECC	[N/A]	Cache bus ECC is not supported
Memory Configuration	[Non-ECC]	Not supported. (The Intel 82443ZX PAC does not provide ECC support.)
System Time	Hour, minute, and second	Specifies the current time.
System Date	Month, day, and year	Specifies the current date.

4.4 Advanced Menu

This menu is for setting advanced features that are available through the chipset.

Table 56. Advanced Menu

Feature	Options	Description
Boot Settings Configuration	No options	Configures Plug and Play and the Numlock key, and resets configuration data. When selected, displays the Boot Settings Configuration submenu.
Peripheral Configuration	No options	Configures peripheral ports and devices. When selected, displays the Peripheral Configuration submenu.
IDE Configuration	No options	Specifies type of connected IDE device.
Diskette Configuration	No options	When selected, displays the Floppy Options submenu.
Event Log Configuration	No options	Configures Event Logging. When selected, displays the Event Log Configuration submenu.
Video Configuration	No options	Configures video features. When selected, displays the Video Configuration submenu.
Resource Configuration	No options	Configures memory blocks and IRQs for legacy ISA devices. When selected, displays the Resource Configuration submenu.

4.4.1 Boot Setting Configuration Submenu

This menu is for setting Plug and Play and the Numlock key, and for resetting configuration data.

Table 57. Boot Setting Configuration Submenu

Feature	Options	Description
Plug & Play O/S	**No (default)** Yes	Specifies if a Plug and Play operating system is being used. *No* lets the BIOS configure all devices. *Yes* lets the operating system configure Plug and Play devices. Not required with a Plug and Play operating system.
Reset Config Data	**No (default)** Yes	Clears the BIOS configuration data on the next boot.
Numlock	Off **On (default)**	Specifies the power on state of the Numlock feature on the numeric keypad of the keyboard.

4.4.2 Peripheral Configuration Submenu

This submenu is used for configuring the computer peripherals.

Table 58. Peripheral Configuration Submenu

Feature	Options	Description
Serial port A	• Disabled • Enabled • **Auto (default)**	Configures serial port A. *Auto* assigns the first free COM port, normally COM1, the address 3F8h, and the interrupt IRQ4. An * (asterisk) displayed next to an address indicates a conflict with another device.
Base I/O address	• **3F8 (default)** • 2F8 • 3E8 • 2E8	Specifies the base I/O address for serial port A, if serial port A is Enabled.
Interrupt	• IRQ 3 • **IRQ 4 (default)**	Specifies the interrupt for serial port A, if serial port A is Enabled.
Serial port B	• Disabled • Enabled • **Auto (default)**	Configures serial port B. *Auto* assigns the first free COM port, normally COM2, the address 2F8h and the interrupt IRQ3. An * (asterisk) displayed next to an address indicates a conflict with another device. If either serial port address is set, that address will not appear in the list of options for the other serial port.
Mode	• **Normal (default)** • IrDA SIR-A • ASK_IR	Specifies the mode for serial port B for normal (COM 2) or infrared applications. This option is not available if serial port B has been disabled.
Base I/O address	• 3F8 • **2F8 (default)** • 3E8 • 2E8	Specifies the base I/O address for serial port B.
Interrupt	• **IRQ 3 (default)** • IRQ 4	Specifies the interrupt for serial port B.

continued

Table 58. Peripheral Configuration Submenu (continued)

Feature	Options	Description
Parallel port	• Disabled • Enabled • **Auto (default)**	Configures the parallel port. *Auto* assigns LPT1 the address 378h and the interrupt IRQ7. An * (asterisk) displayed next to an address indicates a conflict with another device.
Mode	• Output Only • **Bi-directional (default)** • EPP • ECP	Selects the mode for the parallel port. Not available if the parallel port is disabled. *Output Only* operates in AT-compatible mode. *Bi-directional* operates in PS/2-compatible mode. *EPP* is Extended Parallel Port mode, a high-speed bi-directional mode. *ECP* is Enhanced Capabilities Port mode, a high-speed bi-directional mode.
Base I/O address	• **378 (default)** • 278 • 228	Specifies the base I/O address for the parallel port.
Interrupt	• **IRQ 5 (default)** • IRQ 7	Specifies the interrupt for the parallel port.
Audio Device	• Disabled • **Enabled (default)**	Enables or disables the onboard audio subsystem.
Legacy USB Support	• Disabled • Enabled • **Auto (default)**	Enables or disables USB legacy support. (See Section 3.9 on page 75 for more information.)

4.4.3 IDE Configuration

Table 59. IDE Device Configuration

Feature	Options	Description
IDE Controller	• Disabled • Primary • Secondary • **Both (default)**	Specifies the integrated IDE controller. *Primary* enables only the Primary IDE Controller. *Secondary* enables only the Secondary IDE Controller. *Both* enables both IDE controllers.
Hard Disk Pre-Delay	• **Disabled (default)** • 3 Seconds • 6 Seconds • 9 Seconds • 12 Seconds • 15 Seconds • 21 Seconds • 30 Seconds	Specifies the hard disk drive pre-delay.
Primary IDE Master	No options	Reports type of connected IDE device. When selected, displays the Primary IDE Master submenu.
Primary IDE Slave	No options	Reports type of connected IDE device. When selected, displays the Primary IDE Slave submenu.
Secondary IDE Master	No options	Reports type of connected IDE device. When selected, displays the Secondary IDE Master submenu.
Secondary IDE Slave	No options	Reports type of connected IDE device. When selected, displays the Secondary IDE Slave submenu.

4.4.4 IDE Configuration Submenus

This submenu is for configuring IDE devices, including:

- Primary IDE master
- Primary IDE slave
- Secondary IDE master
- Secondary IDE slave

Table 60. IDE Configuration Submenus

Feature	Options	Description
Type	• None • User • **Auto (default)** • CD-ROM • ATAPI Removable • Other ATAPI • IDE Removable	Specifies the IDE configuration mode for IDE devices. *User* allows the cylinders, heads, and sectors fields to be changed. *Auto* automatically fills in the values for the cylinders, heads, and sectors fields.
Maximum Capacity	No options	Reports the maximum capacity for the hard disk, if the type is User or Auto.
LBA Mode Control	• Disabled • **Enabled (default)**	Enables or disables the LBA mode control.
Multi-Sector Transfers	• Disabled • **2 Sectors (default)** • 4 Sectors • 8 Sectors • 16 Sectors	Specifies number of sectors per block for transfers from the hard disk drive to memory. Check the hard disk drive's specifications for optimum setting.
Transfer Mode	• Standard • **Fast PIO 1 (default)** • Fast PIO 2 • Fast PIO 3 • Fast PIO 4 • FPIO 3 / DMA 1 • FPIO 4 / DMA 2	Specifies the method for moving data to/from the drive.
Ultra DMA	• **Disabled (default)** • Mode 0 • Mode 1 • Mode 2	Specifies the Ultra DMA mode for the drive.

4.4.5 Diskette Configurations Submenu

This submenu is for configuring the diskette drive.

Table 61. Diskette Configurations Submenu

Feature	Options	Description
Diskette Controller	• Disabled • **Enabled (default)**	Disables or enables the integrated diskette controller.
Diskette A:	• Not Installed • 360 KB, 5¼″ • 1.2 MB, 5¼″ • 720 KB, 3½″ • **1.44/1.25 MB, 3½″ (default)** • 2.88 MB, 3½″	Specifies the capacity and physical size of diskette drive A.
Diskette Write Protect	• **Disabled (default)** • Enabled	Disables or enables write protect for the diskette drive.

4.4.6 Event Log Configuration

This submenu is for configuring the event logging features.

Table 62. Event Log Configuration Submenu

Feature	Options	Description
Event log	No options	Indicates if there is space available in the event log.
Event log validity	No options	Indicates if the contents of the event log are valid.
View event log	[Enter]	Displays the event log.
Clear all event logs	• **No (default)** • Yes	Clears the event log after rebooting.
Event Logging	• Disabled • **Enabled (default)**	Enables logging of Events.
ECC Event Logging	• Disabled • **Enabled (default)**	Enables logging of ECC events.
Mark events as read	[Enter]	Marks all events as read.

4.4.7 Video Configuration Submenu

This submenu is for configuring video features.

Table 63. Video Configuration Submenu

Feature	Options	Description
Palette Snooping	• **Disabled (default)** • Enabled	Controls the ability of a primary PCI graphics controller to share a common palette with an ISA add-in video card.
AGP Aperture Size	• **64 MB (default)** • 256 MB	Specifies the aperture size for the AGP video controller.

4.4.8 Resource Configuration Submenu

This submenu is for configuring the memory and interrupts.

Table 64. Resource Configuration Submenu

Feature	Options	Description
Memory Reservation	• C8000 - CBFFF **Available (default)** | Reserved • CC000- CFFFF **Available (default)** | Reserved • D0000 - D3FFF **Available (default)** | Reserved • D4000 - D7FFF **Available (default)** | Reserved • D8000 - DBFFF **Available (default)** | Reserved • DC000 - DFFFF **Available (default)** | Reserved	Reserves specific upper memory blocks for use by legacy ISA devices.
IRQ Reservation	• IRQ3 **Available (default)** | Reserved • IRQ4 **Available (default)** | Reserved • IRQ5 **Available (default)** | Reserved • IRQ7 **Available (default)** | Reserved • IRQ10 **Available (default)** | Reserved • IRQ11 **Available (default)** | Reserved	Reserves specific IRQs for use by legacy ISA devices. An * (asterisk) displayed next to an IRQ indicates an IRQ conflict.

4.5 Security Menu

This menu is for setting passwords and security features.

Table 65. Security Menu

Feature	Options	Description
User Password Is	No options	Reports if there is a user password set.
Supervisor Password Is	No options	Reports if there is a supervisor password set.
Set User Password	Password can be up to seven alphanumeric characters.	Specifies the user password.
Set Supervisor Password	Password can be up to seven alphanumeric characters.	Specifies the supervisor password.

4.6 Power Menu

This menu is for setting power management features.

Table 66. Power Menu

Feature	Options	Description
Power Management	• Disabled • **Enabled (default)**	Enables or disables the BIOS power management feature.
Inactivity Timer	• Off • 1 Minute • 5 Minutes • 10 Minutes • **20 Minutes (default)** • 30 Minutes • 60 Minutes • 120 Minutes	Specifies the amount of time before the computer enters standby mode.
Hard Drive	• Disabled • **Enabled (default)**	Enables power management for hard disks during standby and suspend modes.
Video Power Down	• Disabled • Standby • **Suspend (default)** • Sleep	Specifies power management for video during standby and suspend modes.

4.7 Boot Menu

This menu is for setting the boot features and the boot sequence.

Table 67. Boot Menu

Feature	Options	Description
Quiet Boot	• Disabled • **Enabled (default)**	*Disabled* displays normal POST messages. *Enabled* displays OEM logo instead of POST messages.
Quick Boot	• Disabled • **Enabled (default)**	Enables the computer to boot without running certain POST tests.
Scan User Flash Area	• **Disabled (default)** • Enabled	Enables the BIOS to scan the flash memory for user binary files that are executed at boot time.
After Power Failure	• Stays Off • **Last State (default)** • Power On	Specifies the mode of operation if an AC/Power loss occurs. *Power On* restores power to the computer. *Stay Off* keeps the power off until the power button is pressed. *Last State* restores the previous power state before power loss occurred.
On Modem Ring	• **Stay Off (default)** • Power On	Specifies how the computer responds to an incoming call on an installed modem when the power is off.
On LAN	• Stay Off • **Power On (default)**	Specifies how the computer responds to a LAN wakeup event when the power is off.
On PME	• **Stay Off (default)** • Power On	Specifies how the computer responds to a PME wakeup event when the power is off.
First Boot Device Second Boot Device Third Boot Device Fourth Boot Device	• Disabled • 1st IDE-HDD (Note 1) • 2nd IDE-HDD • 3rd IDE-HDD • 4th IDE-HDD • Floppy • ARMD-FDD (Note 2) • ARMD-HDD (Note 3) • ATAPI CDROM • SCSI • Network • I2O	Specifies the boot sequence from the available devices. To specify boot sequence: 1. Select the boot device with <↑> or <↓>. 2. Press <Enter> to set the selection as the intended boot device. The operating system assigns a drive letter to each boot device in the order listed. Changing the order of the devices changes the drive lettering. Not all of the devices in this list are available as second, third, and fourth boot devices. The default settings for the first through fourth boot devices are, respectively: • Floppy • 1st IDE-HDD • ATAPI CDROM • Disabled

Notes:

1. HDD = Hard Disk Drive
2. ARMD-FDD = ATAPI removable device - floppy disk drive
3. ARMD-HDD = ATAPI removable device - hard disk drive

4.8 Exit Menu

This menu is for exiting the BIOS Setup program, saving changes, and loading and saving defaults.

Table 68. Exit Menu

Feature	Description
Exit Saving Changes	Exits and saves the changes in CMOS SRAM.
Exit Discarding Changes	Exits without saving any changes made in the BIOS Setup program.
Load Setup Defaults	Loads the factory default values for all the Setup options.
Load Custom Defaults	Loads the custom defaults for Setup options.
Save Custom Defaults	Saves the current values as custom defaults. Normally, the BIOS reads the Setup values from flash memory. If this memory is corrupted, the BIOS reads the custom defaults. If no custom defaults are set, the BIOS reads the factory defaults.
Discard Changes	Discards changes without exiting Setup. The option values present when the computer was turned on are used.

5 Error Messages and Beep Codes

What This Chapter Contains

5.1 BIOS Error Messages

Table 69. BIOS Error Messages

Error Message	Explanation
GA20 Error	An error occurred with Gate-A20 when switching to protected mode during the memory test.
Pri Master HDD Error Pri Slave HDD Error Sec Master HDD Error Sec Slave HDD Error	Could not read sector from corresponding drive.
Pri Master Drive - ATAPI Incompatible Pri Slave Drive - ATAPI Incompatible Sec Master Drive - ATAPI Incompatible Sec Slave Drive - ATAPI Incompatible	Corresponding drive in not an ATAPI device. Run Setup to make sure device is selected correctly.
A: Drive Error B: Drive Error	No response from diskette drive.
Cache Memory Bad	An error occurred when testing L2 cache. Cache memory may be bad.
CMOS Battery Low	The battery may be losing power. Replace the battery soon.
CMOS Display Type Wrong	The display type is different than what has been stored in CMOS. Check Setup to make sure type is correct.
CMOS Checksum Bad	The CMOS checksum is incorrect. CMOS memory may have been corrupted. Run Setup to reset values.
CMOS Settings Wrong	CMOS values are not the same as the last boot. These values have either been corrupted or the battery has failed.
CMOS Date/Time Not Set	The time and/or date values stored in CMOS are invalid. Run Setup to set correct values.
DMA Error	Error during read/write test of DMA controller.
FDC Failure	Error occurred trying to access diskette drive controller.
HDC Failure	Error occurred trying to access hard disk controller.
Checking NVRAM.....	NVRAM is being checked to see if it is valid.
Update OK!	NVRAM was invalid and has been updated.

continued

Table 69. BIOS Error Messages (continued)

Error Message	Explanation
Updated Failed	NVRAM was invalid but was unable to be updated.
Keyboard Is Locked	The system keyboard lock is engaged. The system must be unlocked to continue to boot.
Keyboard Error	Error in the keyboard connection. Make sure keyboard is connected properly.
KB/Interface Error	Keyboard Interface test failed.
Memory Size Decreased	Memory size has decreased since the last boot. If no memory was removed then memory may be bad.
Memory Size Increased	Memory size has increased since the last boot. If no memory was added there may be a problem with the system.
Memory Size Changed	Memory size has changed since the last boot. If no memory was added or removed then memory may be bad.
No Boot Device Available	System did not find a device to boot.
Off Board Parity Error	A parity error occurred on an offboard card. This error is followed by an address.
On Board Parity Error	A parity error occurred in onboard memory. This error is followed by an address.
Parity Error	A parity error occurred in onboard memory at an unknown address.
NVRAM / CMOS / PASSWORD cleared by Jumper	NVRAM, CMOS, and passwords have been cleared. The system should be powered down and the jumper removed.
<CTRL_N> Pressed	CMOS is ignored and NVRAM is cleared. User must enter Setup.

5.2 Port 80h POST Codes

During the POST, the BIOS generates diagnostic progress codes (POST codes) to I/O port 80h. If the POST fails, execution stops and the last POST code generated is left at port 80h. This code is useful for determining the point where an error occurred.

Displaying the POST codes requires an add-in card (often called a POST card). The POST card can decode the port and display the contents on a medium such as a seven-segment display. These cards can be purchased from JDR Microdevices or other sources.

The following tables provides the POST codes that can be generated by the BIOS. Some codes are repeated in the table because that code applies to more than one operation.

Table 70. Uncompressed INIT Code Checkpoints

Code	Description of POST Operation
D0	NMI is Disabled. Onboard KBC, RTC enabled (if present). Init code Checksum verification starting.
D1	Keyboard controller BAT test, CPU ID saved, and going to 4GB flat mode.
D3	Do necessary chipset initialization, start memory refresh, do Memory sizing.
D4	Verify base memory.
D5	Init code to be copied to segment 0 and control to be transferred to segment 0.
D6	Control is in segment 0. To check recovery mode and verify main BIOS checksum. If either it is recovery mode or main BIOS checksum is bad, go to check point E0 for recovery else go to check point D7 for giving control to main BIOS.
D7	Find Main BIOS module in ROM image.
D8	Uncompress the main BIOS module.
D9	Copy main BIOS image to F000 shadow RAM and give control to main BIOS in F000 shadow RAM.

Table 71. Boot Block Recovery Code Check Points

Code	Description of POST Operation
E0	Onboard Floppy Controller (if any) is initialized. Compressed recovery code is uncompressed in F000:0000 in Shadow RAM and give control to recovery code in F000 Shadow RAM. Initialize interrupt vector tables, initialize system timer, initialize DMA controller, interrupt controller.
E8	Initialize extra (Intel Recovery) Module.
E9	Initialize floppy drive.
EA	Try to boot from floppy. If reading of boot sector is successful, give control to boot sector code.
EB	Booting from floppy failed, look for ATAPI (LS120, Zip) devices.
EC	Try to boot from ATAPI. If reading of boot sector is successful, give control to boot sector code.
EF	Booting from floppy and ATAPI device failed. Give two beeps. Retry the booting procedure again (go to check point E9).

Table 72. Runtime Code Uncompressed in F000 Shadow RAM

Code	Description of POST Operation
03	NMI is Disabled. To check soft reset/power-on.
05	BIOS stack set. Going to disable Cache if any.
06	POST code to be uncompressed.
07	CPU init and CPU data area init to be done.
08	CMOS checksum calculation to be done next.
0B	Any initialization before keyboard BAT to be done next.
0C	KB controller I/B free. To issue the BAT command to keyboard controller.
0E	Any initialization after KB controller BAT to be done next.
0F	Keyboard command byte to be written.
10	Going to issue Pin-23,24 blocking/unblocking command.
11	Going to check pressing of <INS>, <END> key during power-on.
12	To init CMOS if "Init CMOS in every boot" is set or <END> key is pressed. Going to disable DMA and Interrupt controllers.
13	Video display is disabled and port-B is initialized. Chipset init about to begin.
14	8254 timer test about to start.
19	About to start memory refresh test.
1A	Memory Refresh line is toggling. Going to check 15µs ON/OFF time.
23	To read 8042 input port and disable Megakey GreenPC feature. Make BIOS code segment writeable.
24	To do any setup before Int vector init.
25	Interrupt vector initialization to begin. To clear password if necessary.
27	Any initialization before setting video mode to be done.
28	Going for monochrome mode and color mode setting.
2A	Different buses init (system, static, output devices) to start if present. (See Section 5.3 for details of different buses.)
2B	To give control for any setup required before optional video ROM check.
2C	To look for optional video ROM and give control.
2D	To give control to do any processing after video ROM returns control.
2E	If EGA/VGA not found then do display memory R/W test.
2F	EGA/VGA not found. Display memory R/W test about to begin.
30	Display memory R/W test passed. About to look for the retrace checking.
31	Display memory R/W test or retrace checking failed. To do alternate Display memory R/W test.
32	Alternate Display memory R/W test passed. To look for the alternate display retrace checking.
34	Video display checking over. Display mode to be set next.
37	Display mode set. Going to display the power on message.
38	Different buses init (input, IPL, general devices) to start if present. (See Section 5.3 for details of different buses.)
39	Display different buses initialization error messages. (See Section 5.3 for details of different buses.)
3A	New cursor position read and saved. To display the Hit <DEL> message.

continued

Table 72. Runtime Code Uncompressed in F000 Shadow RAM (continued)

Code	Description of POST Operation
40	To prepare the descriptor tables.
42	To enter in virtual mode for memory test.
43	To enable interrupts for diagnostics mode.
44	To initialize data to check memory wrap around at 0:0.
45	Data initialized. Going to check for memory wrap around at 0:0 and finding the total system memory size.
46	Memory wrap around test done. Memory size calculation over. About to go for writing patterns to test memory.
47	Pattern to be tested written in extended memory. Going to write patterns in base 640k memory.
48	Patterns written in base memory. Going to find out amount of memory below 1M memory.
49	Amount of memory below 1M found and verified. Going to find out amount of memory above 1M memory.
4B	Amount of memory above 1M found and verified. Check for soft reset and going to clear memory below 1M for soft reset. (If power on, go to check point # 4Eh).
4C	Memory below 1M cleared. (SOFT RESET) Going to clear memory above 1M.
4D	Memory above 1M cleared. (SOFT RESET) Going to save the memory size. (Go to check point # 52h).
4E	Memory test started. (NOT SOFT RESET) About to display the first 64k memory size.
4F	Memory size display started. This will be updated during memory test. Going for sequential and random memory test.
50	Memory testing/initialization below 1M complete. Going to adjust displayed memory size for relocation/ shadow.
51	Memory size display adjusted due to relocation/ shadow. Memory test above 1M to follow.
52	Memory testing/initialization above 1M complete. Going to save memory size information.
53	Memory size information is saved. CPU registers are saved. Going to enter in real mode.
54	Shutdown successful, CPU in real mode. Going to disable gate A20 line and disable parity/NMI.
57	A20 address line, parity/NMI disable successful. Going to adjust memory size depending on relocation/shadow.
58	Memory size adjusted for relocation/shadow. Going to clear Hit <DEL> message.
59	Hit <DEL> message cleared. <WAIT...> message displayed. About to start DMA and interrupt controller test.
60	DMA page register test passed. To do DMA#1 base register test.
62	DMA#1 base register test passed. To do DMA#2 base register test.
65	DMA#2 base register test passed. To program DMA unit 1 and 2.
66	DMA unit 1 and 2 programming over. To initialize 8259 interrupt controller.
7F	Extended NMI sources enabling is in progress.
80	Keyboard test started. Clearing output buffer, checking for stuck key, to issue keyboard reset command.
81	Keyboard reset error/stuck key found. To issue keyboard controller interface test command.
82	Keyboard controller interface test over. To write command byte and init circular buffer.
83	Command byte written, global data init done. To check for lock-key.

continued

Table 72. Runtime Code Uncompressed in F000 Shadow RAM (continued)

Code	Description of POST Operation
84	Lock-key checking over. To check for memory size mismatch with CMOS.
85	Memory size check done. To display soft error and check for password or bypass setup.
86	Password checked. About to do programming before setup.
87	Programming before setup complete. To uncompress SETUP code and execute CMOS setup.
88	Returned from CMOS setup program and screen is cleared. About to do programming after setup.
89	Programming after setup complete. Going to display power on screen message.
8B	First screen message displayed. <WAIT...> message displayed. PS/2 Mouse check and extended BIOS data area allocation to be done.
8C	Setup options programming after CMOS setup about to start.
8D	Going for hard disk controller reset.
8F	Hard disk controller reset done. Floppy setup to be done next.
91	Floppy setup complete. Hard disk setup to be done next.
95	Init of different buses optional ROMs from C800 to start. (See Section 5.3 for details of different buses.)
96	Going to do any init before C800 optional ROM control.
97	Any init before C800 optional ROM control is over. Optional ROM check and control will be done next.
98	Optional ROM control is done. About to give control to do any required processing after optional ROM returns control and enable external cache.
99	Any initialization required after optional ROM test over. Going to setup timer data area and printer base address.
9A	Return after setting timer and printer base address. Going to set the RS-232 base address.
9B	Returned after RS-232 base address. Going to do any initialization before Coprocessor test.
9C	Required initialization before Coprocessor is over. Going to initialize the Coprocessor next.
9D	Coprocessor initialized. Going to do any initialization after Coprocessor test.
9E	Initialization after Coprocessor test is complete. Going to check extended keyboard, keyboard ID and num-lock.
A2	Going to display any soft errors.
A3	Soft error display complete. Going to set keyboard typematic rate.
A4	Keyboard typematic rate set. To program memory wait states.
A5	Going to enable parity/NMI.
A7	NMI and parity enabled. Going to do any initialization required before giving control to optional ROM at E000.
A8	Initialization before E000 ROM control over. E000 ROM to get control next.
A9	Returned from E000 ROM control. Going to do any initialization required after E000 optional ROM control.
AA	Initialization after E000 optional ROM control is over. Going to display the system configuration.
AB	Put INT13 module runtime image to shadow.
AC	Generate MP for multiprocessor support (if present).
AD	Put CGA INT10 module (if present) in Shadow.

continued

Table 72. Runtime Code Uncompressed in F000 Shadow RAM (continued)

AE	Uncompress SMBIOS module and init SMBIOS code and form the runtime SMBIOS image in shadow.
B1	Going to copy any code to specific area.
00	Copying of code to specific area done. Going to give control to INT-19 boot loader.

5.3 Bus Initialization Checkpoints

The system BIOS gives control to the different buses at the following checkpoints to do various tasks.

Checkpoint	Description
2A	Different buses init (system, static, output devices) to start if present.
38	Different buses init (input, IPL, general devices) to start if present.
39	Display different buses initialization error messages.
95	Init of different buses optional ROMs from C800 to start.

While control is inside the different bus routines, additional checkpoints are output to port 80h as WORD to identify the routines under execution. In these WORD checkpoints, the low byte of the checkpoint is the system BIOS checkpoint from which the control is passed to the different bus routines. The high byte of the checkpoint is the indication of which routine is being executed in the different buses. The upper nibble of the high byte indicates the function that is being executed:

Value	Description
0	func#0, disable all devices on the bus concerned.
1	func#1, static devices init on the bus concerned.
2	func#2, output device init on the bus concerned.
3	func#3, input device init on the bus concerned.
4	func#4, IPL device init on the bus concerned.
5	func#5, general device init on the bus concerned.
6	func#6, error reporting for the bus concerned.
7	func#7, add-on ROM init for all buses.

The lower nibble of the high byte indicates the bus on which the routines are being executed:

Value	Description
0	Generic DIM (Device Initialization Manager).
1	On-board System devices.
2	ISA devices.
3	EISA devices.
4	ISA PnP devices.
5	PCI devices.

5.4 BIOS Beep Codes

Whenever a recoverable error occurs during power-on self test (POST), the BIOS displays an error message describing the problem. The BIOS also issues a beep code (one long tone followed by two short tones) during POST if the video configuration fails (a faulty video card or no card installed) or if an external ROM module does not properly checksum to zero.

An external ROM module (for example, a video BIOS) can also issue audible errors, usually consisting of one long tone followed by a series of short tones. For more information on the beep codes issued, check the documentation for that external device.

There are several POST routines that issue a POST terminal error and shut down the system if they fail. Before shutting down the system, the terminal-error handler issues a beep code signifying the test point error, writes the error to I/O port 80h, attempts to initialize the video and writes the error in the upper left corner of the screen (using both monochrome and color adapters).

If POST completes normally, the BIOS issues one short beep before passing control to the operating system.

Table 73. Beep Codes

Beep	Description
1	Refresh failure
2	Parity can not be reset
3	First 64k memory failure
4	Timer not operational
5	Processor failure (Reserved for historic reason, not used any more)
6	8042 GateA20 can not toggled
7	Exception interrupt error
8	Display memory R/W error
9	ROM checksum error (Reserved for historic reason, not used any more)
10	CMOS Shutdown register test error
11	Invalid BIOS (e.g. POST module not found, etc.)

6 Specifications and Customer Support

What This Chapter Contains

6.1 Online Support

Find information about Intel motherboards under “Product Info” or “Customer Support” at these World Wide Web sites:

http://www.intel.com/design/motherbd
http://support.intel.com/support/motherboards/desktop

6.2 Specifications

The motherboard complies with the following specifications:

Table 74. Specifications

Specification	Description	Revision Level
AC ‘97	Audio Codec ‘97	Revision 2.1, May 1998, Intel Corporation ftp://download.intel.com/pc-supp/platform/ac97
AGP	Accelerated Graphics Port Interface Specification	Revision 1.0, August, 1996, Intel Corporation. The specification is available through the Accelerated Graphics Implementers Forum at: http://www.agpforum.org/
ACPI	Advanced Configuration and Power Interface specification	Revision 1.0a, December 22, 1996 Intel Corporation, Microsoft Corporation, and Toshiba Corporation http://www.agpforum.org
AMI BIOS	American Megatrends	AMIBIOS 98 www.amibios.com
APM	Advanced Power Management BIOS interface specification	Revision 1.2, February, 1996 Intel Corporation, Microsoft Corporation
ATA-3	Information Technology - AT Attachment-3 Interface	X3T10/2008D Revision 6 ATA Anonymous FTP Site: fission.dt.wdc.com
ATAPI	ATA Packet Interface for CD-ROMs	SFF-8020i Revision 2.5 (SFF) Fax Access: (408) 741-1600
ATX	ATX Specification	Revision 2.01, February 1997, Intel Corporation http://developer.intel.com/design/motherbd.atx.htm

continued

Table 74. Specifications (continued)

Specification	Description	Revision Level
El Torito	Bootable CD-ROM format specification	Version 1.0, January 25, 1995 Phoenix Technologies Ltd., IBM Corporation. The El Torito specification is available on the Phoenix Web site http://www.ptltd.com/techs/specs.html
EPP	Enhanced Parallel Port	IEEE 1284 standard, Mode [1 or 2], v1.7
IrDA	Serial Infrared Physical Layer Link specification	Version 1.1, October 17, 1995 Infrared Data Association. Phone: (510) 943-6546 Fax: (510) 943-5600 E-mail: irda@netcom.com
microATX	microATX Motherboard Interface Specification SFX Power Supply Design Guide	Version 1.0, December, 1997 Intel Corporation Version 1.0, December, 1997 Intel Corporation
PCI	PCI Local Bus specification	Revision 2.1, June 1, 1995, PCI Special Interest Group http://www.pcisig.com/
Plug and Play	Plug and Play BIOS specification	Version 1.0a, May 5, 1994 Compaq Computer Corporation, Phoenix Technologies Ltd., Intel Corporation
SDRAM DIMMs (64-and 72-bit)	PC SDRAM Unbuffered DIMM specification PC SDRAM DIMM Specification PC Serial Presence Detect (SPD) Specification	Revision 1.0, February, 1998, Intel Corporation Revision 1.5, November, 1997, Intel Corporation Revision 1.2A, December, 1997
SMBIOS	System Management BIOS	Version 2.3, 12 August 1998 Award Software International Inc., Dell Computer Corporation, Hewlett-Packard Company, Intel Corporation, International Business Machines Corporation, Phoenix Technologies Limited, American Megatrends Inc., and SystemSoft Corporation. http://developer.intel.com/ial/wfm/design/smbios
UHCI	Universal Host Controller Interface	Design Guide Revision 1.1, March 1996 Intel Corporation. The specification is available at: http://www.usb.org/developers
USB	Universal serial bus specification	Revision 1.0, January 15, 1996 Compaq Computer Corporation, Digital Equipment Corporation, IBM PC Company, Intel Corporation, Microsoft Corporation, NEC, Northern Telecom http://usb.org/developers