BYTE INPUT-OUTPUT MODULE

Description

This is a general purpose fully buffered interface module, for reading and writing bytes of data to a byte orientated device.

The module provides:

8 data output lines, each with a storage flip flop. The data lines may be updated by executing a 'Write Data' instruction.

8 data input lines, which may be read in by executing a 'Read Data' instruction.

8 control lines, each with a storage flip flop, which may be updated by executing an 'Output Command' instruction.

8 sense lines whose status may be read by executing a 'Sense Status' or an 'Acknowledge Interrupt' instruction.

1 Priority Interrupt line, which when acknowledged by an 'Acknowledge Interrupt' instruction, automatically transfers the device number of the module to the general register specified by the 'Acknowledge Interrupt' instruction.

1 Interrupt Acknowledge line to the device to let it know that an int. has been acknowledged.

Interface Specifications:

Output Signals

Logical zero is 0V ± 0.5V at 12mA
Logical one is 5V ± 0.5V at 0.5mA
Acknowledge Interrupt pulse width 1.0μS

Input Signals

Logical zero is 0V ± 0.5V at 1.2mA
Logical one is 5V ± 2V at 0.0 mA
The interrupt line requires a positive going input pulse of at least 0.5μS width up to a D.C. level

Programming Notes

1. Strap options allow for any device number up to 256.
2. Data can be transferred to the module by Write Data (WD) instructions:
   WD R1, R2 OR ITS RX/RS FORM.

GENERAL ELECTRIC

70A110025

PROJECT DIR.: K7-12	INFORMATION SPECIFICATION BYTE INPUT-OUTPUT MODULE	CONT. ON 1 SH. NO. 0 (32-023A12)

GENERAL NOTES

F.C.F.
FMF:

APPROVED BY: E. G. White DATE: 9-10 69

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME
A	ISSUE				
A1	REVISED SHS 0, 1,2,3,	P. MILLER			
	PER				
	AN 67DW-44-012	Nov 21, '69			
A2	REV SHS PER	Follmuth			
	A1-097	JULY 21, 1971			

REISSUED

A	Issue										
A1	Dec 10, '69										
A2	Jul 29, 71										

Made By	Issue Date	PROCESS COMPUTER PHOENIX, ARIZ.	Dwg. No. 70A110025 Cont. on 1	Sh. No. 0
E. WHITE	Sept 15, 1969			

PCR 20A 7-62

3. Commands can be transmitted to the module by Output Command (OC) instructions.

OC R1, R2 Or Its RX/RS form

4. The device, in turn, has 8 bits of data and 8 bits of status brought in to the module via a cable. This data and status can be transferred to the Processor by Read Data (RD) and Sense Status (SS) instructions:

RD Dev #, R1 (Data transfer)
SS Dev #, R2 (Status transfer)

Mechanical Considerations

1. The Byte I/O Module, consists of:

1 ea. Byte I/O Module	Part #32-023
3 ea. General Purpose I/O Cable	Part #17-069 F04
1 ea. Schematic	FS 9
1 ea. Test Program	70A112471

2. The interface board may be inserted into any available I/O slot.

3. Cables must be connected as per figures 1 and 2.

FIGURE 1

NAME	STRAP BOARD LOCATION	NAME	STRAP BOARD LOCATION
DIN01	10 - 42	DOUT01	10 - 41
11	20	11	20
21	30	21	30
31	40	31	40
41	50	41	50
51	60	51	60
61	70	61	70
DIN71	11 - 42	DOUT71	11 - 41
SIN01	31 - 41	COUT01	10 - 40
11	41	11	20
21	51	21	30
31	61 - 41	31	40
41	31 - 42	41	50
51	41 - 42	51	60
61	51 - 42	61	70
SIN71	61 - 42	COUT71	11 - 40

FIGURE 2

NAME	LOCATION
RDR1	51 - 40
RDT1	61 - 40
WDT1	41 - 40
OCT1	71 - 40
INT	21 - 40
IACK1	31 - 40

GENERAL ELECTRIC

70A111091

PRINT DIST.: K7-21

BYTE I/O MODULE
MAINTENANCE SPECIFICATION

CONT. ON 1 SH. NO. 0

(02-058A21)

GENERAL NOTES

F.C.F.

FMF: GE-PAC 30

APPROVED BY: E. A. White DATE: Oct 27, 69

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME
A	ISSUE				

REISSUED

Issue					

Made By: E. WHITE

Issue Date: Oct 29, 1969

PROCESS COMPUTER PHOENIX, ARIZ.

Dwg. No. 70A111091 Cont. on 1 Sh. No. 0

REV NO.

CONT ON SHEET SH NO.

TITLE

BYTE I/O MODULE
MAINTENANCE SPECIFICATION

FIRST MADE FOR GE-PAC 30 (02-058A21)

REVISIONS

TABLE OF CONTENTS

PRINTS TO

1. INTRODUCTION

The Byte I/O Module, Part Number 02-058, is a general purpose interface which is used in conjunction with a byte oriented device. There are sixteen stored output lines to the device, and sixteen nonstored input lines from the device. The Command/Status philosophy is not defined for this product; it is defined as per individual device requirements.

2. SCOPE

This document describes the Byte I/O Interface-mother-board, Part Number 32-023. Schematics for the Byte I/O Module are provided on FS9.

3. BLOCK DIAGRAM ANALYSIS

The Byte I/O Interface is a general purpose communication link between the Processor I/O Multiplexor (MPX) Bus and a Byte oriented device. Refer to Figure 1. If the device is addressed, the command and data bytes from the MPX bus are stored into two registers. The outputs from these registers are brought out to the peripheral device to be used as required (one control byte, and one data byte). The data and status bytes from the peripheral device are brought into the interface for interrogation by the Processor.

An interrupt line is provided such that if the peripheral device required service, this line could be activated to generate an I/O interrupt.

All control gated lines, including the interrupt acknowledge line, are available for peripheral device use, with the exception of the status gated line (SST).

4. FUNCTIONAL DIAGRAM ANALYSIS

4.1 Addressing

In order for data transfer to take place between the Multiplexor I/O Bus and the device, the interface must first be addressed with a pre-selected address; the interface will respond only to this address.

The Data Available Lines (DAL's) are activated with the code for the Byte I/O device address. These lines go through single-to- double rail converters (FS9-1); both the true and false outputs from these converters appear

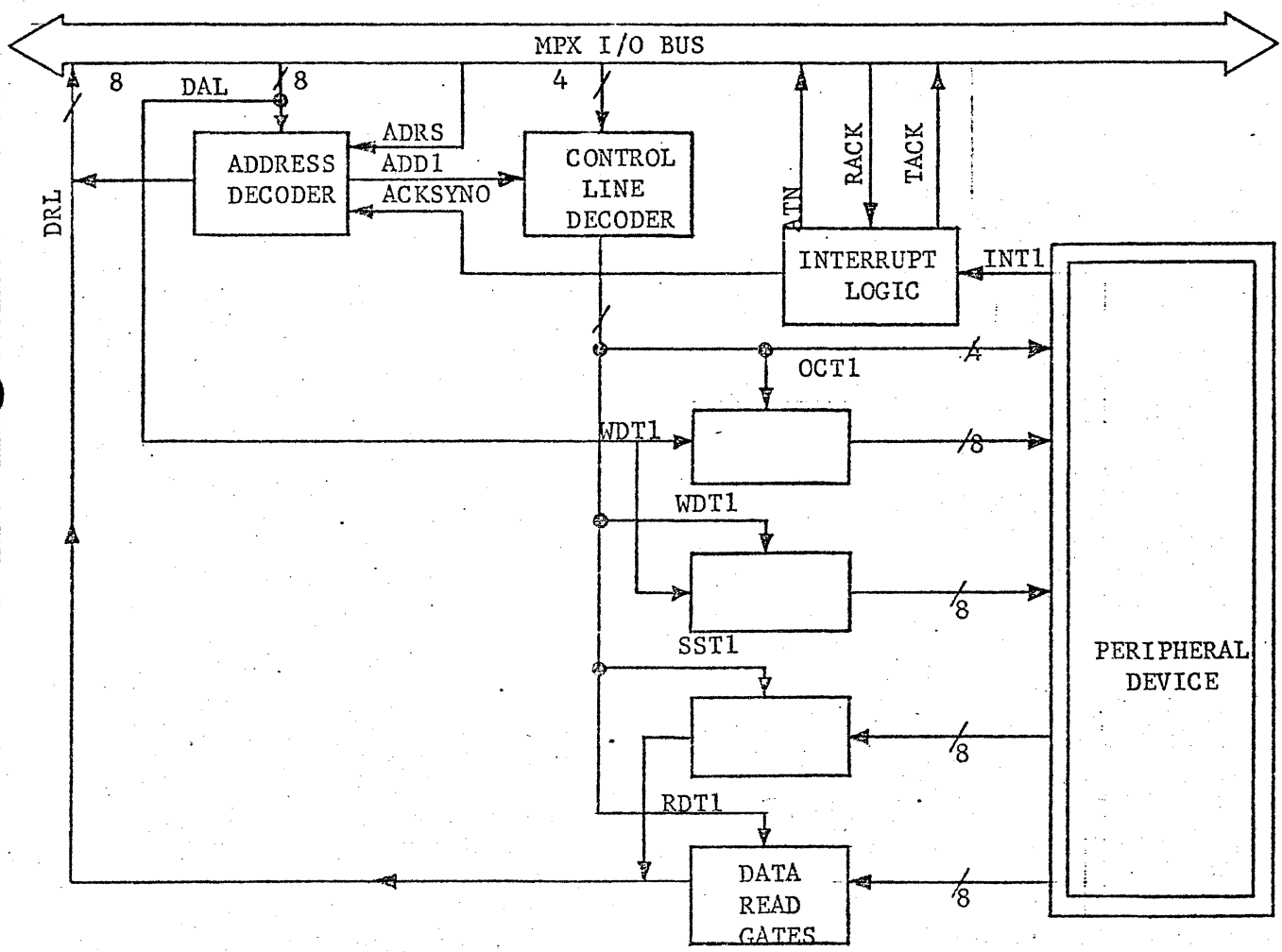

FIGURE 1. Byte I/O Block Diagram

at the input of two 35-038 strap boards. These strap boards are wired such that the DNLX,1 lines will all be high if the proper address is present on the DAL lines. If this is the case, the output from the 35-022 board (1M5) goes low, and is inverted to become DEV,1 (Device Address). If these DAL lines reflect an address, the ADRS,0 control line is activated (2A1). This line is inverted and ANDed with DEV,1 to either set or reset the Address flip-flop depending on whether DEV,1 is high (addressed) or low (not addressed). The resulting AND of the addressed condition is used to send a SYN back to the Processor. The Processor responds to the SYN by deactivating the ADRS,0 control line causing the SYN to drop. The device is now ready for data transfer.

4.2 Writing

With the Address flip-flop set, data is transferred to the interface by first activating the DAL lines and, after settling time, activating the DAO control line. The DA,0 control line is inverted and ANDed with the Address flip-flop (FS9-2). If the Address flip-flop is set, the resultant AND generates a SYN back to the Processor, and is inverted to become WDT,1. The WDT,1 line going high gates the state of the DAL lines into the DATA Register (FS9-5). The return of the SYN to the Processor causes the Processor to deactivate the DA control line. This drops the SYN and the WDT,1. The data remains stored in the register until the next Write Data operation.

The data from the register is buffered and brought out to the peripheral device as DOUTX (high=active) lines.

4.3 Reading

The DR (Data Request) control line is activated by the Processor. It is then inverted and ANDed with the Address flip-flop and RDR,1* (external read control line) -FS9-2. If the device is addressed - Address flip-flop set - and RDR,1 is high, the resultant AND sends back a SYN to the Processor and is inverted to become RDT,1 (FS9-2R4). The RDT,1 signal gates the data inputs from the peripheral device onto the DRL Bus. The SYN return to the Processor causes the Processor to deactivate the DR control line. This will, in turn, shut off the SYN and deactivate the RDT,1, removing the state of the DINX lines from the DRL Bus.

*RDR,1 is an external Read Control Line; this line is used to delay the SYN in case the peripheral device is not ready to transfer data to the interface.

4.4 Status Request

The Processor activate the SR (Status Request) control line. This line is inverted and ANDed with the Address flip-flop (FS9-2). If the Address flip-flop is set (addressed condition), the resultand AND sends back a SYN to the Processor, and is inverted to become SST,1. The SST,1 line gates back the state of the Device Status (SINX,1) lines onto the DRL Bus. The return of the SYN causes the Processor to deactivate the SR control line. This drops the SYN and deactivates the SST1 line, removing the status from the DRL Bus.

4.5 Output Command

The command structure is presented on the DAL lines. After the DAL lines settle, the CMD,0 control line is activated. This line is inverted and ANDed with the Address flip-flop (FS9-2). If the Address flip-flop is set (addressed condition), the resulting AND sends a SYN back to the Processor, and is inverted to become OCT,1. The rising edge of the OCT,1 line sets the state of the DAL lines into the Command Register (FS9-6). The return of the SYN causes the Processor to deactivate the CMD,0 control line. This shuts off the SYN and deactivates the OCT,1 line. The image of the DAL lines is retained in the Command Register. The output from the register is buffered and appears on the connector board (COUTX,1) for external use.

4.6 Interrupt Acknowledge (FS9-3)

The interrupt is caused by a transistion from the ZERO to the ONE state of the INT,1 line. The output from the Interrupt flip-flop is inverted and tied onto the Attention Bus (ATN,0). The ATN,0 line going low causes an I/O interrupt. The Processor will sometime later service the interrupt. It will do this by activating the RACK line. In the Interface, this line will be inverted to become RACK,1.

In order to describe the acknowledge circuit, two cases will be used:

Case 1 - Attention flip-flop set

With the Attention flip-flop set, ATN,1 is high. RACK,1 is normally low, causing the output 61-07 (TACK,0) to be high. TACK,0 is ANDed with ATN,1. Since they are both high, the output 21-07 is low. This locks TACK,0 in the high state. The Processor activates RACK,0 causing RACK,1 to go high. RACK,1 is ANDed with TACK,0. This causes ACKSYN0,0 to go low and its inverted state, IACK,1, to go high. ACKSYN,0 sends back a SYN to the Processor (FS-2) and activates the DNLX,1 lines to reflect the address code of the device. IACK,1, is ANDed with the DNLX,1 lines causing the result to be tied onto the DRL Bus. The return of the SYN causes the Processor to deactivate the RACK,0 line. This deactivates the SYN, ACKSYN,0 and IACK,1 lines. The deactivation of the ACKSYN,0 line removes the SYN from the bus. The deactivation of the IACK,1 removes the Device Address from the DRL Bus, and causes the Attention flip-flop to reset.

Case 2 - Attention flip flop reset (no interrupt)

With the Attention flip-flop reset, the ATN,1 line is low. This causes the output 21-07 to be high. If the Processor activates RACK,0, RACK,1 will go high. RACK,1 is then ANDed with the output 21-07. This causes TACK,0 to go low, transmitting the Receive Acknowledge to the next I/O device. If the ATN,1 line should go high while RACK,1 is still high, it is locked out because TACK,0 is low.

5. TROUBLESHOOTING

If a malfunction occurs in the Byte I/O controller, the trouble can be isolated by use of the test program as described in Programming Manual PCP129.

6. MNEMONICS

This section provides an alphabetical list of the mnemonics used in the Byte I/O Module. A brief description of each mnemonic, and a reference to its source on the schematic, FS9, are also provided.

MNEMONIC	MEANING	SCHEMATIC LOCATION
ACKSYN	Acknowledge interrupt SYN	1A5
ADRS	Address Control Line	2A1
ATN	Attention Line	3F9
CMD	Command Control Line	2A7
COUTXX	Command Output Lines	6G9
DA	Data Available Control Line	2A5
DALXX	Data Available Lines	1
DEV	Device Addressed Match	1R5
DINXX	Data Input Lines	4G1
DNLXX	Device Name Lines	1
DOUTXX	Data Output Lines	5G9
DR	Data Request Control Line	2A4
DRLXX	Data Receive Lines	3M9
IACK	Interrupt Acknowledge Gate	3A2
INT	Interrupt Line	3A2
OCT	Output Command Gate	2R7
RACK	Receive Acknowledge	3A7
RDR	Read Ready	2B4
RDT	Read Data Gated	2R4
SCLR	System Clear	2A8
SINXX	Status Input Lines	4G5

MNEMONIC	MEANING	SCHEMATIC LOCATION
SR	Status Request Control Line	2A5
SST	Sense Status Gate	2R6
SYN	Sync	2R3
TACK	Transmit Acknowledge	3A4
WDT	Write Data Gated	2R5

GENERAL ELECTRIC

70A111162

PRINT DIST.	BYTE I/O MODULE	CONT. ON 1 SH. NO. 0
K7-20	INSTALLATION SPECIFICATION	(02-056A20)

GENERAL NOTES

F.C.F.

FMF: GE-PAC 30

APPROVED BY: E A. White DATE: March 16, 70

REVISION STATUS

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Made By	Issue Date	PROCESS	Dwg. No. 70A111162
E WHITE, MARCH 10, 1970	Mon M 1970	COMPUTER PHOENIX, ARIZ.	Cont. on 1 Sh. No 0

PGE REV. 2-62

TITLE BYTE I/O MODULE
INSTALLATION SPECIFICATION

FIRST MADE FOR GE-PAC 30 (02-058A20)

REVISIONS

1. UNPACKING

When this module is shipped with a Processor, there are no special unpacking procedures. However, if the Byte I/O Module is shipped as part of an expansion unit, unpack it carefully and check for breakage and damage to components.

2. PHYSICAL CHARACTERISTICS

This module consists of a standard 9-3/4 inch by 10-1/2 inch mother-board and three 17-069F04 cables.

3. LOCATION

The mother-board connects to any I/O slot on the Processor or expansion chassis. The BACK0/TACK0 strap must be removed from the I/O slot (114-0 to 214-0).

4. SAFEGUARDS

To prevent damage to personnel and equipment, make sure the AC power is off while installing the module.

5. CABLES

The 17-069F04 cables are connected as shown in Table 1 and Table 2.

6. DEVICE ADDRESSING

The device address of this module is X'0B'. This address can be changed by changing the strapping on two 35-038 strap boards as shown in Figure 1 and in Table 3.

For X'0B', pins numbered 61, 31, 60, and 30 are connected directly to the Address NAND gate. Pins numbered 71, 41, 70, and 40 are the address line 1-side. Pins numbered 51, 21, 50, and 20 are the address line 0-side. (See Figure 1).

7. INSTALLATION CHECK

Run Test Program 7CA112471 to determine if the Byte I/O Module has been installed correctly and is running properly.

PRINTS TO

TABLE 1. CABLE LOCATION

NAME	STRAP BOARD LOCATION		NAME	STRAP BOARD LOCATION	
DIN01	10	42	DOUT01	10	41
DIN11	20	42	DOUT11	20	41
DIN21	30	42	DOUT21	30	41
DIN31	40	42	DOUT31	40	41
DIN41	50	52	DOUT41	50	41
DIN51	60	42	DOUT51	60	41
DIN61	70	42	DOUT61	70	41
DIN71	11	42	DOUT71	11	41
SIN01	31	41	COUT01	10	40
SIN11	41	41	COUT11	20	40
SIN21	51	41	COUT21	30	40
SIN31	61	41	COUT31	40	40
SIN41	31	42	COUT41	50	40
SIN51	41	42	COUT51	60	40
SIN61	51	42	COUT61	70	40
SIN71	61	42	COUT71	11	40

NOTE

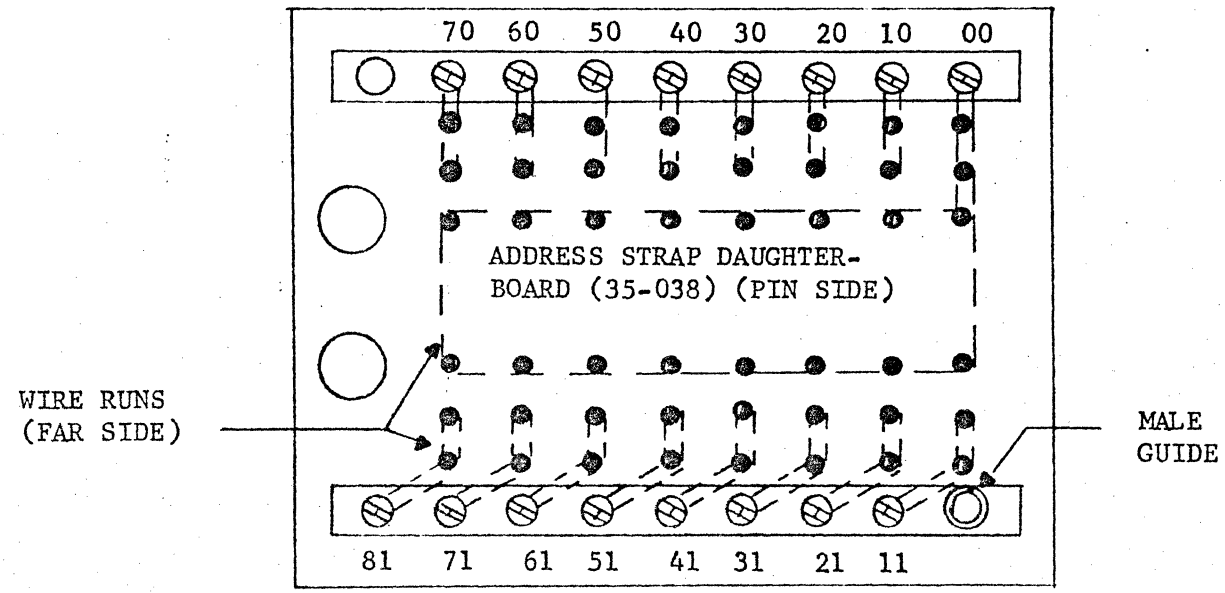
If the device address is changed, the test program must also change.

TABLE 2. CABLE SIGNALS AND LOCATIONS

NAME	LOCATION
RDR1	51-40
RDT1	61-40
WDT1	41-40
OCT1	71-40
INT	21-40
IACK1	31-40

Figure 1 Strap Daughter Board Device Addressing

D.B. LOC	PIN NUMBER	LEVEL	HEXADECIMAL WEIGHT	EXAMPLES OF DEVICE ADDRESSING X'14C:	X'12B'
02	61 - - - - - 71 - - - - - 51	1 0	8	61 TO 51	61 TO 51
	31 - - - - - 41 - - - - - 21	1 0	4	31 TO 41	31 TO 21
	60 - - - - - 70 - - - - - 50	1 0	2	60 TO 50	60 TO 70
	30 - - - - - 40 - - - - - 20	1 0	1	30 TO 20	30 TO 20
03	61 - - - - - 71 - - - - - 51	1 0	8	61 TO 71	61 TO 71
	31 - - - - - 41 - - - - - 21	1 0	4	31 TO 41	31 TO 21
	60 - - - - - 70 - - - - - 50	1 0	2	60 TO 50	60 TO 70
	30 - - - - - 40 - - - - - 20	1 0	1	30 TO 20	30 TO 20



PRINTS TO

GENERAL ELECTRIC

70A106367

PRINT DIST. K6-24

MODIFICATION SPECIFICATIONS
MARK CENTURY 120

CONT. ON 1 SH. NO. 0

GENERAL NOTES

F.C.F.
FMF: AJH

APPROVED BY: W. N. Patterson DATE: 12-23-69

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A	ISSUE				
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D Nadler
Nov. 17, 1970

Made By W. N. Patterson

Issue Date Jan. 9, 1970

PROCESS COMPUTER PHOENIX, ARIZ.

Dwg. No. 70A106367
Cont. on 1 Sh. No. 0

PCE 20A 7-62

GENERAL

The purpose of this specification is to define the additions and changes tc be made to a standard GE Mark Century 120 Model 2 numerical positioning control for use with a GE-PAC 30 computer via a modified Byte-I/O Module.

Fundamentally, the MC120 when operated in the auto mode, will receive its data from the computer rather than the paper tape reader. However, for ease of maintenance and set-up, the paper tape equipment is to be retained. In general, the MC120's will run unattended and therefore, any operation which would throw it out of the 'cycle start' mode should be avoided. It is also desirable that the MC120 and the GE-PAC 30 not be tied together with DC control lines. Therefore, all communications will be by AC coupled electronic circuits or isolated by relay coil and contact.

Figure one is a Block Diagram of the overall situation:

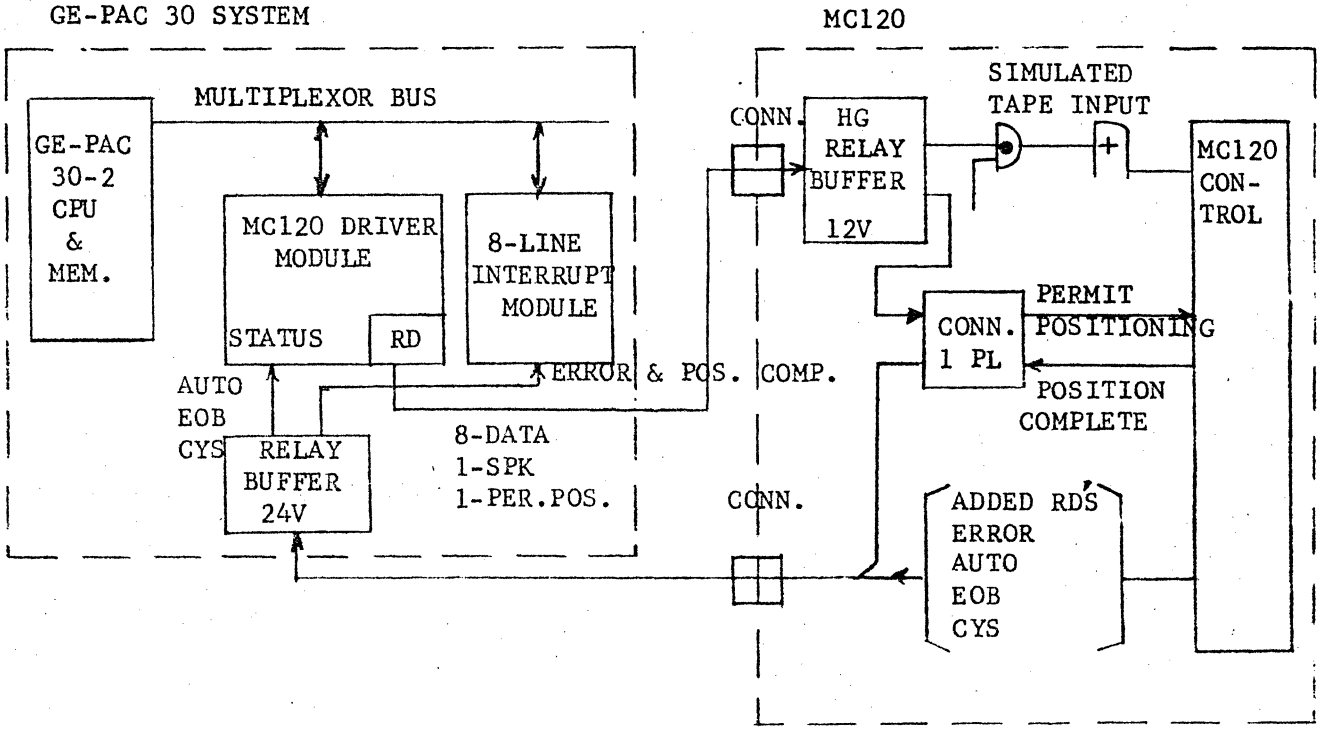

FIGURE 1

GENERAL (Cont'd)

The necessary changes are:

a. Mount two relay buffer cards supplied by PCD.

b. Modify tape input circuitry to accept computer simulated tape (8 data & one sprocket) signals in the Auto mode only.

c. Modify the Cycle Start logic so that a Reading Error (parity error) does not reset 'Cycle Start' Flip-Flop when in Auto.

d. Add, if necessary, a relay driver to drive an external 24 volt relay to provide a Reading Error (parity) signal to the computer.

e. Add relay drivers to drive external 24 volt relays to indicate to the computer the following; 'Auto' mode, EOB (End of Block) and Cycle Start.

DETAILS OF IMPLEMENTATION

In order to expedite the implementation of this modification, PCD will supply connectors and other mounting hardware to mount two IC3600KHSK3 Relay Cards. Each one of these cards has 8 - 12 volt mercury wetted relays. At a later time, PCD will actually supply two of these cards for each controller. Attachments include the drawings for the above relay card, connector & card guide. These drawings include an assembly drawing (further note orientation of relays and note that they must be within 15° of vertical), schematic and logic representation of card which includes pin numbers and other necessary information.

If it is any help as far as space or available spare circuits in this application, there will be no use made of the 'M' function decoding relays since all such actions are being directly controlled by the digital outputs from the computer.

In order to facilitate interconnection of the system, it is desirable to make the connections via connectors. This could be one connector for input and one for outputs or alternately they can be in one common connector. This is the service shops option. However, we do ask that the mating connector be supplied to PCD.

KHSK3 RELAY WIRING

The relay coils shall be wired to a common posi ive voltage with individual grounding through a driver switch. The relay outpu s for da a shall be wired from the normally closed contacts. The simulated sprocket & the permit pos itioning outputs shall be wired from the normally open contacts.

TESTING

To insure that the modifications meet the intent, prior to the availability of a computer and interface to test the entire sub-system, it should be tested with a simulated computer output. The simulated computer output could be composed of 9 toggle switches for data & permit position, a momentary pushbutton for sprocket signal. Provision will have to be made to cause the data to go to zero's on release of the sprocket signal. Three lights can be provided to indicate CYS, AUTO & EOB.

It should be ascertained that data can be correctly loaded to either X or Y register, that a parity error doesn't cause a drop out of CYCLESTART, permit positioning & position complete logic works correctly and that AUTO, CYS and EOB signals are brought to the interface connector.

DOCUMENTATION

The intent should be to modify the documentation so that a qualified numerical control servicemen can understand the changes and maintain the equipment without further aid.

It will be necessary to produce new sheets of drawings for those areas modified and to produce drawing covering the added equipment.

Furthermore, all the sets of Red books supplied with this order must be revised. It should be sufficient to change the Elementary Diagram & Wire Table Sections and to insert a page(s) in the Operation Chapter which identifies that there are modifications, the nature of the modifications and what descriptive sections that it might effect.

Purchase modification from:

General Electric Service Shop
3601 E. LaPalma
Anaheim, California 92806

Attention: Steven J. Krofchok
Manager, Special Manufacturing Operation
(714) 630-2650

GENERAL ELECTRIC

70A110396

PRINT DIST.	BYTE I/O MODULE	CONT. ON 1 SH.NO. 0
K7-19	PRODUCT SPECIFICATION	(02-058 A19)

GENERAL NOTES

F.C.F.

FMF: GE-PAC 30

APPROVED BY: E. J. White DATE: Sept 19, 69

REVISION STATUS

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A	ISSUE				
B	REVISED SH 1 PER	P. MILLER			
	AN 6WDW-44-012	Nov. 21, '69			
C	REV. SH. 1&2 PER	P. MILLER			
	AN 6WDW-44-015	Jan. 2, 1970			
D	REV. SH.1 PER	L.MORAES			
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	A1-097	JULY 27, 71			

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	Feb 19, 1970		

Issue Date 9/24/69

PROCESS COMPUTER PHOENIX, ARIZ.

Dwg. No. 70A110396 Cont. on 1 Sh. No. 0

Dept E. WHITE

PCE 20A 7-62

1. DOCUMENTATION

The following documents are shipped with the 02-058.
1 each 70A111162 Installation Specification
1 each 70A111091 Maintenance Specification
1 each 70A112471 Test Program
1 each 70B113259 (FS9)
1 each 70A110025 Information Specification.

2. PARTS LIST

1 each 32-023 Byte I/O Interface Board
3 each 17-069F04 Cable Assembly

3. DIMENSIONS

Mother-Board 9.75" x 10.5"

4. WEIGHT

Mother-Board: 1-1/2 pounds

5. POWER

+5 volts ± 10%; 0.75 amps

6. ENVIRONMENTAL

6.1 Temperature: 0° to 50°C

6.2 Humidity: Equal or exceeds processor

6.3 Vibration Equal or exceeds processor

7. DESCRIPTION

The 70A104048G78 (02-058) byte I/O module is a general purpose fully buffered interface module, for reading and writing bytes of data to/from byte oriented devices.

The interface can be connected directly to the I/O Multiplexor Bus in the Processor chassis or Expansion Card File.

The interface contains sixteen storage FF's connected as the devices inputs (eight data bit & eight command bit). The devices outputs appear on sixteen unstored lines, which can be interrogated by the Processor. (Eight data bit and eight status bit).

An interrupt line is provided which can interrupt the Processor when service is required. This line is available to the user for energization by a signal of his choosing.

8. ACCEPTANCE TEST

The interface must execute the test program described in 70A112471 in order to be considered operational. The program should also run under the prescribed voltage variations.

GENERAL ELECTRIC

70A110444

PRINT DIST.	PROGRAMMING SPECIFICATION	CONT. ON 1	SH. NO. 0
K7-15	BYTE I/O MODULE		

GENERAL NOTES

F.C.F.
FMF:

APPROVED BY: _____ DATE: 12-6-71

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A	Issued												

Made By	Issue Date	PROCESS	Dwg. No. 70A110444
J. Lima/LAP	DEC 9 197	COMPUTER PHOENIX, ARIZ.	Cont. on 1 Sh. No. 0

PCE 20A 7-62

REVISIONS

1. INTRODUCTION

This module provides a general purpose, fully buffered interface to 8-bit oriented devices for reading and writing bytes of data. The module provides:

A. Eight Data Output Lines, each with a storage flip-flop. The data lines may be updated by executing a 'Write Data' instruction.

B. Eight Data Input Lines, which may be read in by executing a 'Read Data' instruction. Data Input Lines to the module are brought in via a cable.

C. Eight Control Lines, each with a storage flip-flop, which may be updated by executing an 'Output Command' instruction.

D. Eight Sense Lines, the status of which may be read in by executing a 'Sense Status' instruction. These Sense Lines are brought into the module via a cable.

E. One Priority Interrupt Line which, when acknowledged by an "Acknowledge Interrupt" instruction, automatically transfers the device number of the module to the general register specified by the 'Acknowledge Interrupt' instruction.

The device number X'0B' is normally assigned to this device.

2. STATUS AND COMMAND BYTES

The actual configuration of the status and command bytes for this device depends upon the equipment connected to the module.

3. PROGRAMMING CONSIDERATIONS

R1 contains the device number.

A. Data may be transferred to the module by:

```
WD    R1,DATA
```

B. Data may be read from the module by:

```
RD    R1,DATA
```

C. Commands may be transmitted to the module by:

```
OC    R1,CMD
```

where CMD is a memory byte containing the desired information.

D. The module handles eight bits of status, which may be transferred to the processor by:

```
SSR    R1,R2   (Inputs status byte to R2)
```

K7-15

PRINTS TO

GENERAL ELECTRIC
PROCESS COMPUTERS
PHOENIX ARIZONA

TITLE FUNCTIONAL SCHEMATIC
BYTE I/O MODULE

DRAWING NUMBER	CONT	PAGE
70B113239	0A	0

FIRST MADE FOR GE-PAC-30
(FS9)

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME
D	ISSUED				
D,	REV SH. 0A, 3 PER AN	J.Morse			
	6WDW-44-014	DEC 24, '69			
E	REV. SH. 2 PER	F. Flores			
	AN 6WDW-44-019	APR. 20, 70			

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME

REISSUED

D	ISSUED
D,	Jan. 12, 1970
E	May 14, 1970

REISSUED

(FS9)

MADE BY	APPROVAL	REV.		DWG. NO.	CONT.	PAGE
[illegible] 27AUG69	E.G. White		D	70B113239	0A	0
ISSUED September 11, 1969	Sept 9 69			PRINTS TO: K7-08		

PCE 2101

DIST	UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING					GENERAL ELECTRIC	TITLE	DWG NO (FS9)
	APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES	PROCESS COMPUTER PHOENIX	FUNCTIONAL SCHEMATIC BYTE I/O MODULE FOR GE-PAC-30	70B113239
		√	±	±	±			CONT ON SHEET 1 SH NO 0A

SHEET INDEX

CONTENTS	SHEET NO.	SHEET ISSUE 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
SHEET INDEX SUPPORTING INFORMATION	0A	-	2	3																	
FUNCTIONAL SCHEMATICS	1	1	2	2																	
	2	1	2	2																	
	3	1	2	3																	
	4	1	2	2																	
	5	1	2	2																	
	6	1	2	2																	
BACK PANEL MAP	7	-	2	2																	
	ASSY PWB	SPARE	SPARE																		

SUPPORTING INFORMATION

CATEGORY	PART NO.
MOTHER BOARD ASSEMBLY	3E-023R01

SHEET INDEX NOTES:

1. CHANGES ON THIS DRAWING SHALL REQUIRE ONLY THE REISSUE OF SHEETS AFFECTED.
2. THE ISSUE OF THIS SHEET SHALL DETERMINE THE LATEST ISSUE OF THIS DRAWING.
3. IN THE EVENT THAT THE REVISION LEVEL STAMPED ON THE PWB DOES NOT CORRESPOND TO THAT IN THE SUPPORTING INFORMATION TABLE, PLEASE REQUEST SCHEMATIC OF THE CORRECT REVISION LEVEL FROM:
"GENERAL ELECTRIC COMPANY
40 FEDERAL ST.
WEST LYNN, MASSACHUSETTS 01905".

DRAWN BY	DATE	CHKD BY	DATE	REV.		ISSUE NO. (FS9)
J. Cummings	27 AUG 69	E.A. White	Sept 1 '69	D		70B113239
ISSUED	Sept 11, 1969	APPD		D_1		CONT ON SHEET 1 SH NO. 0A

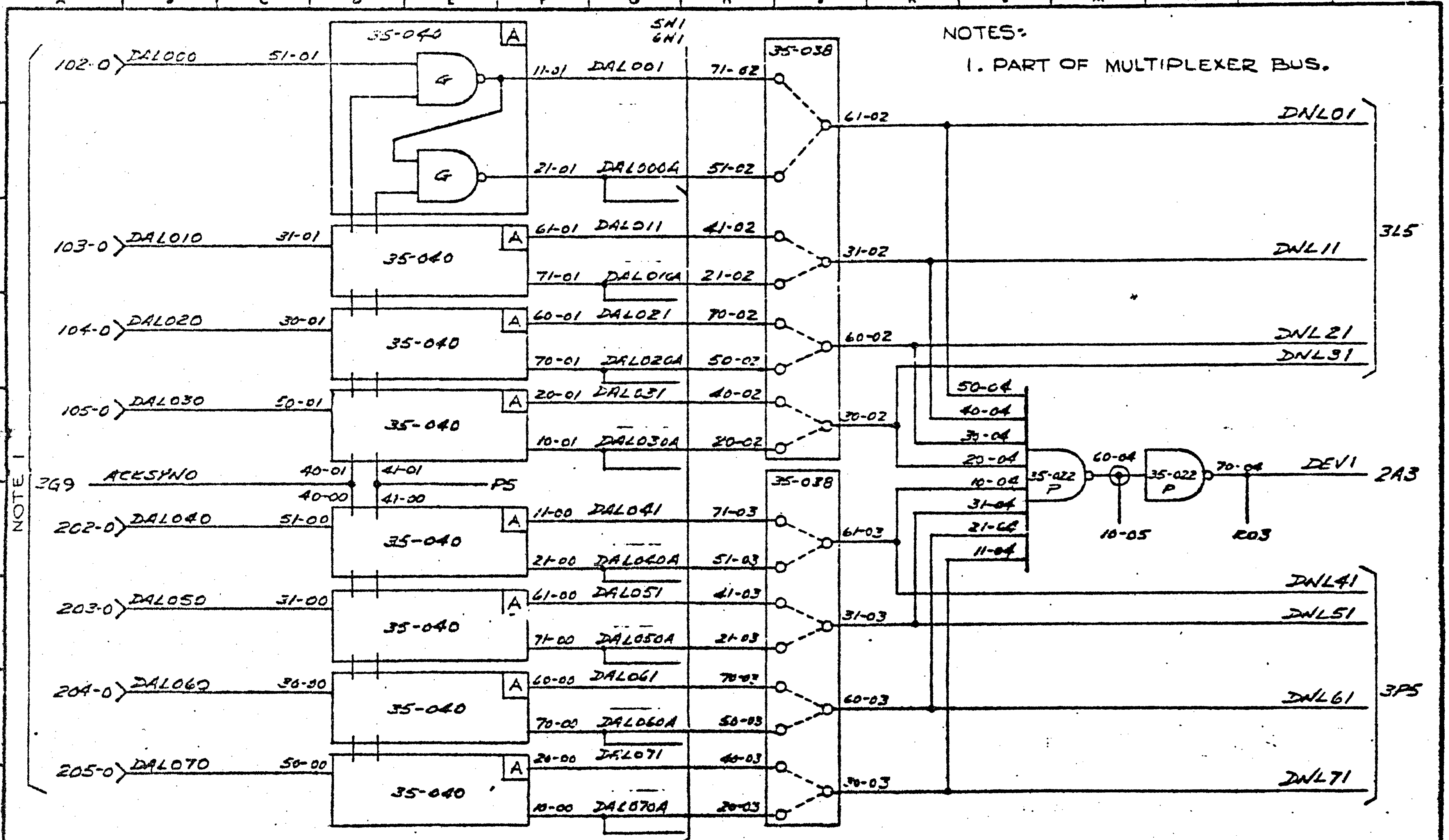
UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING —

APPLIED PRACTICES | SURFACES √ | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE
FUNCTIONAL SCHEMATIC
BYTE I/O MODULE
GE-PAC-30

DWG. NO. (FS9)
70B113239
CONT ON SHEET 2 SH NO 1



NOTES:
1. PART OF MULTIPLEXER BUS.
NOTE 1
102-0 DAL000 51-01
103-0 DAL010 31-01
104-0 DAL020 30-01
105-0 DAL030 50-01
3G9 ACKSYNO 40-01 40-00 41-01 41-00 P5
202-0 DAL040 51-00
203-0 DAL050 31-00
204-0 DAL060 30-00
205-0 DAL070 50-00
35-040 A
G
SN1 6N1
11-01 DAL001 71-02
21-01 DAL000A 51-02
61-01 DAL011 41-02
71-01 DAL010A 21-02
60-01 DAL021 70-02
70-01 DAL020A 50-02
20-01 DAL031 40-02
10-01 DAL030A 20-02
11-00 DAL041 71-03
21-00 DAL040A 51-03
61-00 DAL051 41-03
71-00 DAL050A 21-03
60-00 DAL061 70-03
70-00 DAL060A 50-03
20-00 DAL071 40-03
10-00 DAL070A 20-03
35-038
61-02 31-02 60-02 30-02 61-03 31-03 60-03 30-03
DNL01 DNL11 DNL21 DNL31 3L5
DNL41 DNL51 DNL61 DNL71 3P5
50-04 40-04 30-04 20-04 10-04 31-04 21-04 11-04
35-022 P
60-04
10-05
70-04 DEV1 2A3
R03

MADE BY J. [signature] 27 AUG 69
ISSUED Sept 11, 1969
APPROVAL E. G. White Sept 9, 69
REV. D

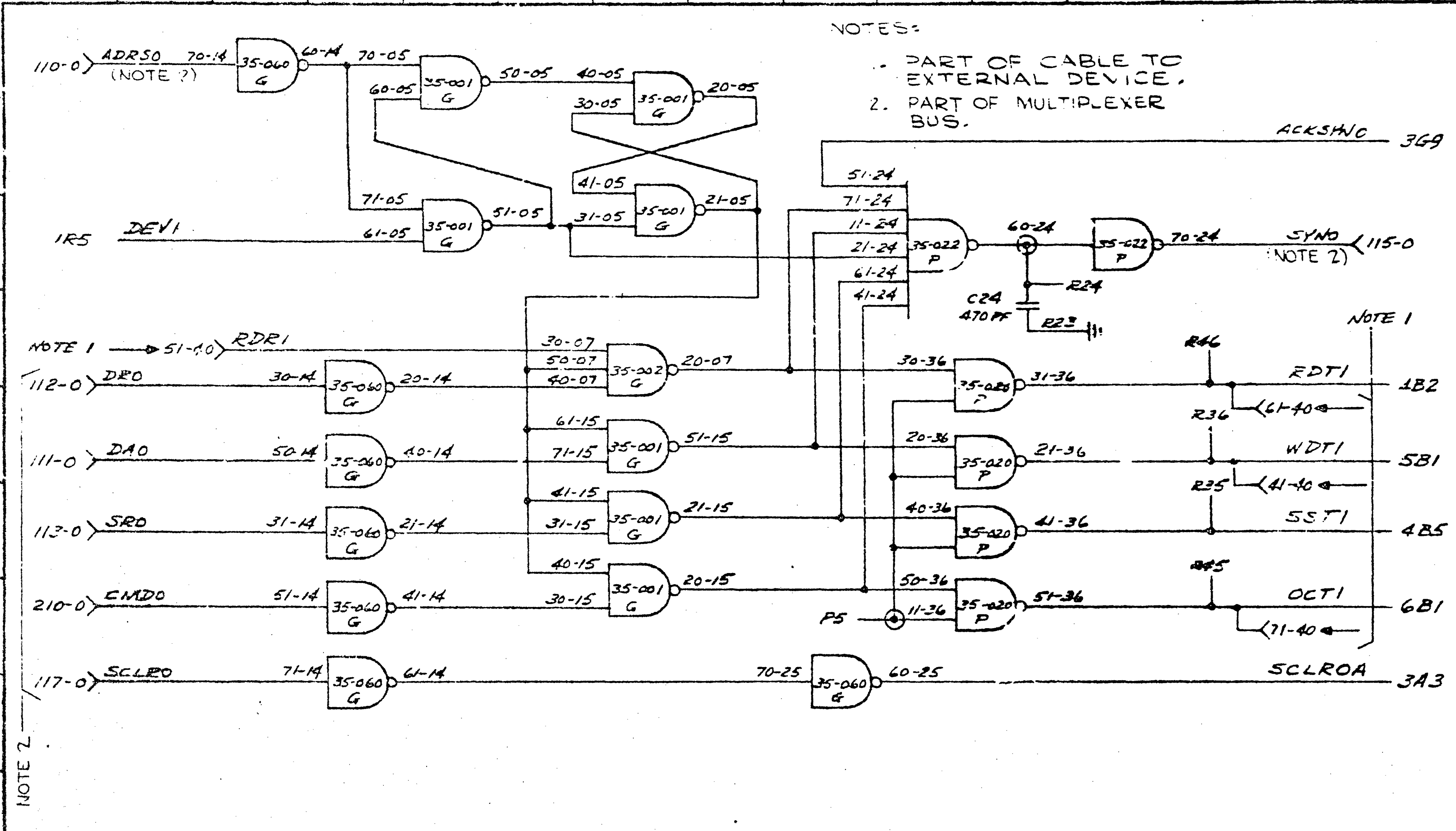
DWG. NO. (FS9)
70B113239
CONT ON SHEET 2 SH NO. 1

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING —			
APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS	
	√	FRACTIONS ±	DECIMALS ±	ANGLES ±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
BYTE I/O MODULE
GE-PAC-30

DWG NO (FS9) 70B113239
CONT ON SHEET 3 SH NO 2



DRAWN BY	27 AUG 69	APPROVAL			REV
ISSUED	Sept 11, 1969		CHKR		

DWG NO (FS9) 70B113239
CONT ON SHEET 3 SH NO 2

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

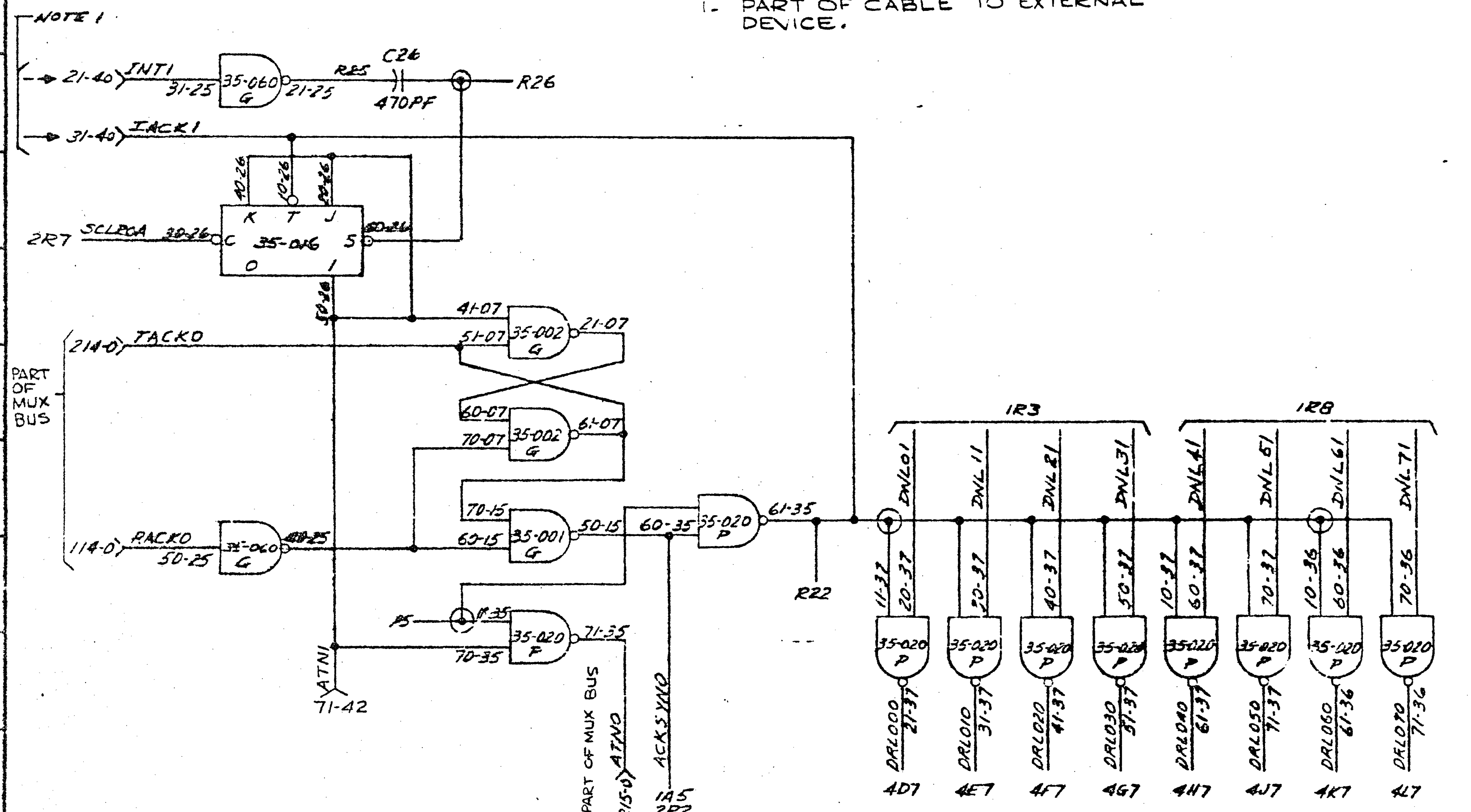
UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING -

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	V	±	±	±

TITLE FUNCTIONAL SCHEMATIC
BYTE I/O MODULE
GE-PAC-30

DWG NO. (FS9) 70B113239
CONT. ON SHEET 4 SH NO. 3

NOTES:
1. PART OF CABLE TO EXTERNAL DEVICE.



NOTE 1
21-40
INT1
31-25
35-060 G
21-25
RES
C26
470PF
R26
31-40
IACK1
40-26
10-26
K T J
2R7
SCLPGA
35-016
S
0 1
50-26
41-07
51-07
35-002 G
21-07
214-0
IACKO
PART OF MUX BUS
60-07
70-07
35-002 G
61-07
70-15
60-15
35-001 G
50-15
60-35
35-020 P
61-35
114-0
RACKO
50-25
35-060 G
R22
P5
35-020 P
71-35
70-35
ATN1
71-42
PART OF MUX BUS
ATNO
215-0
ACKSYNO
1A5
2R2
IR3
IR8
DNL01
DNL11
DNL21
DNL31
DNL41
DNL51
DNL61
DNL71
11-37
20-37
30-37
40-37
50-37
10-37
60-37
70-37
10-36
60-36
70-36
35-020 P
DRL000 21-37
DRL010 31-37
DRL020 41-37
DRL030 51-37
DRL040 61-37
DRL050 71-37
DRL060 61-36
DRL070 71-36
4D7
4E7
4F7
4G7
4H7
4J7
4K7
4L7

MADE BY	ISSUED			REV.	
J. [illegible] 27 AUG 69	E. G. [illegible] 1-9-69			D	
Sept 11, 1969				D1	

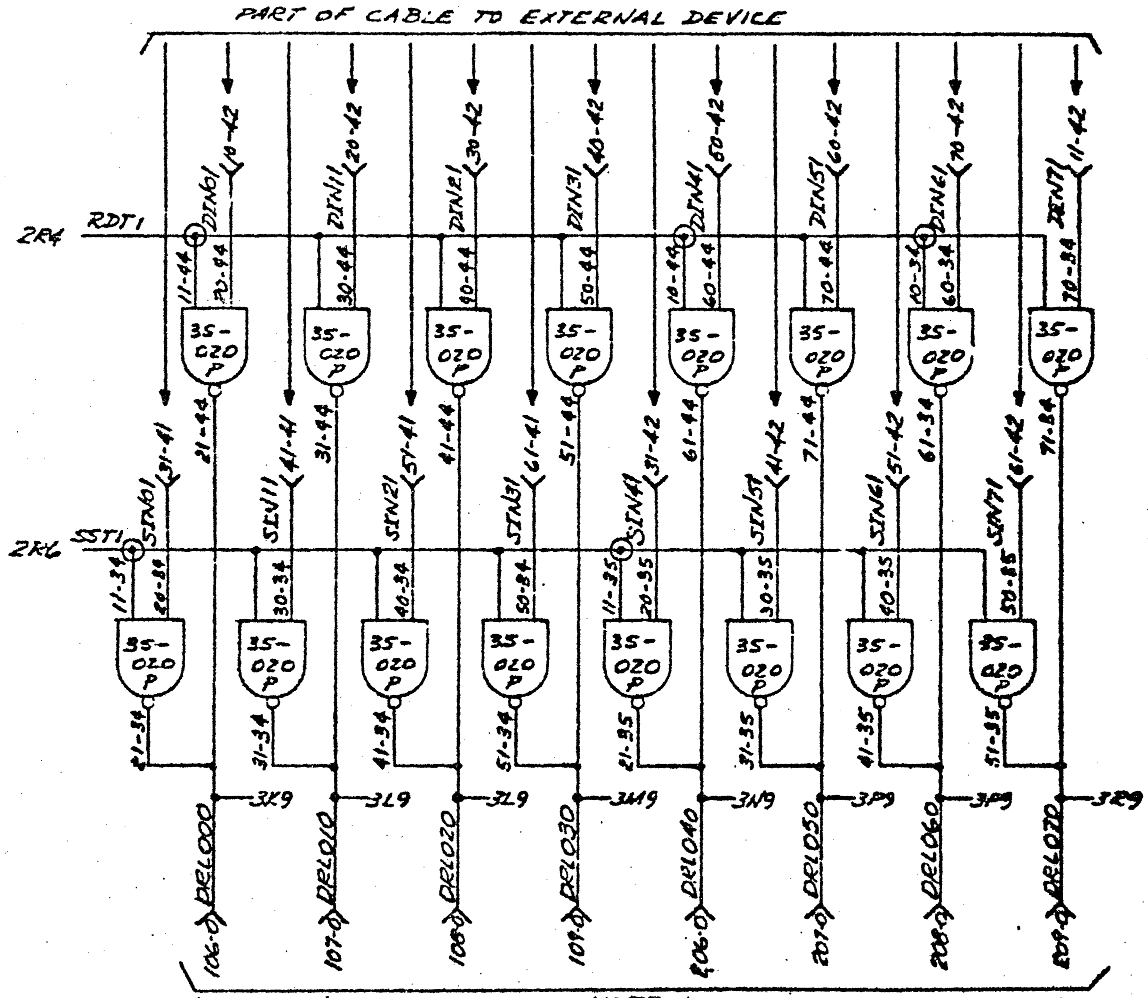
DWG NO. (FS9) 70B113239
CONT ON SHEET 4 SH NO. 3

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
BYTE I/O MODULE
GE-PAC-30

DWG NO. (FS9) 70B113239
CONT. ON SHEET 5 SH NO. 4

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING —



NOTES:

1. PART OF MULTIPLEXER BUS.

MADE BY J. [signature] 27 AUG 69
ISSUED Sept. 11, 1969
APPROVAL [signature] Sept 9 '69
REV. D

DWG. NO. (FS9) 70B113239
CONT. ON SHEET 5 SH NO. 4

DIST.

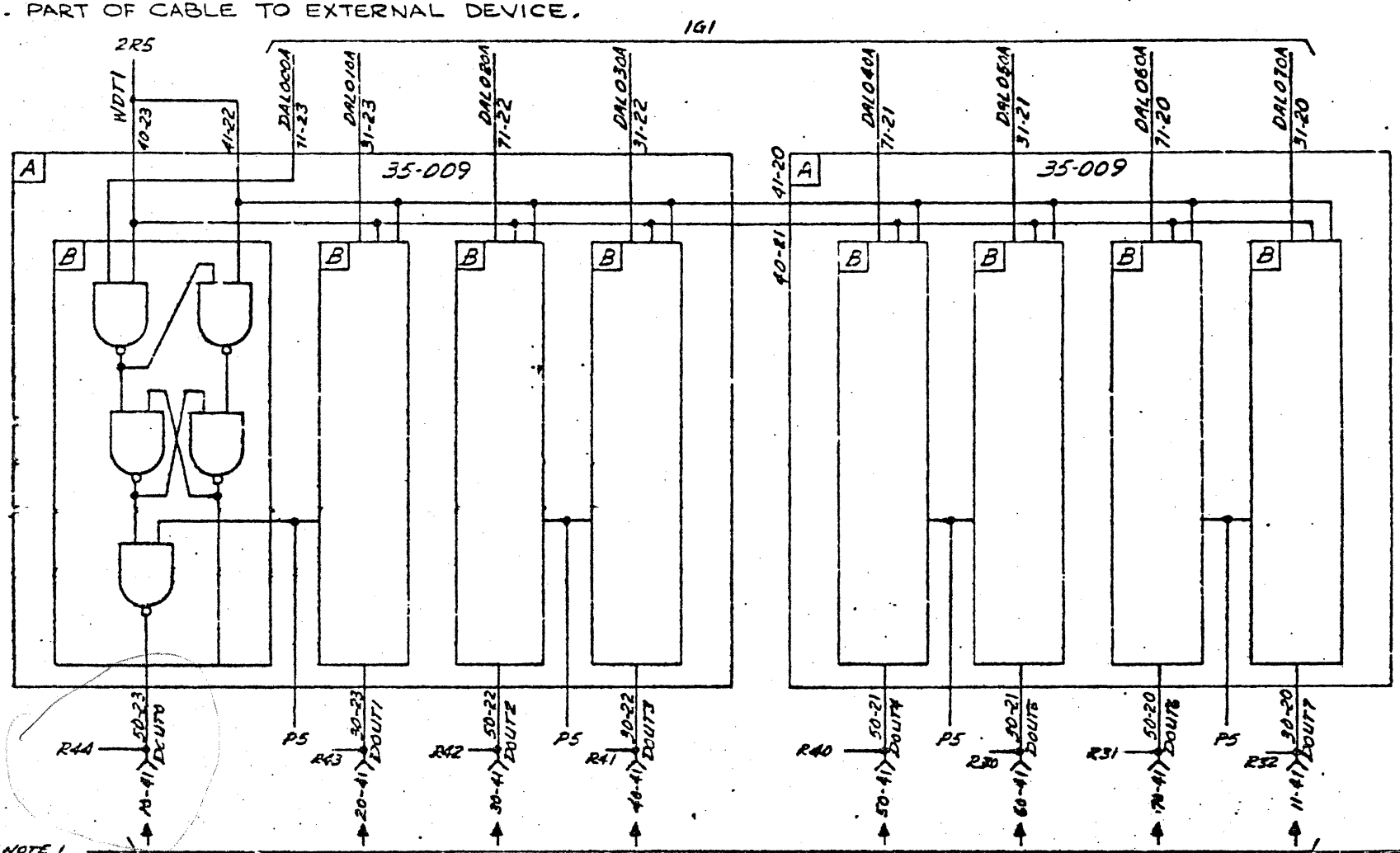
UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING
APPLIED PRACTICES | SURFACES: V | TOLERANCES ON MACHINED DIMENSIONS ONLY: FRACTIONS ± | DECIMALS ± | ANGLES ±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
BYTE I/O MODULE
FOR GE-PAC-30 I FCF

DWG NO (FS9)
70B113239
SHEET 6 OF DWG NO. 5

NOTES:
1. PART OF CABLE TO EXTERNAL DEVICE.



DRAWN BY J. Lyman 27 AUG 69	APPROVED E. C. White Sept 9, 64	DES.	REV. D	DWG. NO. (FS9) 70B113239	
RELEASED Sept 14 1969		CHKD.		SHEET 6 OF DWG NO. 5	

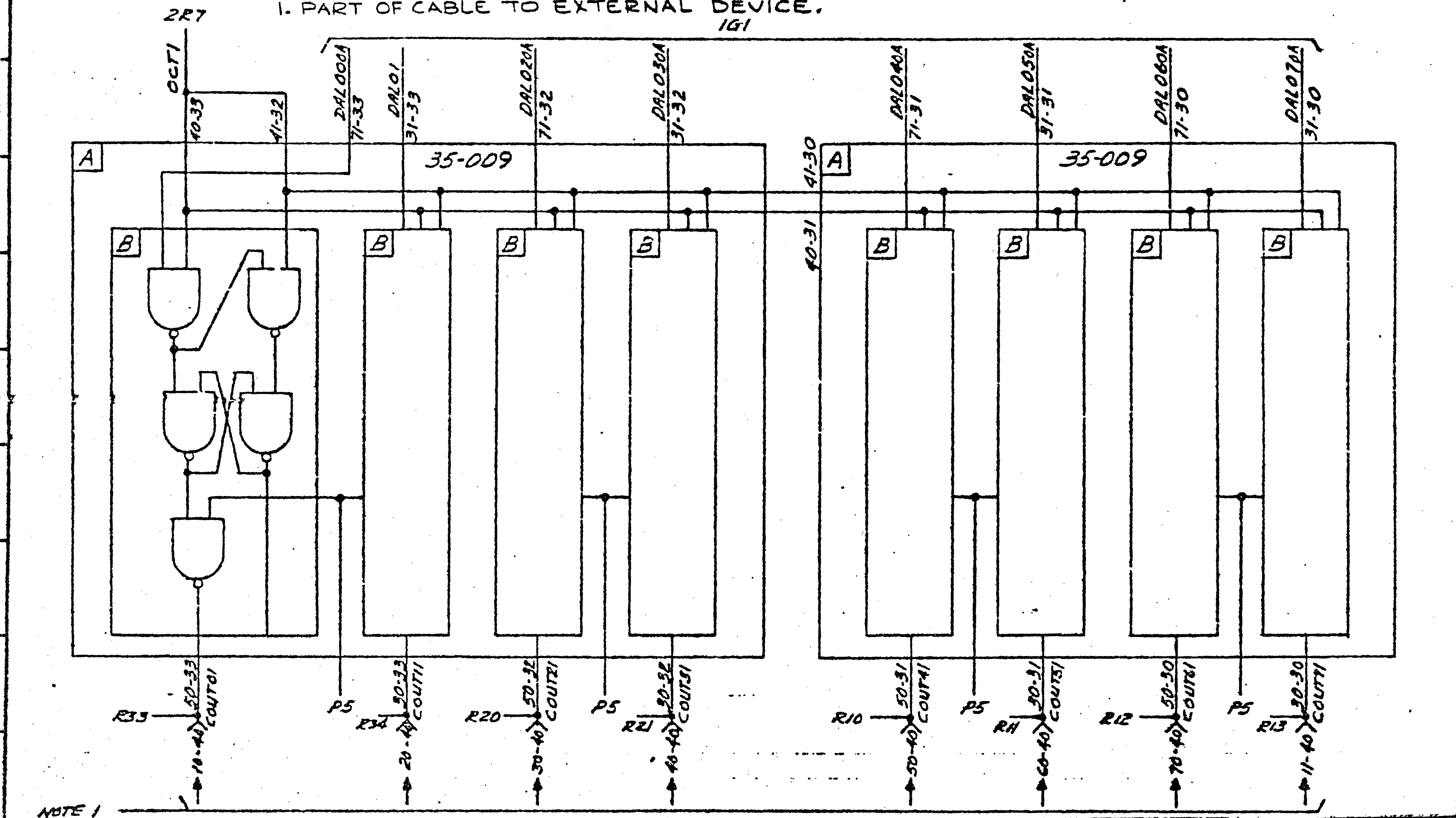
GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

FUNCTIONAL SCHEMATIC
BYTE I/O MODULE
GE-PAC-30

DWG NO. (FS9) 70B113239
CONT ON SHEET 7 SH NO. 6

NOTES:

1. PART OF CABLE TO EXTERNAL DEVICE.



MADE BY 27 AUG 69
APPROVAL Sept 9, 69
Sept 11, 1969
D

DWG NO. (FS9) 70B113239
CONT ON SHEET 7 SH NO. 6

		FUNCTIONAL SCHEMATIC BYTE I/O MODULE		(FS9) 70B113239
UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING: APPLIED PRACTICES / SURFACES √ / TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± DECIMALS ± ANGLES ±	GENERAL ELECTRIC PROCESS COMPUTER PHOENIX	TITLE FUNCTIONAL SCHEMATIC BYTE I/O MODULE	GE-PAC-30	DWG NO (FS9) 70B113239 CONT ON SHEET F SH NO 7

BACK PANEL MAP

CONN POS																			
MOTH. BD																			
	VERT. POS	HORIZ POS			HORIZ POS			HORIZ POS			HORIZ POS			HORIZ POS			HORIZ POS		
		0	1	2	0	1	2	0	1	2	0	1	2	0	1	2	0	1	2
1	22																		
	21																		
	20																		
	19																		
	18																		
	17																		
	16																		
	15																		
	14																		
	13																		
	12																		
	11																		
	10																		
	09																		
	08																		
	07																		
	06																		
	05																		
	04																		
	03																		
	02																		
	01																		
	00																		
0	22																		
	21																		
	20																		
	19																		
	18																		
	17		SCLRO																
	16																		
	15		SYNO	ATNO															
	14		CACKO	TACKO															
	13		SCO																
	12		[illegible]																
	11		[illegible]																
	10		ADCSO	CMDO															
	09		DRL030	DRL070															
	08		DRL020	DRL080															
	07		DRL010	DRL050															
	06		DRL000	DRL040															
	05		DAL030	DAL070															
	04		DAL020	DAL060															
	03		DAL010	DAL050															
	02		DAL000	DAL040															
	01																		
	00																		

MADE BY	APPROVAL	DES.	REV.	
J. [illegible] 27 AUG 69	E. C. White		D	DWG NO (FS9) 70B113239
ISSUED Sept 11, 1969	Sept 9, 69	CHKD		CONT ON SHEET F SH NO 7

GENERAL ELECTRIC

70C180660 SH NO 0

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING

APPLIED PRACTICES	SURFACES	ALLOWANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	✓	±	±	±

TITLE LOGIC

MC 120 DRIVER MODULE

FIRST MADE FOR SYS. STD

FSE: AJH

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME
A	ISSUE				
B	REV SH 1,2,3, PER AN 8AJH-22-005	Nov 2,70			
C	REV. SH 6-8 PER AN 8AJH-22-008	Dec 21 70			

REISSUED

A [illegible]
B Jan 22 1971
C Jan 19, 1971

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME

REISSUED

REV NO.

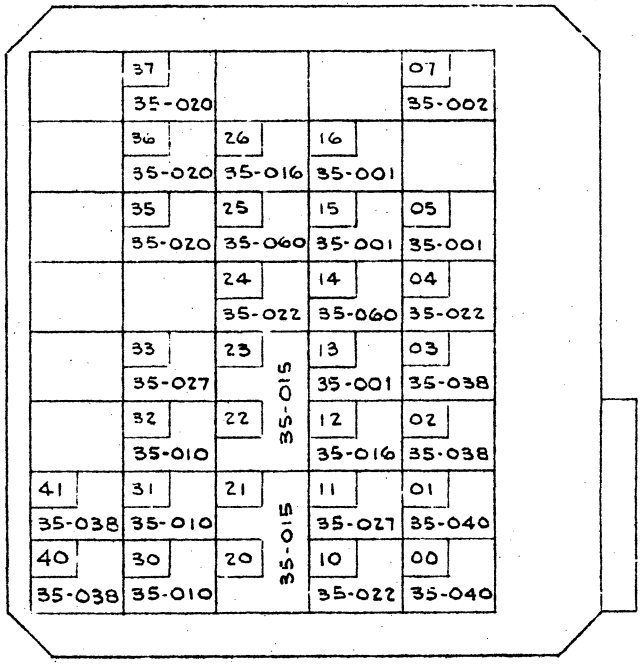
PROPRIETARY INFORMATION OF GENERAL ELECTRIC COMPANY

REVISIONS	PRINTS TO
	K6-17

CR [illegible] 24 FEB 70 DCT 19 1970	APPROVED 10/6/70	PROCESS COMPUTER DEPT PHOENIX	70C180660 SH NO 0

DESCRIPTION	SHEET NUMBER	DAUGHTER BOARD LOCATIONS	DAUGHTER BD. PART NO. VENDOR	DAUGHTER BD. PART NO. G.E.
SUPPORTING INFORMATION	0			
	1			
INTERFACE SUMMARY	2			
BLK & TIMING DIAG.	3			
DATA OUT ADDRESS DECODE	4	00, 01	35-040	70A110382G35
		02, 03	-038	G31
		04	-027	G22
CONTROL CIRCUIT	5	24	-022	G22
		05, 15	-001	G1
		14	-060	G49
		36	-020	G20
INTERRUPT CONTROL	6	36, 35	020	G20
		10	-022	G22
		15, 16	-001	G1
		07	-002	G2
		26	-016	G16
		25	-060	G49
		23	-015	G15
DATA TIMING-STATUS INPUT	7	33, 11	-027	G27
		35, 36, 37	-020	G20
DATA REGISTER-RELAY DRIVER	8	12	-016	G16
		30, 31, 32	-10	G10
		20, 21, 22, 23	35-015	70A110382G15

SHEET INDEX



MC120 DRIVER MODULE

BACK PANEL INTERFACE MAP

CONN POS					
MOTH BD.					
VERT POS.	HORIZ POS				
	0	1	SH	2	SH
1 22					
21					
20					
19					
18					
17					
16					
15					
14					
13					
12					
11					
10					
09					
08					
07					
06					
05					
04					
03					
02					
01					
00					
0 22		P5		GND	
21					
20					
19					
18					
17		SCLRO			
16					
15		SYNO		ATNO	
14		RACKO		TACKO	
13		SRO			
12					
11		A			
10		ADRSO		CMDO	
09		DRL030		DRL070	
08		DRL020		DRL060	
07		DRL010		DRL050	
06		DRL000		DRL040	
05		DAL030		DAL070	
04		DAL020		DAL060	
03		DAL010		DAL050	
02		DAL000		DAL040	
01		P15			
00		P5		GND	

MNEMONIC DEFINITIONS

ACKSYN	ACKNOWLEDGE SYNC.
AD	ADDRESS STORE
ADRS	ADDRESS CONTROL SIGNAL
ASYN	ADDRESS SYNC
ATN	ATTENTION INTERRUPT
AUTO	AUTOMATIC MODE
BSY	BUSY
CMD	COMMAND CONTROL SIGNAL
CYS	CYCLE START
DA	DATA AVAILABLE CONTROL SIGNAL
DAL	DATA AVAILABLE LINE
DEV	DEVICE NUMBER
DL	DATA LINE OUTPUT
DNL	DATA LINE STATUS GATING
DRL	DATA REQUEST LINE
EOB	END OF BLOCK, DATA
EOBNC	END OF BLOCK, NUMERICAL CONTROL
OCT	OUTPUT COMMAND GATING SIGNAL
PPOS	PERMIT POSITION OUTPUT
RACK	RETURN ACKNOWLEDGE INTERRUPT
RSDA	RESET DATA REGISTER
RSPK	RESET SPROCKET FLIP FLOP
SCLR	SYSTEM CLEAR CONTROL SIGNAL
SPK	SPROCKET OUTPUT
SR	STATUS REQUEST CONTROL SIGNAL
SSPK	SET SPROCKET FLIP FLOP
SYN	SYNCHRONIZATION SIGNAL
SST	SERVICE STATUS GATING SIGNAL
TACK	TRANSMIT ACKNOWLEDGE INTERRUPT
WDT	WRITE DATA GATING SIGNAL
XRP	EXTRA RESISTER PULL-UP
ATNR	ATTENTION FLIP FLOP RESET
ATNS	ATTENTION FLIP FLOP SET
EOBR	END OF BLOCK STORE FLIP FLOP RESET
EOBST	END OF BLOCK STORE FLIP FLOP TOGGLE

TEST POINTS IMPLEMENTED

DESIG	MNEMONIC	SHEET
L01	EOBBA	6
L02	SSPK1	7
L03	RSPK1	7
L04	RSPKO	7
L05	SSPKO	7
L06	BSY1	7
L07	RSDA1A	7
L08	BSYO	7
L09	RSDAO	7
L10	DA1	5
L11	ATN1	6
L12	OCT1	6
L13	WDT1	5

GENERAL ELECTRIC

70C180660

4 3

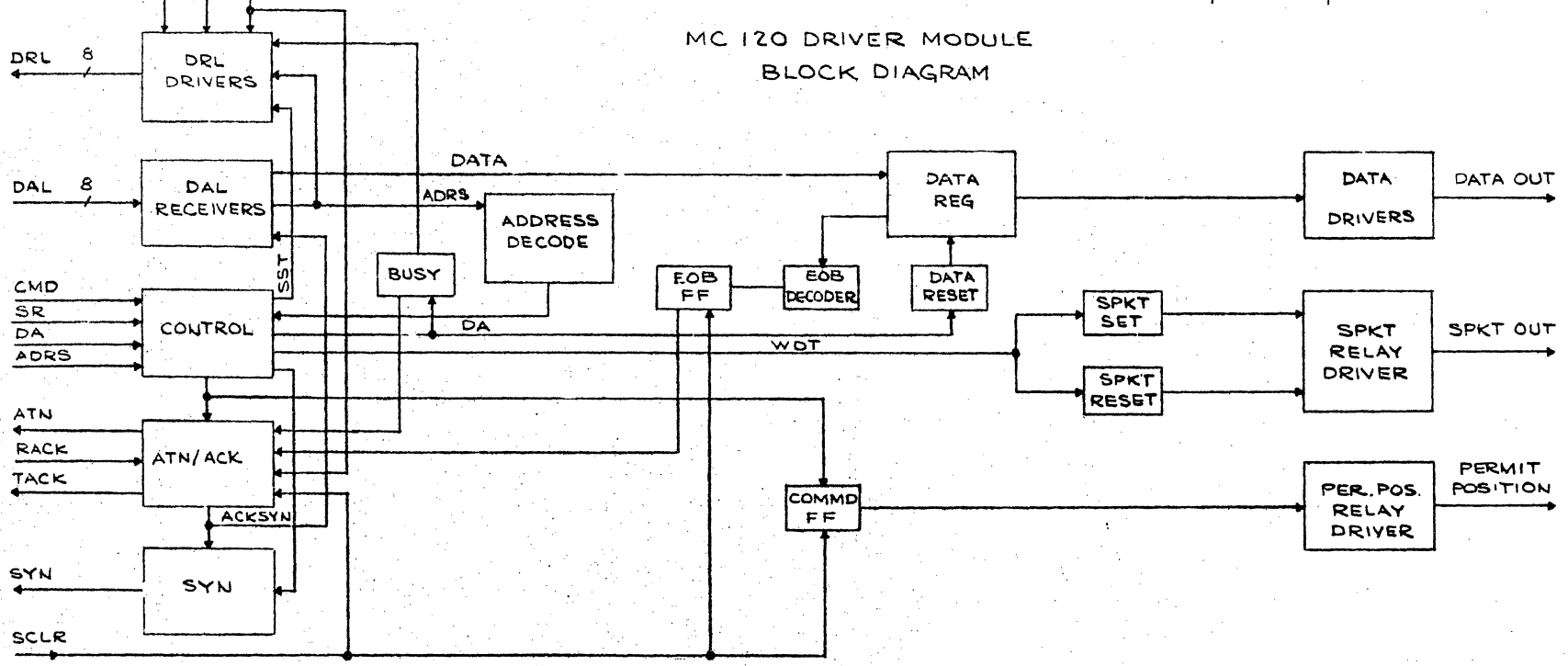
UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:
APPLIED PRACTICES | SURFACES ✓ | STANDARDS ON MACHINED SURFACES: FRACTIONAL ± | DECIMALS ± | ANGULAR ±

TITLE LOGIC

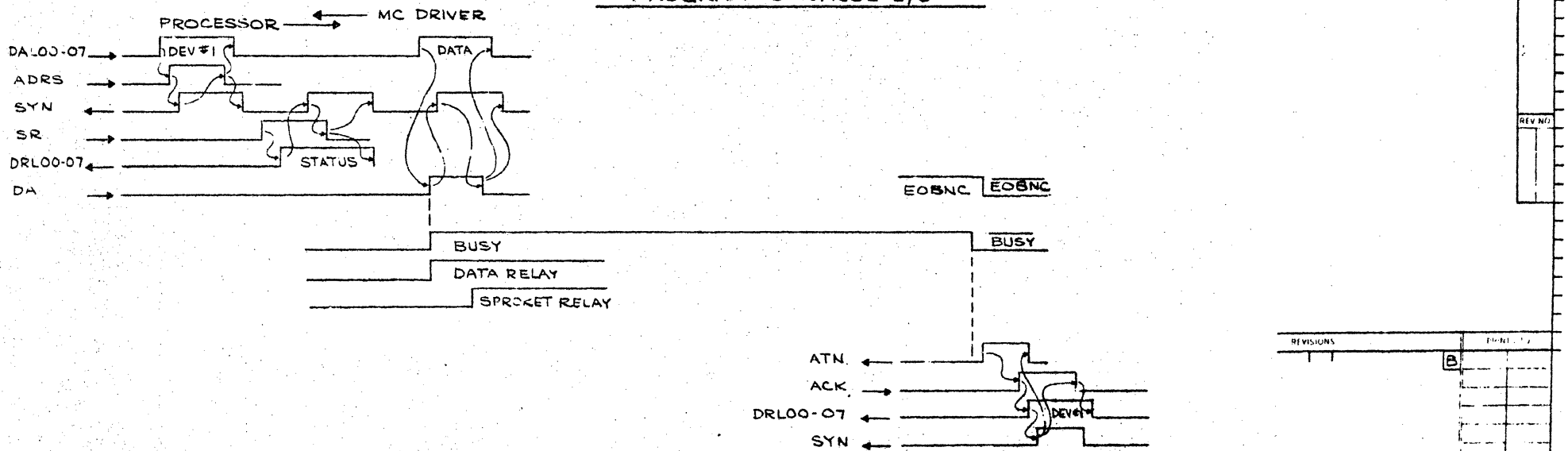
BLOCK AND TIMING DIAGRAM

FIRST MADE FOR SYS. STP.

MC 120 DRIVER MODULE BLOCK DIAGRAM



PROGRAM CONTROL I/Ø



REV NO

REVISIONS

B

			PROCESS COMPUTER DEPT. PHOENIX	70C180660
				4 5

APPROVED: Morse 25 FEB 70
DRAWN: OCT 19 1970

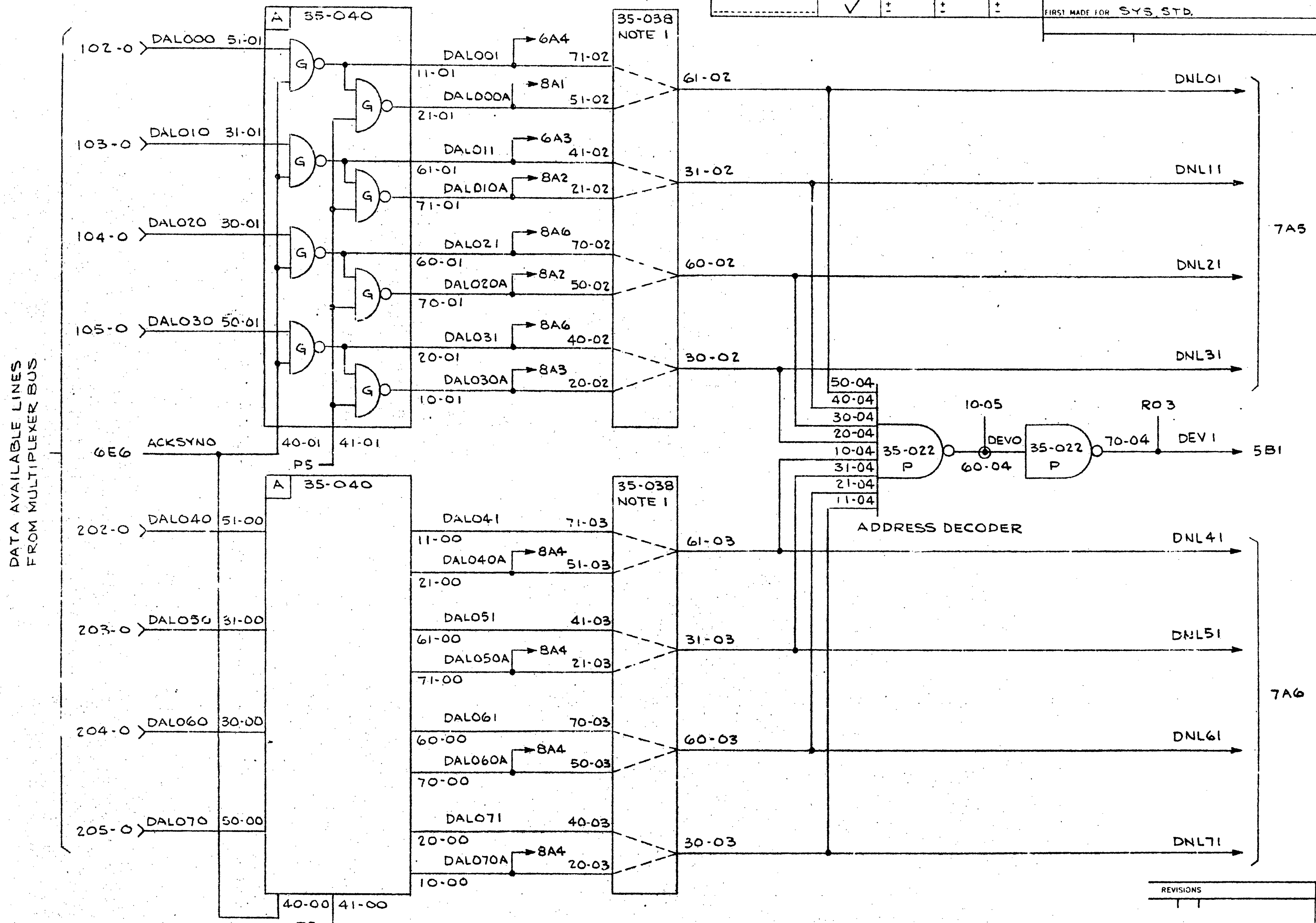
2 3 4 5 6

GENERAL ELECTRIC 180660 5 4

TITLE LOGIC DATA OUT & ADDRESS DECODE

FIRST MADE FOR SYS. STD.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING: APPLIED PRACTICES | SURFACES ✓ | TOLERANCES ON FINISHED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±



DATA AVAILABLE LINES FROM MULTIPLEXER BUS
A 35-040
35-038 NOTE 1
102-0 DAL000 51-01
103-0 DAL010 31-01
104-0 DAL020 30-01
105-0 DAL030 50-01
DAL001 6A4 71-02 11-01
DAL000A 8A1 51-02 21-01
DAL011 6A3 41-02 61-01
DAL010A 8A2 21-02 71-01
DAL021 8A6 70-02 60-01
DAL020A 8A2 50-02 70-01
DAL031 8A6 40-02 20-01
DAL030A 8A3 20-02 10-01
61-02 DNL01
31-02 DNL11
60-02 DNL21
30-02 DNL31
7A5
6E6 ACKSYNO 40-01 41-01 PS
202-0 DAL040 51-00
203-0 DAL050 31-00
204-0 DAL060 30-00
205-0 DAL070 50-00
DAL041 71-03 11-00
DAL040A 8A4 51-03 21-00
DAL051 41-03 61-00
DAL050A 8A4 21-03 71-00
DAL061 70-03 60-00
DAL060A 8A4 50-03 70-00
DAL071 40-03 20-00
DAL070A 8A4 20-03 10-00
40-00 41-00 PS
61-03 DNL41
31-03 DNL51
60-03 DNL61
30-03 DNL71
7A6
50-04 40-04 30-04 20-04 10-04 31-04 21-04 11-04
35-022 P
10-05 DEVO 60-04
35-022 P 70-04 R03 DEV1 5B1
ADDRESS DECODER

NOTE:

1. THE ADDRESS FOR THIS MODULE IS WIRED ON THESE ADDRESS STRAP DAUGHTER BOARDS (35-038). ADDRESS IS NORMALLY WIRED FOR X '09'.

REVISIONS | PRINTS TO

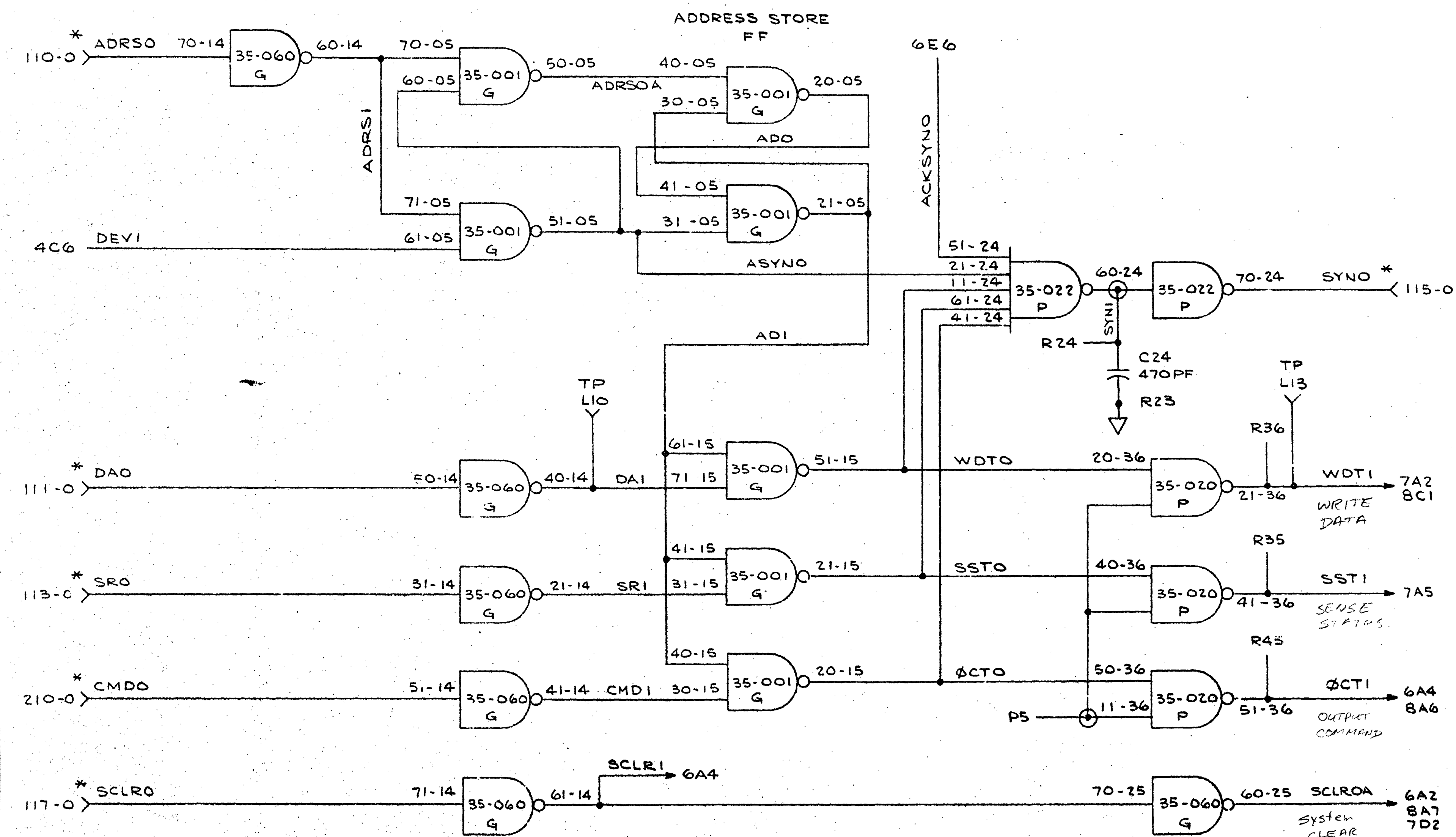
ISSUED 26 JAN 70 OCT 19 1970 | APPROVALS | PROCESS COMPUTER PHOENIX | 70C180660 CONT ON SHEET 5 SH NO 4

CONTROL CIRCUIT

LOGIC

FIRST MADE FOR SYS. STD.

APPLIED PRACTICES | SURFACES ✓


ADDRESS STORE FF
110-0 ADRSO 70-14 35-060 G 60-14
70-05 35-001 G 50-05 ADRSOA
60-05
40-05 35-001 G 20-05
30-05
ADO
ADRSI
41-05 35-001 G 21-05
31-05
71-05 35-001 G 51-05
4C6 DEVI 61-05
ASYNO
6E6
ACKSYNO
51-24
21-24
11-24
61-24
41-24
35-022 P 60-24
SYNI
35-022 P 70-24 SYNO 115-0
R24
C24 470PF
R23
ADI
TP L10
TP L13
111-0 DAO 50-14 35-060 G 40-14 DAI
61-15 35-001 G 51-15
71 15
WDTO
20-36 35-020 P 21-36
R36
WDTI 7A2 8C1
WRITE DATA
113-0 SRO 31-14 35-060 G 21-14 SRI
41-15 35-001 G 21-15
31-15
SSTO
40-36 35-020 P 41-36
R35
SSTI 7A5
SENSE STATUS
210-0 CMDO 51-14 35-060 G 41-14 CMDI
40-15 35-001 G 20-15
30-15
ØCTO
50-36 35-020 P 51-36
11-36
P5
R45
ØCTI 6A4 8A6
OUTPUT COMMAND
117-0 SCLRO 71-14 35-060 G 61-14
SCLRI 6A4
70-25 35-060 G 60-25 SCLROA 6A2 8A7 7D2
System CLEAR

* PART OF MULTIPLEXER BUS.

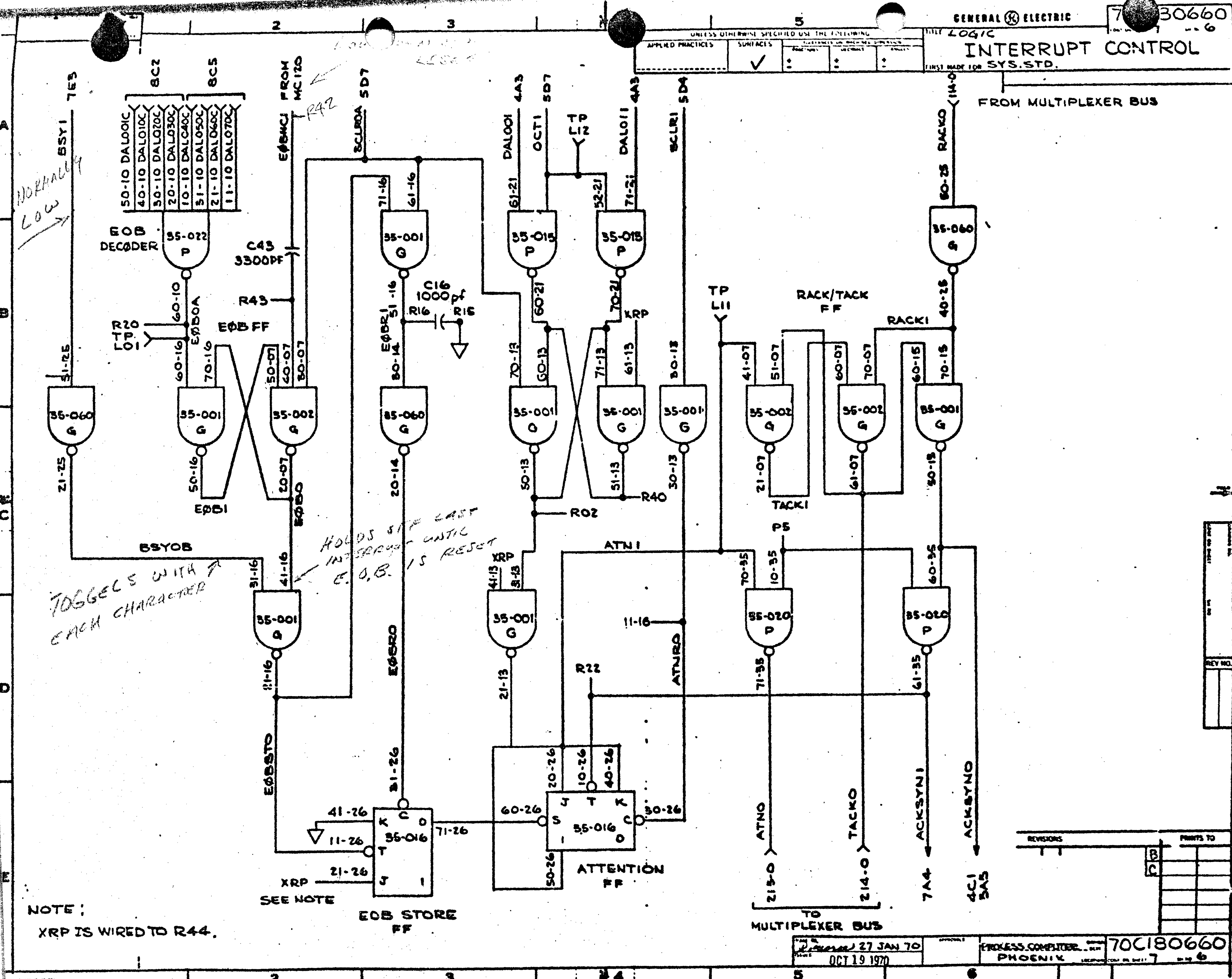
REVISIONS | PRINTS TO

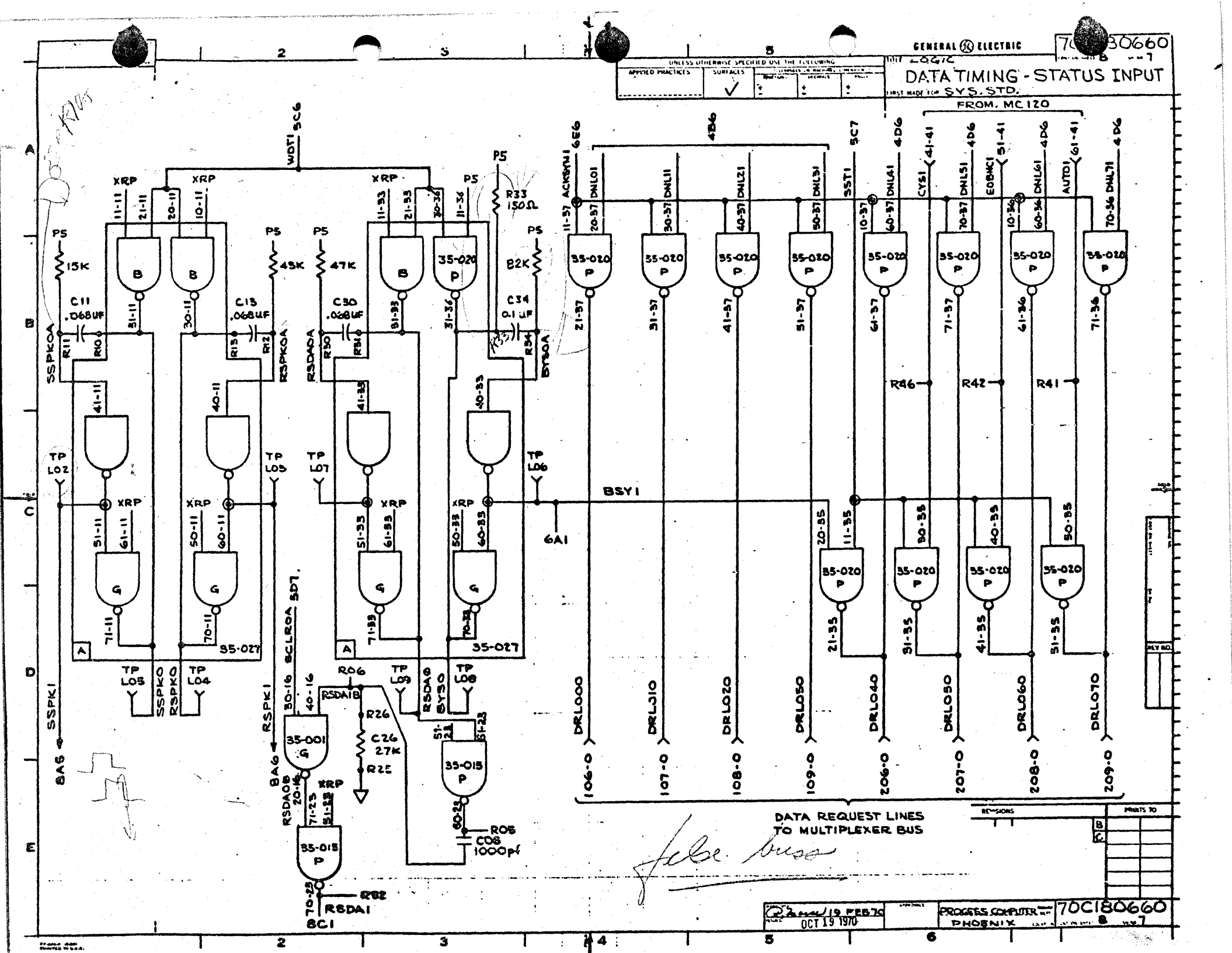
MADE BY: 27 JAN 70
ISSUED: OCT 19 1970

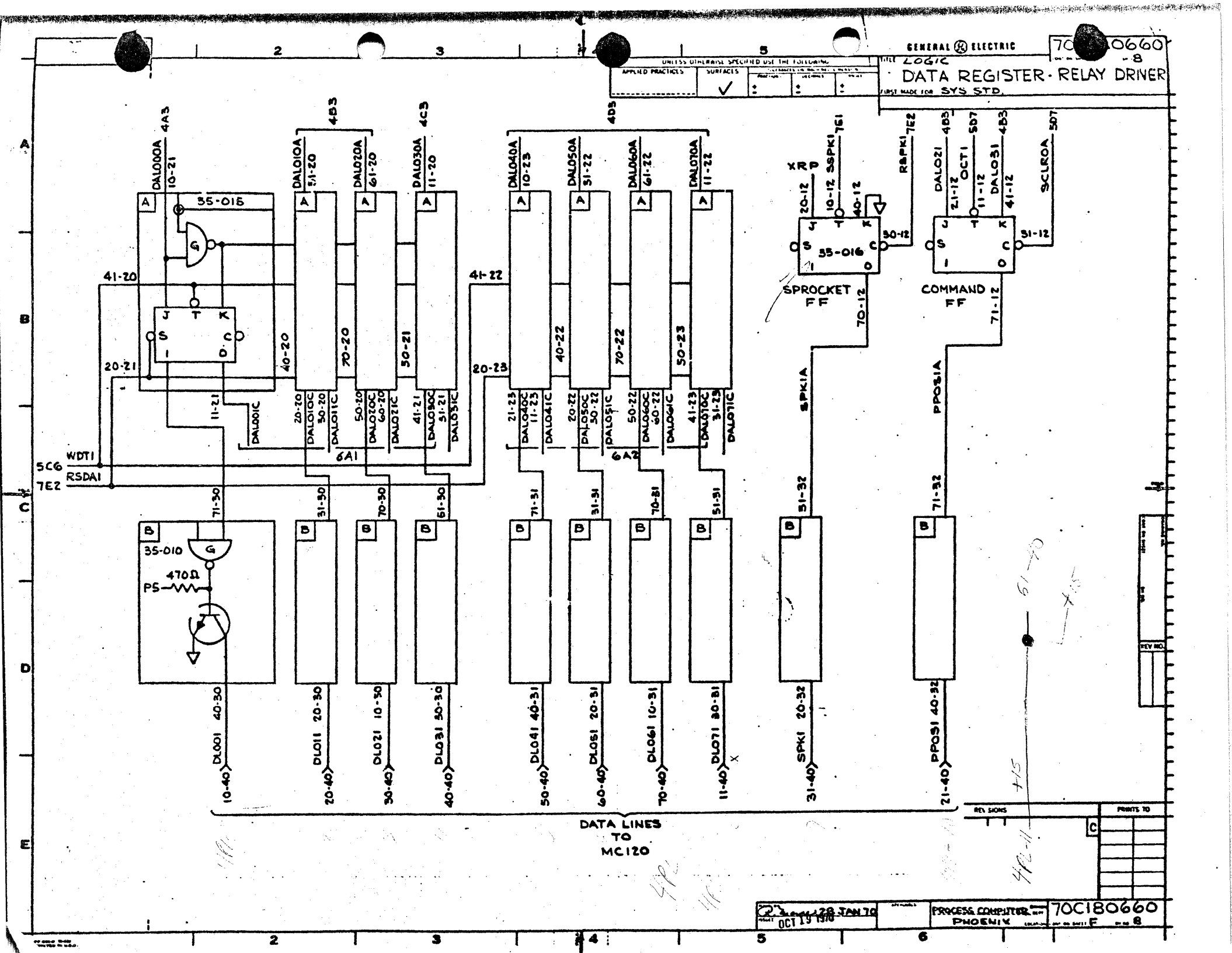
PROCESS COMPUTER DEPT — PHOENIX

70C180660

CONT ON SHEET 6 — SH NO 5


GENERAL ELECTRIC
70C180660
LOGIC
INTERRUPT CONTROL
SYS. STD.
FROM MULTIPLEXER BUS
EOB DECODER
EØB FF
RACK/TACK FF
EOB STORE FF
ATTENTION FF
TO MULTIPLEXER BUS
NORMALLY LOW
TOGGLES WITH EACH CHARACTER
HOLDS THE LAST INTERRUPT UNTIL E.O.B. IS RESET
NOTE:
XRP IS WIRED TO R44.
27 JAN 70
OCT 19 1970
PROCESS COMPUTER
PHOENIX


GENERAL ELECTRIC
70C180660
DATA TIMING - STATUS INPUT
SYS. STD.
FROM MC120
WDT1 5C6
P5
15K
45K
47K
82K
R33 150Ω
C11 .068UF
C13 .068UF
C30 .068UF
C34 0.1 UF
SSPKOA
RSPKOA
RSDAOA
BYSOA
XRP
35-020
35-027
35-001
35-015
35-018
ACKSYN1 6E6
DNL01
DNL11
DNL21
DNL31
SST1 5C7
DNLA1 4D6
CYS1 41-41
DNLS1 4D6
EOBKC1 51-41
DNL61 4D6
AUTO1 61-41
DNL71 4D6
BSY1
6A1
R46
R42
R41
DRL000
DRL010
DRL020
DRL030
DRL040
DRL050
DRL060
DRL070
106-0
107-0
108-0
109-0
206-0
207-0
208-0
209-0
DATA REQUEST LINES TO MULTIPLEXER BUS
TP L02
TP L05
TP L04
TP L07
TP L06
TP L09
TP L08
SSPKO
RSPKO
SSPKI
RSPKI
BA6
SCLR0A 5D7
RSDA0B
RSDAIB
R26
C26 27K
R25
R06
C06 1000pf
R02
RSDAI
8C1
REVISIONS
PRINTS TO
OCT 19 1970
PROGRESS COMPUTER
PHOENIX
70C180660


GENERAL ELECTRIC
70C180660
-8
UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING
APPLIED PRACTICES
SURFACES
TITLE LOGIC
DATA REGISTER - RELAY DRIVER
FIRST MADE FOR SYS STD.
DALO00A 4A3
10-21
35-015
DALO10A 4B3
51-20
DALO20A
61-20
DALO30A 4C3
11-20
DALO40A 4D3
10-23
DALO50A
51-22
DALO60A
61-22
DALO70A
11-22
41-20
40-20
70-20
50-21
41-22
40-22
70-22
50-23
20-21
20-23
DALO01C
DALO10C 20-20 50-20
DALO11C
DALO20C 50-20 60-20
DALO21C
DALO30C 41-21 51-21
DALO31C
DALO40C 21-23 11-23
DALO41C
DALO50C 20-22 50-22
DALO51C
DALO60C 50-22 60-22
DALO61C
DALO70C 41-23 31-23
DALO71C
6A1
6A2
WDT1
5C6
RSDA1
7E2
11-21
71-30
31-30
70-30
61-30
71-31
31-31
70-31
51-31
35-010
470Ω
PS
DL001 40-30
DL011 20-30
DL021 10-30
DL031 30-30
DL041 40-31
DL051 20-31
DL061 10-31
DL071 30-31
10-40
20-40
30-40
40-40
50-40
60-40
70-40
11-40
DATA LINES TO MC120
XRP
20-12
10-12
SSPK1 7G1
40-12
35-016
50-12
SPROCKET FF
70-12
SPK1A
51-32
SPK1 20-32
31-40
R&PK1 7E2
DALO21 4B3
21-12
OCT1 5D7
11-12
DALO31 4B3
41-12
SCLR0A 5D7
51-12
COMMAND FF
71-12
PPOS1A
71-32
PPOS1 40-32
21-40
REVISIONS
PRINTS TO
C
28 JAN 70
OCT 19 1970
PROCESS COMPUTER PHOENIX
70C180660
F
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